ML2216-XXX/ML22P16

Oki ADPCM2 Algorithm-Based Speech Synthesis LSI

GENERAL DESCRIPTION

The ML2216-XXX is speech synthesis device with a 8Mbit P2ROM built-in.
The ML2216-XXX incorporates ADPCM2 decoder, 12-bit D/A converter, and low-pass filter. Moreover, the monophonic speaker amplifier for driving a direct speaker is built in.
The ML2216-XXX carried out all functions required for a voice response circuit to one chip. For this reason, inclusion to small and pocket equipment became still easier.

ML2216-xxx serves as write-in shipment.
ML22P16 is speech synthesis device with 8M bit OTP memory built-in. User is able to program a device one time by using exclusive tool.

FEATURES

- Built-in memory capacity and the Maximum playback time length (please refer to the following table)

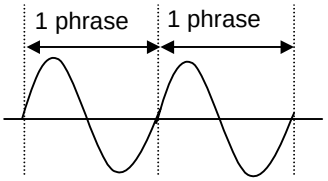
Type	ROM capacity	Maximum playback time length (sec) (In 4-bit ADPCM2)		
		F_{SAM} = 4.0 kHz	F_{SAM} = 8.0 kHz	F_{SAM} = 16 kHz
ML2216/ML22P16	8 Mbit	524	262	131

- Non-linear 8-bit PCM, 8-bit PCM, 16-bit PCM, and 4-bit ADPCM2 algorithms
- Sampling frequency: 4.0 kHz, 5.3 kHz, 6.4 kHz, 8.0 kHz, 10.7 kHz, 12.8 kHz, 16.0 kHz
- 12-bit D/A converter built in
- Built-in low-pass filter: Digital filter
- Amplifier built-in for a speaker drive: 0.3W 8Ω(At VDD=5.0V)
- CPU interface: 3 line type serial clock synchronization
- Maximum number of phrases: 256 phrases
- Volume control function: VOLUME command (16 step / OFF)
- Repeat function: LOOP command
- Master clock frequency: 4.096 MHz
- Power supply voltage: 2.7V to 3.6V or 4.5V to 5.5V
- Operating temperature: -20°C to +85°C
- Package: 44-pin plastic QFP (QFP44-P-910-0.80-2K)
  (ML2216-XXXGA, ML22P16GA)

Table below summarizes the points of difference between the ML2250 family and the ML2216/ML22P16.

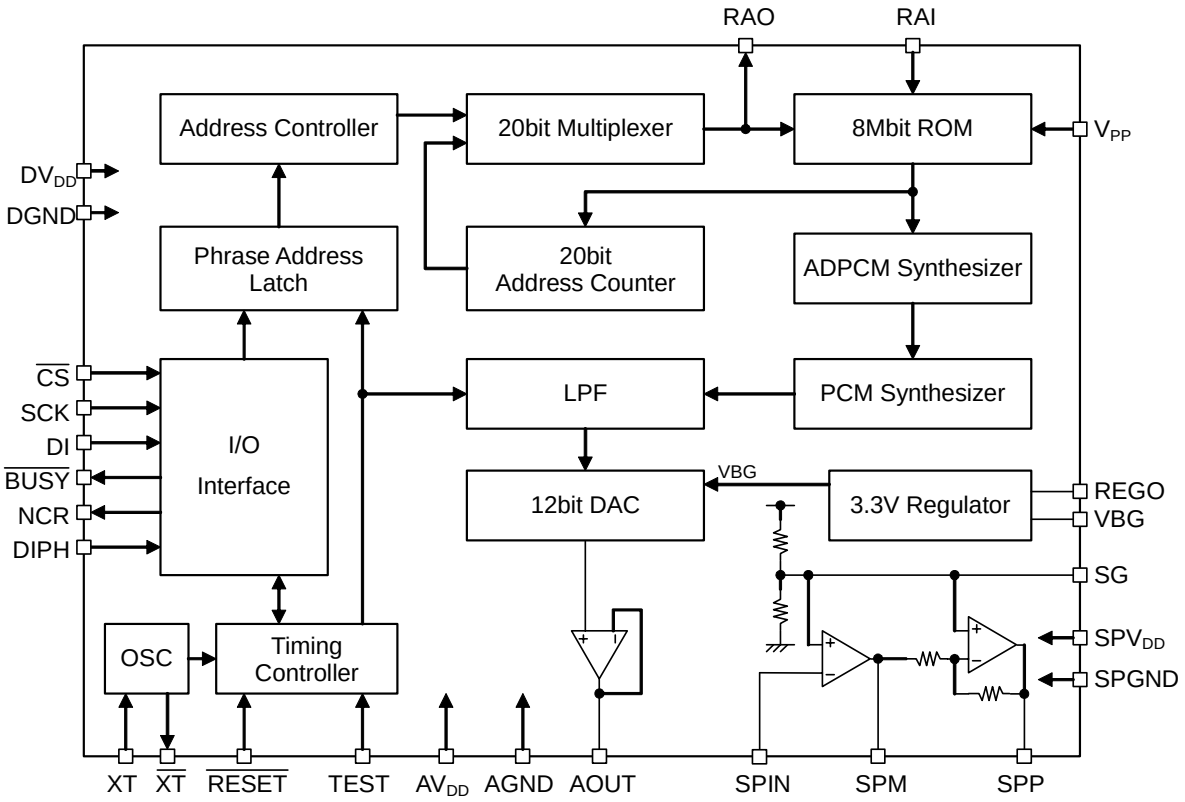
	ML2250 family	ML2216/ML22P16
Interface	Parallel or serial	Serial
Playback method	2-bit ADPCM2 4-bit ADPCM2 8-bit PCM 8-bit non-linear PCM 16-bit PCM	4-bit ADPCM2 8-bit PCM 8-bit non-linear PCM 16-bit PCM
Max. number of phrases	256	256
Sampling frequency (kHz)	4.0/5.3/6.4/8.0/10.7/12.8/16.0/21.3/25.6/32.0/42.7/48.0	4.0/5.3/6.4/8.0/10.7/12.8/16.0
Clock frequency	4.096 MHz	4.096 MHz
D/A converter	Voltage type: 14 bits	Current type: 12 bits
Low-pass filter	FIR type interpolation filter	Secondary comb filter
Amplifier for a speaker drive	None	built-in
Number of channels	2 channels	1 channel
Phrase control table	Both 2 channels without user definable phrase restrictions	1 channel without user definable phrase restrictions
Volume adjustment	29 steps (–2 dB/–5 dB steps)	16 steps
Silent insertion function	built-in(4ms to 1024ms)	built-in(20ms to 1024ms)
Repeat function	No limit	No limit
Seam silence interval in continuous playback	0 (Note)	0 (Note)
Others	External data input possible	—
Package	44-pin plastic QFP	44-pin plastic QFP

Note: Continuous playback shown in the figure below is possible.



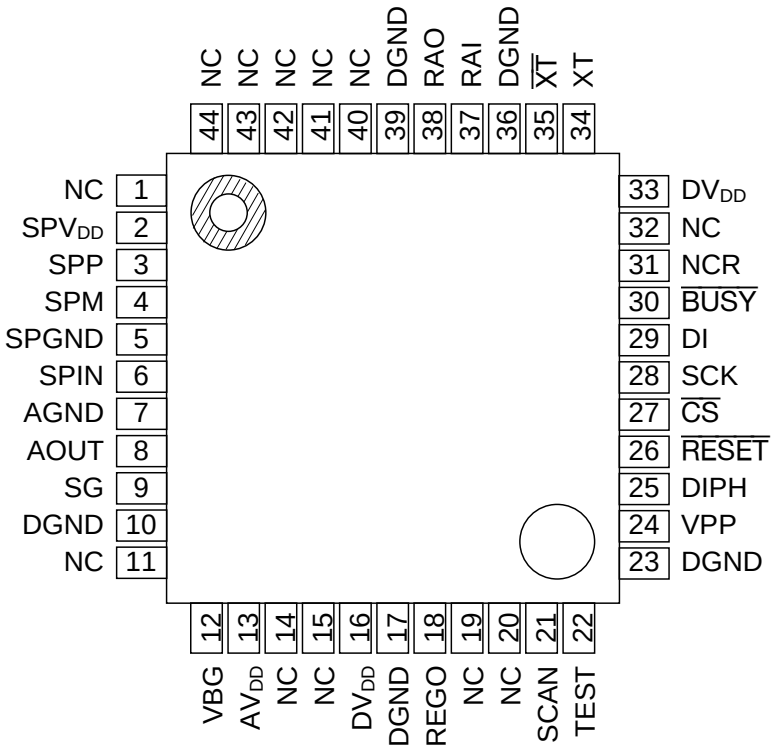
No silence interval

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)

44-pin plastic QFP



NC: No Connection

PIN DESCRIPTIONS

Pin	Symbol	Type	Description
26	$\overline{\text{RESET}}$	I	reset input pin. At “L” level input, the device enters the initial state. During reset input, operation of all circuits stops and it will be in a power down state. Input the "L" level at the time of a power supply injection. After power supply voltage is stabilized, please make it "H" level.
27	$\overline{\text{CS}}$	I	CPU interface chip select pin. A serial interface becomes effective on the "L" level.
28	SCK	I	serial clock input pin.
29	DI	I	serial data input pin.
25	DIPH	I	A DIPH pin chooses the timing which takes in serial data inside LSI. When a DIPH pin is the "L" level, DI input data is taken in inside LSI by the rising edge of a SCK clock. When a DIPH pin is "H" level, DI input data is taken in inside LSI by the falling edge of a SCK clock.
30	$\overline{\text{BUSY}}$	O	A $\overline{\text{BUSY}}$ pin outputs the signal which shows a phrase reproduction state. The "L" level is outputted during reproduction.
31	NCR	O	A NCR pin outputs the signal which shows the input permission state of a command. When the NCR pin is "H" level ,a command input is possible. When the NCR pin is the "L" level ,a command input cannot be performed.
34	XT	I	Wired to a crystal or ceramic oscillator. A feedback resistor of around 1 MΩ is built in between this XT pin and $\overline{\text{XT}}$ pin (pin 35). When using an external clock, input the clock from this pin. When you use a crystal or ceramic oscillator, please connect with the latest of LSI as much as possible.
35	$\overline{\text{XT}}$	O	Wired to a ceramic or crystal oscillator. When using an external clock, keep this pin open. When you use a crystal or ceramic oscillator, please connect with the latest of LSI as much as possible.
18	REGO	O	Regulator output pin. It becomes the power supply of Built-in P2ROM. Insert a 10 μF or larger capacitor between this pin and DGND pin.
12	VBG	O	Standard voltage output pin for 3.3V regulators. Insert a 0.1 μF capacitor between this pin and DGND pin.
9	SG	O	Standard voltage output pin of built-in speaker amplifier. Insert a 0.1 μF or larger capacitor between this pin and AGND pin.
8	AOUT	O	Analog output pin. When you input into built-in speaker amplifier, insert a 10 μF capacitor between this pin and SPIN pin.

Pin	Symbol	Type	Description
6	SPIN	I	Analog input pin of built-in speaker amplifier. A reversal amplifier consists of connecting external resistance between AOUT pin and SPM pin.
4	SPM	O	Analog output pin of built-in speaker amplifier. A speaker is connected between SPM pin and SPP pin. External resistance is connected between SPIN pin and this pin.
3	SPP	O	Analog output pin of built-in speaker amplifier. A speaker is connected between SPM pin and SPP pin.
38	RAO	O	Address output pin of Built-in P2ROM. It connects with RAI pin directly.
37	RAI	I	Address input pin of Built-in P2ROM. RAO pin is connected directly.
24	VPP	I	Program power supply pin at the time of the data writing to P2ROM. Input “L” level to this pin.
22	TEST	I	Test pin for the device. Input “L” level to this pin. This pin has a pull-down resistor built in.
21	SCAN	I	Test pin for the device. Input “L” level to this pin. This pin has a pull-down resistor built in.
16, 33	DV_{DD}	—	Digital power supply pin. Insert a 0.1 μF or larger bypass capacitor between this pin and DGND pin.
10, 17, 23, 36, 39	DGND	—	Digital ground pin.
13	AV_{DD}	—	Analog power supply pin. Insert a 0.1 μF or larger bypass capacitor between this pin and AGND pin.
7	AGND	—	Digital ground pin.
2	SPV_{DD}	—	Speaker amplifier ower supply pin. Insert a 10 μF or larger bypass capacitor between this pin and SPGND pin.
5	SPGND	—	Speaker amplifier Ground pin.

ABSOLUTE MAXIMUM RATINGS

(DGND = AGND = SPGND = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Digital power supply voltage	DV_{DD}	Ta = 25°C	–0.3 to +7.0	V
Analog power supply voltage	AV_{DD}		–0.3 to +7.0	V
Speaker amplifier power supply voltage	SPV_{DD}		–0.3 to +7.0	V
Input voltage	V_{IN}	Ta = 25°C	–0.3 to DV_{DD} +0.3	V
Permissible loss	P_D		1.66	W
Output short-circuit current	I_{SC}	Except SPM and SPP and REGO pin	10	mA
		SPM and SPP pin	540	mA
		REGO pin	40	mA
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(DGND = AGND = SPGND = 0 V)

Parameter	Symbol	Condition	Range			Unit
Digital power supply voltage	DV_{DD}	When not using a regulator	2.7 to 3.6			V
		When using a regulator	4.5 to 5.5			V
Analog power supply voltage	AV_{DD}	When not using a regulator	2.7 to 3.6			V
		When using a regulator	4.5 to 5.5			V
Speaker amplifier power supply voltage	SPV_{DD}	When not using a regulator	2.7 to 3.6			V
		When using a regulator	4.5 to 5.5			V
Operating temperature	T_{OP}	—	-20 to +85			°C
Master clock frequency	f_{OSC}	—	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	
Crystal oscillation external capacity	Cd,Cg	—	15	30	45	pF

ELECTRICAL CHARACTERISTICS

DC Characteristics (3 V)

DV_{DD} = AV_{DD} = SPV_{DD} = 2.7 to 3.6 V, DGND = AGND = SPGND = 0 V, Ta = -20 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	0.86×V_{DD}	—		V
"L" input voltage	V_{IL}	—	—	—	0.14× V_{DD}	V
"H" output voltage1	V_{OH1}	I_{OH} = –1mA	V_{DD} –0.4	—	—	V
"H" output voltage2 (Note 1)	V_{OH2}	I_{OH} = –100μA	V_{DD} –0.4	—	—	V
"L" output voltage1	V_{OL1}	I_{OL} = 4 mA	—	—	0.4	V
"L" output voltage2 (Note 1)	V_{OL2}	I_{OL} = 100 μA	—	—	0.4	V
"H" input current 1	I_{IH1}	V_{IH} = DV_{DD}	—	—	10	μA
"H" input current 2 (Note 2)	I_{IH2}	V_{IH} = DV_{DD}	0.3	2.0	15	μA
"H" input current 3 (Note 3)	I_{IH3}	V_{IH} = DV_{DD}	5	40	130	μA
"L" input current 1	I_{IL1}	V_{IL} = DGND	–10	—	—	μA
"L" input current 2 (Note 2)	I_{IL2}	V_{IL} = DGND	–15	–2.0	–0.3	μA
"L" input current3 (Note 3)	I_{IL3}	V_{IL} = DGND	–10	—	—	μA
Playback Operating current consumption 1	I_{DD}	f_{OSC} = 4.096 MHz at no load Read Operation	—	—	10	mA
Standby current consumption	I_{DDS}	Ta = -20 to +85°C	—	1	20	μA

Notes: 1.Applies to $\overline{XT}$pin.
2.Applies to XT pin.
3.Applies to TEST and SCAN pins.

DC Characteristics (5 V)

DV_{DD} = AV_{DD} = SPV_{DD} = 4.5 to 5.5 V, DGND = AGND = SPGND = 0 V, Ta = -20 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	$0.8 \times V_{DD}$	—		V
"L" input voltage	V_{IL}	—	—	—	$0.2 \times V_{DD}$	V
"H" output voltage1	V_{OH1}	I_{OH} = –1mA	V_{DD} –0.4	—	—	V
"H" output voltage2 (Note 1)	V_{OH2}	I_{OH} = –100μA	V_{DD} –0.4	—	—	V
"L" output voltage1	V_{OL1}	I_{OL} = 4 mA	—	—	0.4	V
"L" output voltage2 (Note 1)	V_{OL2}	I_{OL} = 100 μA	—	—	0.4	V
"H" input current 1	I_{IH1}	V_{IH} = DV_{DD}	—	—	10	μA
"H" input current 2 (Note 2)	I_{IH2}	V_{IH} = DV_{DD}	0.8	5.0	20	μA
"H" input current 3 (Note 3)	I_{IH3}	V_{IH} = DV_{DD}	30	140	350	μA
"L" input current 1	I_{IL1}	V_{IL} = DGND	–10	—	—	μA
"L" input current 2 (Note 2)	I_{IL2}	V_{IL} = DGND	–20	–5.0	–0.8	μA
"L" input current3 (Note 3)	I_{IL3}	V_{IL} = DGND	–10	—	—	μA
Playback Operating current consumption 1	I_{DD}	f_{OSC} = 4.096 MHz at no load Read Operation	—	—	10	mA
Standby current consumption	I_{DDS}	Ta =-20 to +85°C	—	1	30	μA

Notes: 1.Applies to $\overline{XT}$pin.
2.Applies to XT pin.
3.Applies to TEST and SCAN pins.

Analog Section Characteristics (3 V)

DV_{DD} = AV_{DD} = SPV_{DD} = 2.7 to 3.6 V, DGND = AGND = SPGND = 0 V, Ta = -20 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AOUT output load resistance	R_{LA}	When 1 / 2AV_{DD} output	5	—	—	kΩ
AOUT output voltage range	V_{AO}	No output load	0.1	—	2.0	V
SPIN Input resistance	R_{SPI}	—	1	—	—	MΩ
SPP pull-down resistor	R_{SPP}	When power-down state	15	—	65	kΩ
SPM pull-down resistor	R_{SPM}	When power-down state	1	—	20	kΩ
SPM, SPP output load resistance	R_{LSP}	—	8	—	—	Ω
Speaker amplifier output electric power	P_{SPO}	SPV_{DD} = 3.3V,fin = 1kHz, R_{SPO} = 8Ω,THD≥10%	80	100	—	mW
SPM-SPP output offset voltage at non-signal	V_{OF}	SPIN – SPM profit = 0dB When 8Ω load	-50	—	50	mV
SG output voltage	V_{SG}	—	0.48×AV_{DD}	0.5×AV_{DD}	0.52×AV_{DD}	V
SG output resistance	R_{SG}	—	12	20	28	kΩ

Analog Section Characteristics (5 V)

DV_{DD} = AV_{DD} = SPV_{DD} = 4.5 to 5.5 V, DGND = AGND = SPGND = 0 V, Ta = -20 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AOUT output load resistance	R_{LA}	When 1 / 2AV_{DD} output	50	—	—	kΩ
AOUT output voltage range	V_{AO}	No output load	0.1	—	2.0	V
SPIN Input resistance	R_{SPI}	—	1	—	—	MΩ
SPP pull-down resistor	R_{SPP}	When power-down state	15	—	65	kΩ
SPM pull-down resistor	R_{SPM}	When power-down state	1	—	20	kΩ
SPM, SPP output load resistance	R_{LSP}	—	8	—	—	Ω
Speaker amplifier output electric power	P_{SPO}	SPV_{DD} = 5.0V,fin = 1kHz, R_{SPO} = 8Ω,THD≥10%	250	300	—	mW
SPM-SPP output offset voltage at non-signal	V_{OF}	SPIN – SPM profit = 0dB When 8Ω load	-50	—	50	mV
SG output voltage	V_{SG}	—	0.48×AV_{DD}	0.5×AV_{DD}	0.52×AV_{DD}	V
SG output resistance	R_{SG}	—	12	20	28	kΩ

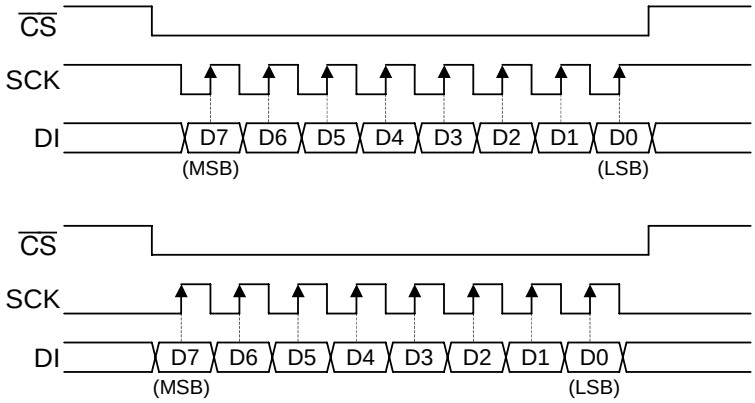
FUNCTIONAL DESCRIPTION

Serial Interface

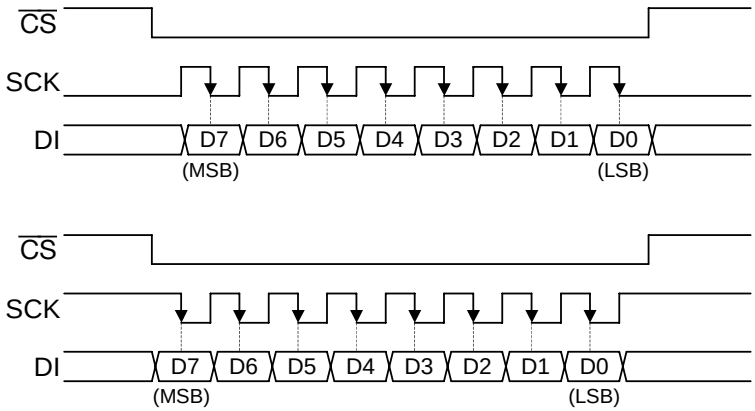
The serial interface inputs various commands and data by CS, SCK, and DI pin.
The micro-computer interface becomes effective when CS pin is set to “L” level.
To input the commands and data, “L” level is input to CS pins followed by, from MSB, to DI pin in synchronization with the input clock signal at SCK pin. Data at DI pin is captured inside the device on the rising or falling edge of the clock at SCK pin. And the command is executed on the rising or falling edge of eight clocks of a SCK pin.
The selection of rising/falling edge of SCK clock is determined by the DIPH pin. If the DIPH pin is at “L” level, the DI pin data is captured inside the device on the rising edge of SCK clock. Conversely, if DIPH pin is at “H” level, then the DI pin data is captured on the falling edge of SCK clock.
Even if it makes CS pin “L” level fixation, the input of command data is possible. However, when pulses other than specification are inputted into a SCK pin, LSI does not operate normally. The count of the number of clocks of a SCK pin returns to an initial state by making CS pin into “H” level.

Command and Data Input Timings

- SCK Rising Edge Operation (DIPH pin is at “L” level)



- SCK falling Edge Operation (DIPH pin is at “H” level)



Commands List

Each command is 1-byte (8 bits) input. PLAY and MUON only are 2 bytes input.

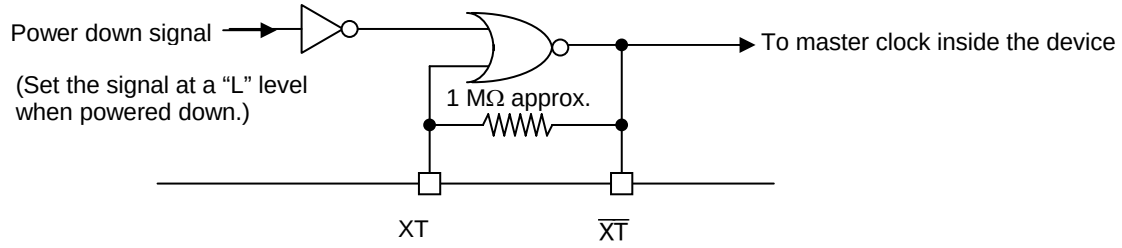
Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
PUP1	0	0	0	0	–	–	–	–	Instantly shifts the power down device to the command standby state.
PUP2	0	0	0	1	–	–	–	–	Suppresses pop noise and shifts the power down device to the command standby state.
PDWN1	0	0	1	0	–	–	–	–	Instantly shifts the device from the command standby state to the power down state.
PDWN2	0	0	1	1	–	–	–	–	Suppresses pop noise and shifts the device from the command standby state to power down state.
PLAY	0	1	0	0	–	–	–	–	Inputs the phrase, and then starts the playback.
	F7	F6	F5	F4	F3	F2	F1	F0	
STOP	0	1	1	0	–	–	–	–	ends the voice.
MUON	0	1	1	1	–	–	–	–	Inserts silence time and then inserts silence.
	M7	M6	M5	M4	M3	M2	M1	M0	
SLOOP	1	0	0	0	–	–	–	–	Repeats the playback mode setting command. Effective only for the channel being used for playback.
CLOOP	1	0	0	1	–	–	–	–	Repeat playback mode releasing command. Inputting the STOP command releases repeat playback mode automatically.
VOL	1	0	1	0	V3	V2	V1	V0	Sets the volume of playback.
SPKR	1	0	1	1	–	–	OP	PD	Power down control commands of speaker amplifier.

F7 to F0: Phrase address
M7 to M0:Silence time length
V3 to V0: Sound volume
PD power down control of speaker amplifier
OP pop noise control of speaker amplifier

Power Down Function

In power down state, the power down function in the device stops the internal operation and oscillation, and minimizes the static Idd.
When an external clock is in use, input "L" level to the XT pin, so that current does not flow into the oscillation circuit.

Figure below shows the equivalent circuit of $\overline{XT}$ and XT pins.



Initial state at the time of reset input and power down state

Each output pin state is shown.

Digital output pin	state	Analog output pin	state
NCR	"H" level	REGO	DGND level
$\overline{BUSY}$	"H" level	VBG	AGND level
RAO	"L" level	SG	AGND level
		AOUT	AGND level
		SPM	SPGND level
		SPP	SPGND level

Voice Synthesis Algorithm

The ML2250 family contains 5 algorithm types to match the characteristic of playback voice: 4-bit ADPCM 2 algorithm, 8-bit PCM algorithm, 8-bit non-linear PCM algorithm, and 16-bit PCM algorithm.
Key feature of each algorithm is described in the table below.

Voice synthesis algorithm	Applied waveform	Feature
Oki 4-bit ADPCM2	Normal voice waveform	Oki's specific speech synthesis algorithm of improved waveform follow-up with improved 4-bit ADPCM.
Oki 8-bit Nonlinear PCM	High-frequency components inclusive sound effect etc.	Algorithm which plays back mid-range of waveform as 10-bit equivalent voice quality.
8-bit PCM	High-frequency components inclusive sound effect etc.	Normal 8-bit PCM algorithm
16-bit PCM	High-frequency components inclusive sound effect etc.	Normal 16-bit PCM algorithm

Memory Allocation and Creating Voice Data

The ROM is partitioned into 4 data areas: voice (i.e., phrase) control area, test area, voice area, and phrase control table area.
The voice control area manages the ROM's voice data. It controls the start/end addresses of voice data, usage/not usage of the phrase control table function and so on. The voice control area stores voice control data for 256 phrases.
The test area stores the data for testing.
The voice area stores the actual waveform data.
The phrase control table area stores data for effective use of voice data. As for the details, please refer to the Phrase Control Table Function.
There is no phrase control table area if the phrase control table is not used.

The ROM data is created using a development tool.

ROM Addresses (ML2216)

0x00000 0x007FF	Voice control area (16 Kbit Fixed)
0x00800 0x00807	Test area
0x00808 max: 0xFFFFF	Voice area
max: 0xFFFFF	Phrase Control Table area Depends on creation of ROM data.

Playback Time and Memory Capacity

The playback time depends upon the memory capacity, sampling frequency, and playback method.
The equation showing the relationship is given below.

$$\text{Playback time [sec]} = \frac{1{,}024 \times (\text{Memory capacity} - 16)\ \text{(bit)}}{\text{Sampling frequency (kHz)} \times \text{Bit length}}$$

(Bit length is ADPCM, ADPCM 2 = 4 bits; PCM = 8 bits.)

Example: Let the sampling frequency be 16 kHz and 4-bit ADPCM algorithm. If one 8 Mbits ROM is used, then the playback time is obtained as follows:

$$\text{Playback time} = \frac{1{,}024 \times (8 \times 1{,}024 - 16)\ \text{(bit)}}{16\ \text{(kHz)} \times 4\ \text{(bit)}} \cong 131\ \text{(sec)}$$

The above equation gives the playback time when the phrase control table function is not used.

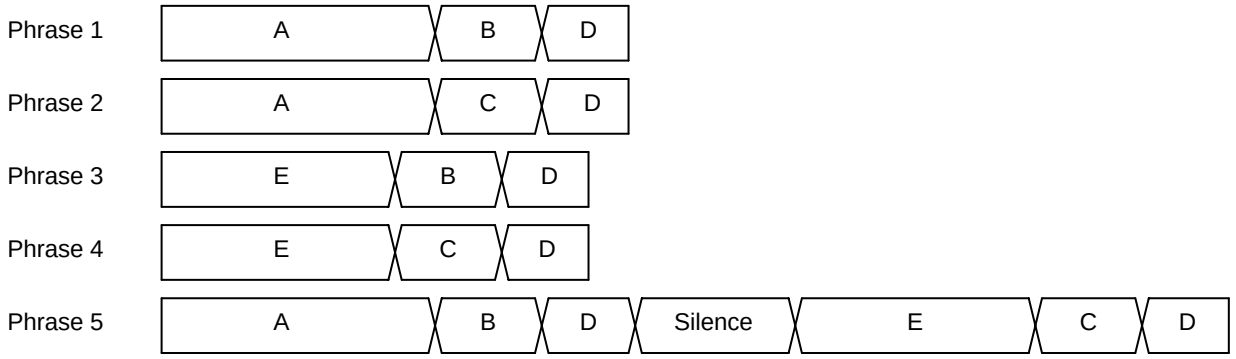
Phrase Control Table Function

The phrase control table function makes it possible to play back multiple phrases in succession. The following functions are set using the phrase control table function:

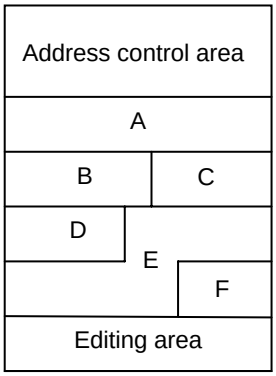
- Continuous playback: There is no limit to the number of times a continuous playback can be specified. It depends on the memory capacity only.
- Silence insertion function: 20 to 1024 ms

Using the phrase control table function enables to effectively use the memory capacity of voice ROM.
Below is an example of the ROM configuration in the case of using the phrase control table function.

Example 1: Phrases Using the Phrase Control Table Function

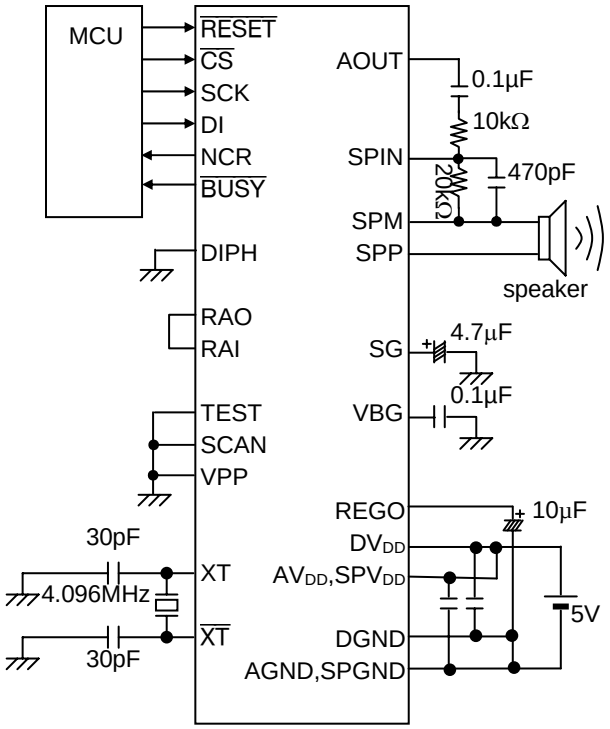


Example 2: Example of ROM Data in case Example 1 Converted to ROM

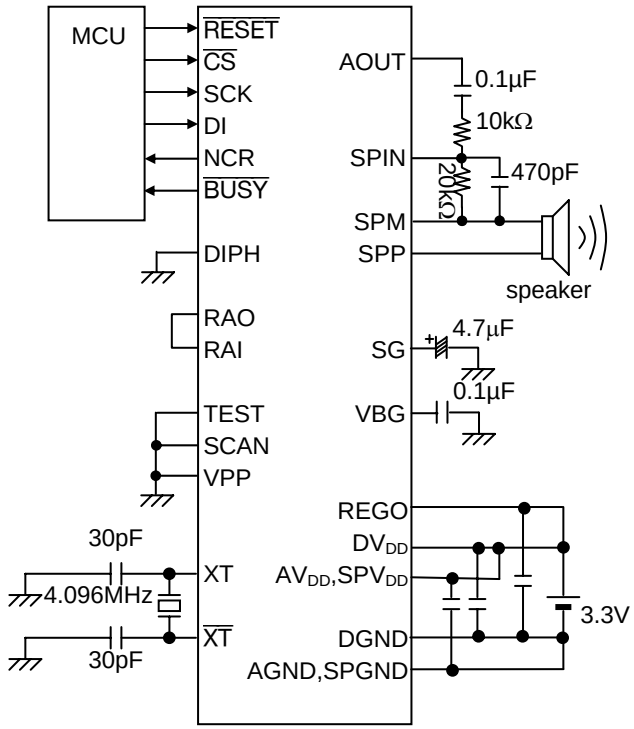


APPLICATION CIRCUIT EXAMPLE (ML2216)

At DV_{DD} = AV_{DD} = SPV_{DD} = 5.0V



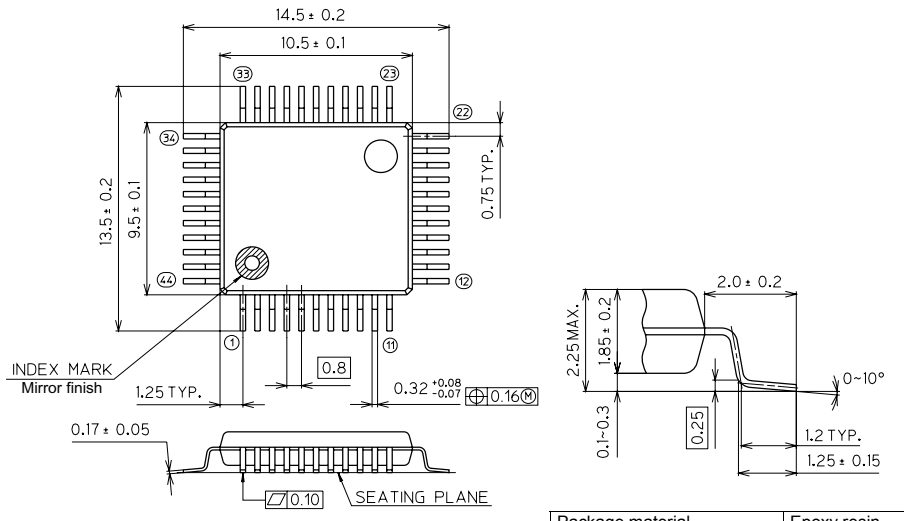
At DV_{DD} = AV_{DD} = SPV_{DD} = 3.0V



PACKAGE DIMENSIONS

(Unit: mm)

QFP44-P-910-0.80-2K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.41 TYP.
Rev. No./Last Revised	4/Nov. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. OKI SEMICONDUCTOR assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

5. Neither indemnity against nor license of a third party's industrial and intellectual property right, etc. is granted by us in connection with the use of the product and/or the information and drawings contained herein. No responsibility is assumed by us for any infringement of a third party's right which may result from the use thereof.

6. The products listed in this document are intended for use in general electronics equipment for commercial applications (e.g., office automation, communication equipment, measurement equipment, consumer electronics, etc.). These products are not, unless specifically authorized by OKI SEMICONDUCTOR authorized for use in any system or application that requires special or enhanced quality and reliability characteristics nor in any system or application where the failure of such system or application may result in the loss or damage of property, or death or injury to humans.
   Such applications include, but are not limited to, traffic and automotive equipment, safety devices, aerospace equipment, nuclear power control, medical equipment, and life-support systems.

7. Certain products in this document may need government approval before they can be exported to particular countries. The purchaser assumes the responsibility of determining the legality of export of these products and will take appropriate and necessary steps at their own expense for these.

8. No part of the contents contained herein may be reprinted or reproduced without our prior permission.