3.3 Volt Laser Driver IC for Applications to 3 Gbps

CX02066

FEATURES

- High speed operation; suitable for applications to 3 Gbps.
  Typical rise/fall times <90 ps.
- DC or AC coupled modulation drive.
- Differential data and clock inputs to minimize pattern dependent jitter.
- Independently Programmable Laser Bias and Modulation currents.
  Bias current to 100 mA and modulation current to 85 mA at V_{CC}=3.3V
- Automatic Laser Power Control, with programmable Temperature Compensation and 'Slow-Start'.
- Bias and modulation current monitor
- Operates with +3.3 Volt supply
- Functionally compatible with MAX 3869
- The CX02066 is available in die form, or packages (BCC+24 or TQFP32)

APPLICATIONS

- Short reach SONET/SDH
- Metro SONET/SDH
- Datacomms Modules

DESCRIPTION

The CX02066 is a highly integrated, programmable laser driver intended for SONET/SDH applications with FEC to 3 Gbps. Using differential PECL data and clock inputs, the CX02066 supplies the bias and modulation current for driving an edge-emitting laser. The modulation output can be DC-coupled to the laser diode, giving a significant power saving over AC-coupled operation.

The CX02066 includes automatic power control to maintain a constant average laser output power over temperature and life. In addition, the modulation current is temperature compensated to minimize variation in extinction ratio over temperature.

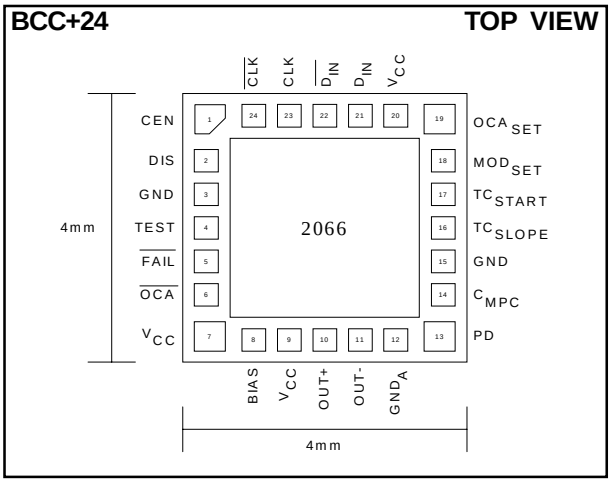
Output flags indicate laser end of life as well as failure of the APC circuitry to maintain average output power.

ORDERING INFORMATION

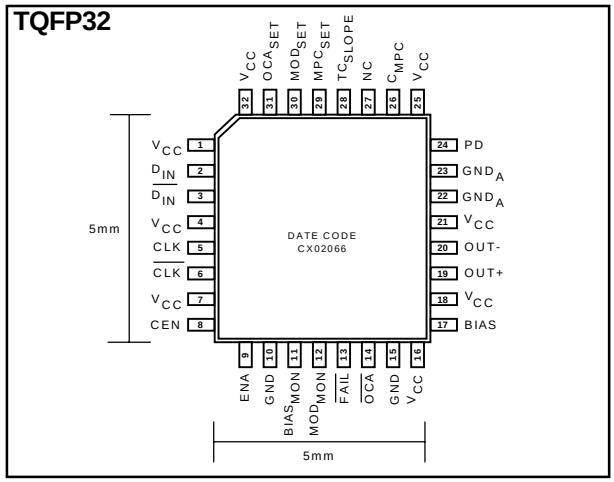
Part Number	Pin Package
CX02066DIEWP	Waffle Pack
CX02066WAFER	Expanded Whole 8" Wafer on a 10" Grip Ring
CX02066B24	BCC+24
CX02066TQ32	TQFP32

CONNECTIONS

BCC+24 **TOP VIEW**



TQFP32



PIN DESCRIPTION - BCC+24

Pin No BCC+24	Name	Function
1	CEN	Clock Enable Input (TTL/CMOS). Set HIGH or Not Connected to use CLK inputs, LOW when not using CLK inputs.
2	DIS	Bias and Modulation Output Disable (TTL/CMOS). LOW for normal operation.
3, 15	GND	Ground
4	TEST	Factory Test Pin - tie to V_{CC}
5	$\overline{FAIL}$	Mean Power Control Failure indicator (TTL/CMOS). Goes low when control loop is no longer able to maintain constant current at PD.
6	$\overline{OCA}$	Over-Current Alarm (TTL/CMOS). Goes low when I_{BIAS} exceeds the preset bias current limit
8	BIAS	Laser bias current output
9, 7, 20	V_{CC}	Power supply
10	OUT+	Positive modulation current output. Sinks current when D_{IN} is HIGH.
11	OUT-	Negative modulation current output. Sinks current when $\overline{D_{IN}}$ is HIGH.
12	GND_A	Ground for output stage.(inductor to ground)
13	PD	Monitor photodiode input. This input is connected to the monitor photodiode anode for automatic power control.
14	C_{MPC}	Mean power control dominant pole capacitor
16	TC_{SLOPE}	Connecting a resistor between this pin and ground sets the temperature coefficient of I_{MODSET} (using the internal IC temperature).
17	TC_{START}	Secondary temperature coefficient of I_{MOD}. A resistor on this pin to ground sets the temperature at which the temperature compensation starts.
18	MOD_{SET}	Modulation current set. Connect a resistor between this pin and ground to set.
19	OCA_{SET}	Overcurrent alarm set. Connect a resistor between this pin and ground to set.
21	D_{IN}	Positive Data Input (PECL). Self biased.
22	$\overline{D_{IN}}$	Negative Data Input (PECL). Self biased.
23	CLK	Positive Clock Input (PECL). Self biased. Can leave disconnected if not used.
24	$\overline{CLK}$	Negative Clock Input (PECL). Self biased. Can leave disconnected if not used.

PIN DESCRIPTION - TQFP 32

Pin No TQFP32	Name	Function
1	V_{CC}	Power Supply
2	D_{IN}	Positive Data Input (PECL).Self biased.
3	$\overline{D_{IN}}$	Negative Data Input (PECL).Self biased.
4, 7, 16, 18, 21, 25, 32	V_{CC}	Power Supply
5	CLK	Positive Clock Input (PECL). Self biased. Can leave disconnected if not used.
6	$\overline{CLK}$	Negative Clock Input (PECL). Self biased. Can leave disconnected if not used.
8	CEN	Clock Enable Input (TTL/CMOS). Set HIGH or not connected to use CLK inputs, LOW when not using CLK inputs.
9	ENA	Bias and modulation Output Enable (TTL/CMOS). HIGH for normal operation.
10, 15	GND	Ground
11	$BIAS_{MON}$	Bias monitor and temperature-dependent bias current limit. Connect a resistor between this pin and V_{CC} to monitor.
12	MOD_{MON}	Bias monitor and temperature-dependent bias current limit. Connect a resistor between this pin and V_{CC} to monitor.
13	$\overline{FAIL}$	Mean Power Control Failure indicator (TTL/CMOS). Goes LOW when control loop is no longer able to maintain constant current at I_{PIN}.
14	$\overline{OCA}$	Over-Current Alarm (TTL/CMOS). Goes LOW when I_{BIAS} exceeds the preset bias current limit
17	BIAS	Laser bias current output
19	OUT+	Positive modulation current output. Sinks current when D_{IN} is HIGH.
20	OUT-	Negative modulation current output. Sinks current when $\overline{D_{IN}}$ is HIGH.

PIN DESCRIPTION - TQFP 32

Pin No TQFP32	Name	Function
22, 23	GND_A	Ground for output stage (inductor to ground)
24	PD	Monitor photodiode input. This input is connected to the monitor photodiode anode for automatic power control.
26	C_{MPC}	Mean power control dominant pole capacitor
27	NC	No connect and may be grounded for compatibility with MAX3869
28	TC_{SLOPE}	Connecting a resistor between this pin and ground sets the temperature coefficient of I_{MODSET} (using the internal IC temperature).
29	MPC_{SET}	A resistor between this pin and ground sets the mean optical power
30	MOD_{SET}	Modulation current set. Connect a resistor between this pin and ground to set.
31	OCA_{SET}	Overcurrent alarm set. Connect a resistor between this pin and ground to set.

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Power supply (V_{CC}-GND)	-0.5 to +6.0	V
Operating ambient	-40 to +85	°C
Storage Temperature	-65 to +150	°C
Maximum laser bias current	120	mA
Maximum laser moduation current (through OUT+/OUT2+, OUT-/OUT2-)	100	mA

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

RECOMMENDED OPERATING CONDITIONS

Parameter	Rating	Units
Power supply (V_{CC} -GND)	3.3 ± 10%	V
Junction Temperature (die)	-40 to +120	°C
Operating ambient	-40 to +85	°C

AC CHARACTERISTICS

Parameter	Conditions	Min.	Typ.	Max.	Units
Differential input voltage	$=2x(D_{IN}+$ HIGH $-D_{IN}+_{LOW})$ (clock inputs follow same relationship)	300	-	1860	mV
Modulation current range		2.5	-	85	mA
Modulation current with output disabled	DIS=HIGH	-	-	300	µA
Programmable range for modulation current temperature coefficient	Adjustable	500	-	10^4	ppm/°C
Programmable temperature at which modualtion current TC compensation enables	Programed by choice of R_{TCSET}	20	-	60	°C
Modulation output rise time Modulation output fall time	20% to 80% into 25Ω. 20% to 80% into 25Ω.	-	-	100 116	ps
Overshoot of modulation output current	Into 25Ω load	-10	-	+10	%
Modulation output pulse width distortion	Measured using alternating 1-0 pattern	-	-	20	ps
Modulation output random jitter	rms. 12kHz to 20MHz	-	-	4	mUI
Total output jitter (data input latch enabled)	Peak-to-Peak.Measured into 25Ω load using 1867 MHz Bessel filter: 2^{23} -1 PRBS at 2.488Gbps; using clock inputs (includes PWD, random and deterministic)	-	-	42	ps

(V_{CC}=+3.3V± 5%, T_A=-40°C to +85°C, unless otherwise noted)

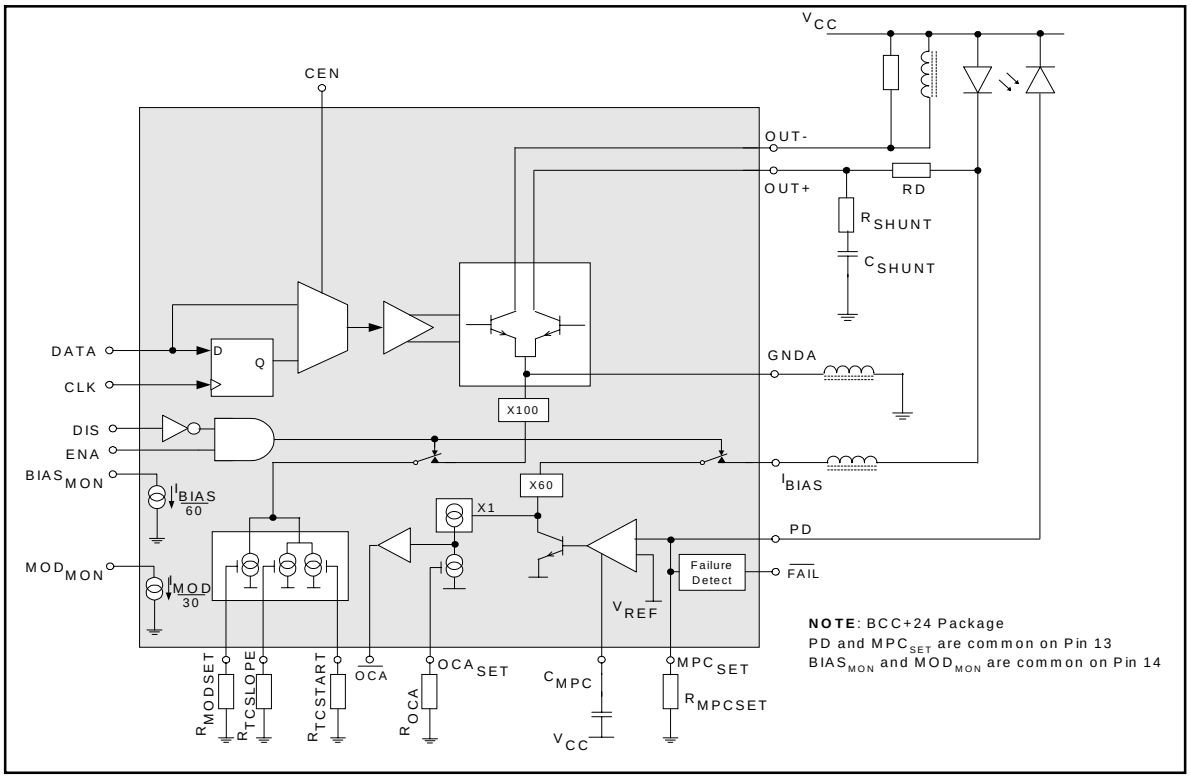
DC CHARACTERISTICS

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Current	I_{BIAS}=50mA I_{MOD}=50mA Excluding IBIAS and IMOD	-	57	-	mA
Supply Current	I_{BIAS}=100mA I_{MOD}=85mA Excluding IBIAS and IMOD	-	70	75	mA
Bias current adjust range	Limited by I_{REF} across temperature range	2	-	100	mA
Bias current with output disabled	Tx_Disable=high	-	-	300	µA
Maximum bias current limit	TA=+85°C (adjustable)	100(1)	-	-	mA
Change in I_{REF} over temperature	Adjustable	200(1)	-	500	µA/°C
Monitor diode reverse bias voltage		2	-	-	V
Monitor diode current adjustment range		10	-	1500	µA
TTL/CMOS input HIGH voltage (CEN, DIS)		2.0	-	-	V
TTL/CMOS input LOW voltage (CEN, DIS)		-	-	0.8	V
CMOS output HIGH voltage (FAIL, OCA)		2.4	-	-	V
CMOS output LOW voltage (FAIL, OCA)		-	-	0.4	V
Differential input Impedance	Data and Clock inputs	2.5	-	-	kΩ
Common-mode input voltage		V_{CC}- 1.38	-	V_{CC}- $\frac{V_{IN(Diff)}}{4}$	V
Self-Biased common mode input voltage	Data and clock inputs	V_{CC}- 1.38	-	V_{CC}- 0.47	V

(V_{CC}=+3.3V$\pm$ 5%, T_A=-40°C to +85°C, unless otherwise noted)

(1) Default value.

FUNCTIONAL DIAGRAM



FUNCTIONAL DESCRIPTION

Overview

The CX02066 laser driver consists of a high-speed modulation driver and a laser bias generator with mean power control (MPC). It is optimized for high speed, low power operation at 3.3V supply. To minimize the pattern-dependent jitter of the input signal, the device accepts an input clock signal for data retiming. This feature can be enabled using the external CEN pin.

Modulator

The modulator output stage is designed to drive up to 85mA in either AC-coupled or DC-coupled mode. DC-coupled performance depends on the laser used.

The CX02066 modulation output is optimized for driving a 25Ω load; the minimum required voltage at OUT+ and OUT- is 0.6V. To interface with the laser diode, a matching resistor (RD) is required for impedance matching. An RC shunt network is necessary to compensate for the laser diode parasitic inductance, thereby improving the optical eye.

Typical values are R_{SHUNT} = 51Ω, C_{SHUNT} = 3.3pF. These values will need to be optomised for the specfic laser being used.

Any capacitive loading at the cathode of a laser diode will degrade the optical output performance. An inductor is used to isolate the BIAS pin from the laser cathode.

Mean Power Control

To maintain constant average optical power, the CX02066 incorporates a control loop to compensate for the changes in laser threshold current over temperature and lifetime. A monitor photodiode mounted in the laser package is used to convert the optical power into a photocurrent. The MPC loop adjusts the laser bias current so that the voltage at PD is matched to an on-chip reference voltage. The external resistor (R_{MPCSET}) sets the optical power.

$R_{MPCSET} = 1.28/I_{PIN}$

I_{PIN} is the mean current from the monitor photodiode at the required mean laser power level (see laster datasheet).The time constant of the loop is determined by C_{MPC}. In some applications the internal capacitance on C_{MPC} may be sufficient and an external C_{MPC} will not be required.

FUNCTIONAL DESCRIPTION

Safety Logic

Safety logic is provided in order to limit the maximum bias current. The bias current at which the safety logic trips is set by an external resistor to ground (R_{OCA}) from the OCA_{SET} pin. When the bias current limit is reached alarm flag OCA is asserted LOW. A loop failure alarm is also provided to detect when the bias current can no longer be adjusted to achieve the desired average optical power.

Data Input Latch

To minimize input data pattern-dependent jitter, a differential clock signal can be connected to the data input latch. If CEN is HIGH, the input data is retimed by the rising edge of CLK+. If CEN is LOW, the input data is directly connected to the output stage. If CEN is left floading it will be pulled HIGH by the internal circuitry. When this latch function is not used, connect CLK+ to V_{CC} and leave CLK- unconnected.

Enable Control

The CX02066 incorporates a dual laser driver enable function. When ENA is LOW or DIS is HIGH, both the bias and modulation currents are off. Only DIS is available on the BCC package.

Current Monitors

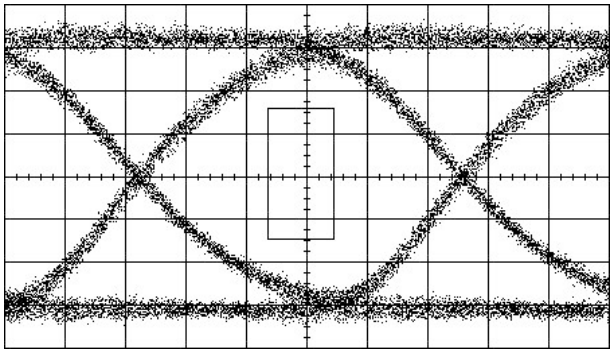
The CX02066 features bias and modulation current monitor outputs. The BIASMON output sinks a current equal to nominally 1/55 of the laser bias current (IBIAS). The MODMON output sinks a current equal to nominally 1/55 of the laser peak to peak modulation current (IMOD). BIASMON and MODMON should be connected through a pull-up resistor to VCC. Choose a pull-up resistor value that ensures a voltage at BIASMON greater than VCC - 1.6V and a voltage at MODMON greater than VCC - 1.0V. These pins should be tied to VCC if not used.

Slow-Start

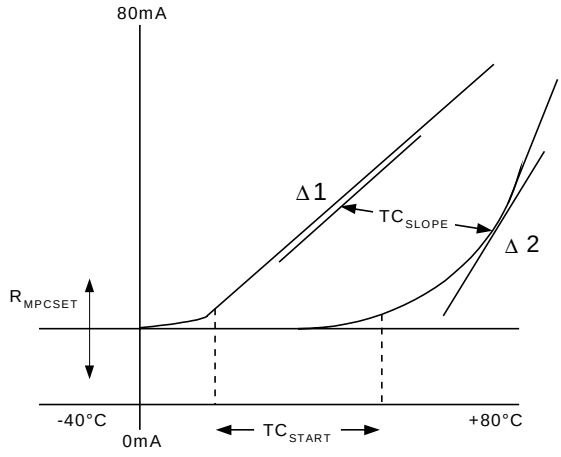
For laser safety and reliability, the CX02066 incorporates a slow-start circuit that provides a delay of approximately 200ns before enabling the laser diode.

TYPICAL EYE DIAGRAM

2.5Gbps Optical Eye @ -3dBm (1.87GHz Filter)

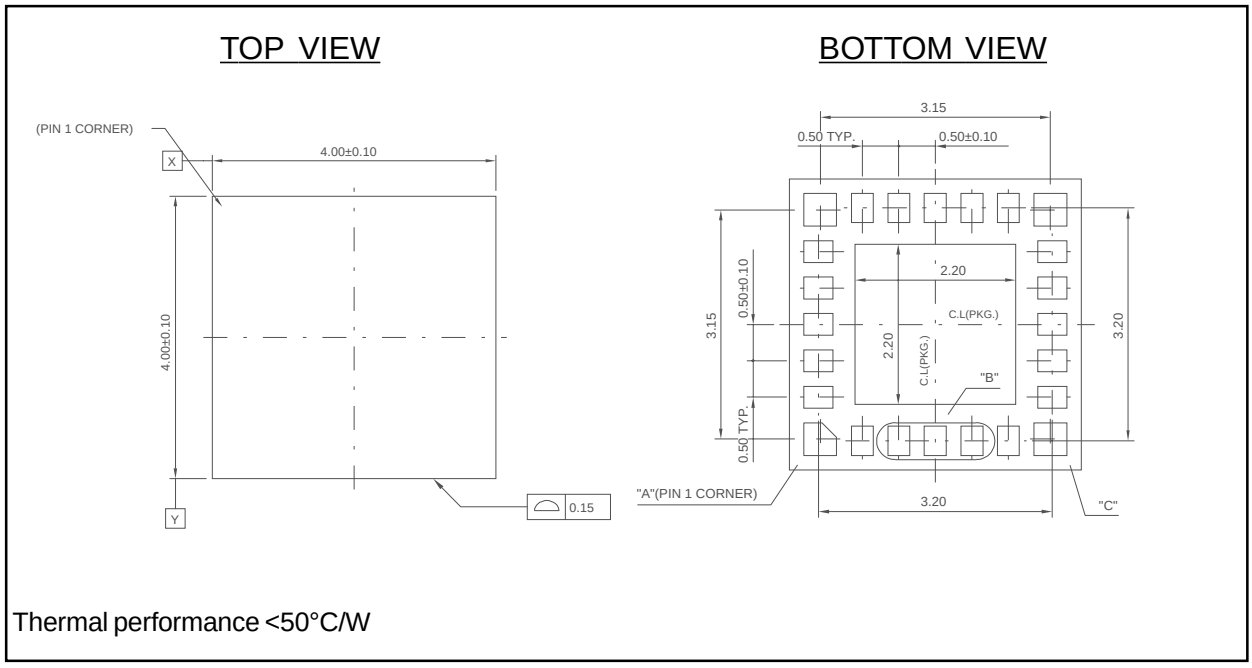


TEMPERATURE COMPENSATION



PACKAGE INFORMATION

Package Outline 24L BCC+

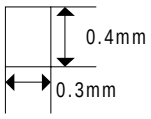


Thermal performance <50°C/W

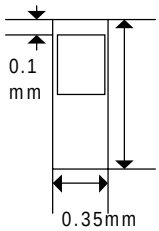
SMT MOUNTING GUIDELINES

BCC Pads

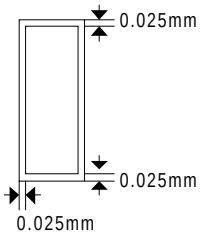
Terminal



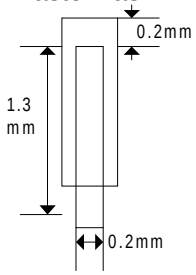
PCB Land



Solder Resist Mask

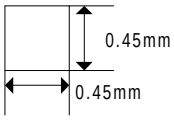


Paste Mask



Corner Pads

Terminal



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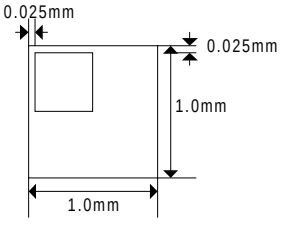
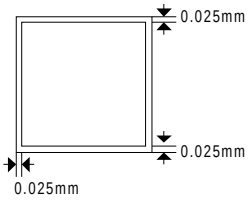


Solder Resist Mask



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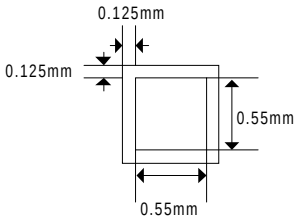
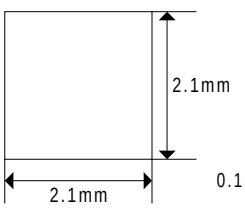
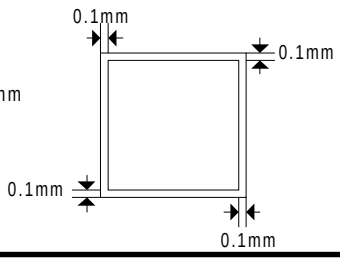


Exposed Central Pad (connected to ground plane)

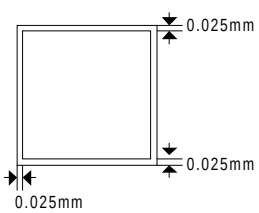
Terminal



PCB Land



Solder Resist Mask



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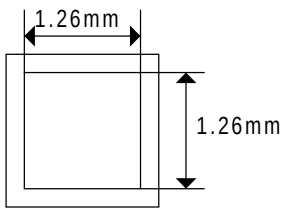
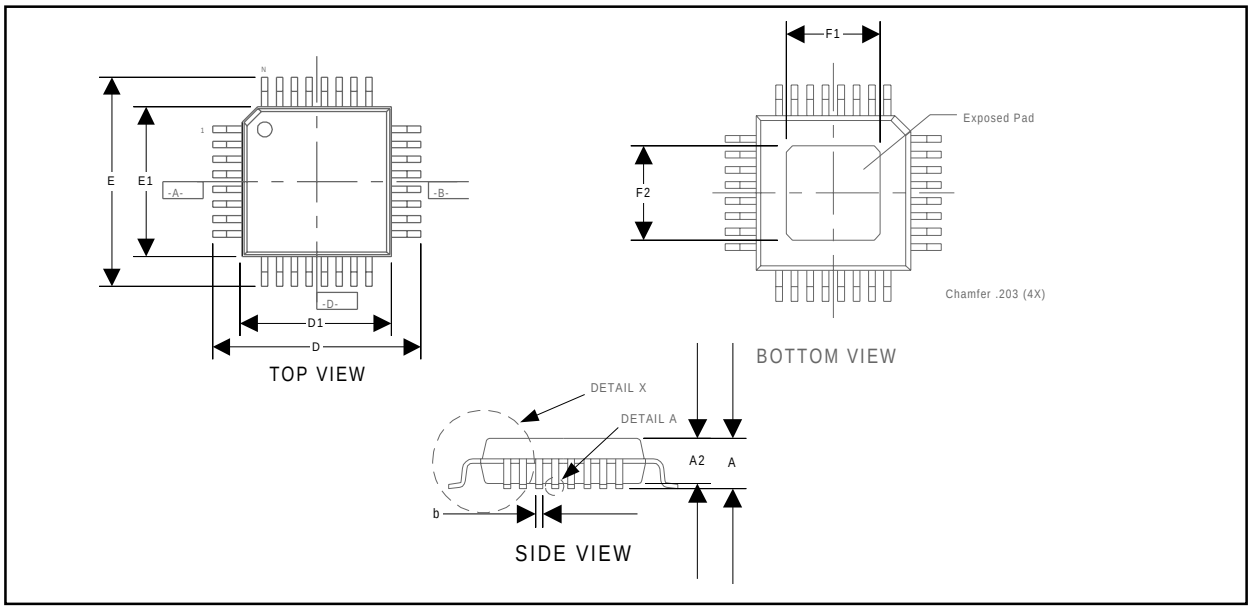


PACKAGE INFORMATION

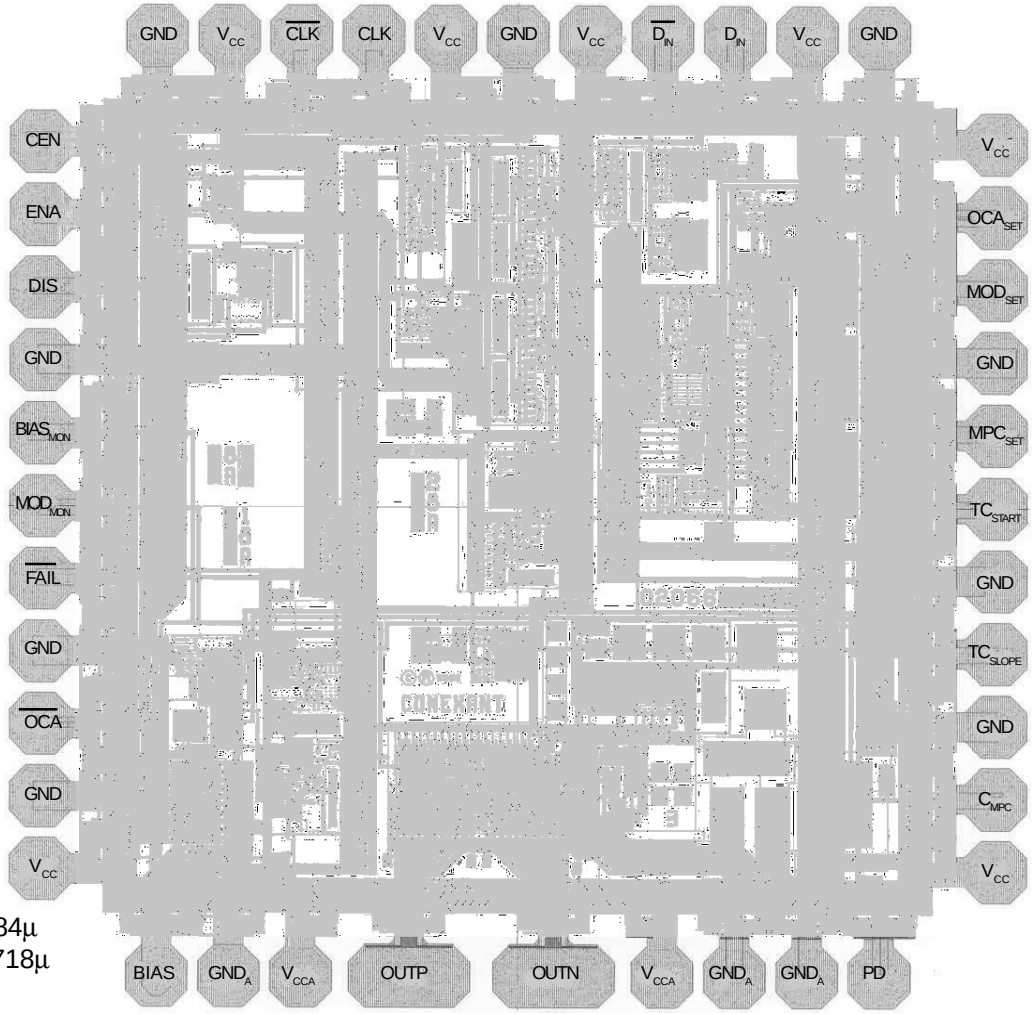
Package Outline TQFP 32



Dimensions	Tolerance	5X5X1.4mm TQFP, + 2.00mm FP		5X5X1.0mm TQFP, + 2.00mm FP
N	Lead Count	32	20	32
A	MAX.	1.60		1.20
A1	± 0.05	0.05		0.05
A2	± 0.05	1.40		1.00
A3	± 0.05	0.6365		0.4365
D	± 0.15	7.00		7.00
D1	± 0.05	5.00		5.00
E	± 0.15	7.00		7.00
E1	± 0.05	5.00		5.00
L	+0.15/-0.10	0.60		0.60
L1	REF.	1.00		1.00
e	TYP.	0.50	0.80	0.50
b	± 0.05	0.22	0.35	0.22
0	***	0° - 7°		0° - 7°
01	± 4°	6°		6°
R	MAX.	0.15		0.15
R1	TYP.	0.15		0.15
aaa	MAX.	0.08		0.08
ccc	MAX.	0.08		0.08
F1	+/- 0.10	3.05		2.67
F2	+/- 0.10	3.05		2.67

BARE DIE INFORMATION

Chip Layout



Dimensions:
Pad opening 84x84µ
Die Size 1790x1718µ

Pad Centres

PIN	X	Y	PIN	X	Y	PIN	X	Y	PIN	X	Y
CEN	-727	550	BIAS	-550	-711	V_{CC}	727	-550	GND	550	711
ENA	-727	440	GND_A	-440	-711	C_{MPC}	727	-440	V_{CC}	440	711
DIS	-727	330	V_{CCA}	-330	-711	GND	727	-330	D_{IN}	330	711
GND	-727	220	*OUTP	-210	-711	TC_{SLOPE}	727	-220	$\overline{D_{IN}}$	220	711
$BIAS_{MON}$	-727	110	*OUTP	-210	-711	GND	727	-110	V_{CC}	110	711
MOD_{MON}	-727	0	*OUTN	100	-711	TC_{START}	727	0	GND	0	711
$\overline{FAIL}$	-727	-110	*OUTN	100	-711	MPC_{SET}	727	110	V_{CC}	-110	711
GND	-727	-220	V_{CCA}	220	-711	GND	727	220	CLK	-220	711
$\overline{OCA}$	-727	-330	GND_A	330	-711	MOD_{SET}	727	330	$\overline{CLK}$	-330	711
GND	-727	-440	GND_A	440	-711	OCA_{SET}	727	440	V_{CC}	-440	711
V_{CC}	-727	-550	PD	550	-711	V_{CC}	727	550	GND	-550	711

* SINGLE PAD/DOUBLE BOND

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