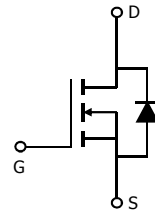


## General Description

The AO4452 is fabricated with SDMOS™ trench technology that combines excellent  $R_{DS(ON)}$  with low gate charge. The result is outstanding efficiency with controlled switching behavior. This universal technology is well suited for PWM, load switching and general purpose applications.

## Features

$V_{DS}$	100V
$I_D$ (at $V_{GS}=10V$ )	8A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 25m $\Omega$
$R_{DS(ON)}$ (at $V_{GS} = 7V$ )	< 31m $\Omega$



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 25$	V
Continuous Drain Current	$I_D$	$T_A=25^\circ\text{C}$	8
		$T_A=70^\circ\text{C}$	6.5
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	57	A
Avalanche Current <sup>C</sup>	$I_{AR}$	28	A
Repetitive avalanche energy $L=0.1\text{mH}$ <sup>C</sup>	$E_{AR}$	39	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_A=25^\circ\text{C}$	3.1
		$T_A=70^\circ\text{C}$	2
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	31	40	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A, D</sup>		Steady-State	59	75
Maximum Junction-to-Lead	$R_{\theta JL}$	16	24	$^\circ\text{C/W}$

Electrical Characteristics (T <sub>J</sub> =25°C unless otherwise noted)						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
B <sub>V</sub> DSS	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	100			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V			10	μA
			T <sub>J</sub> =55°C			
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±25V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2	3.2	4	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	60			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =8A		20.5	25	mΩ
			T <sub>J</sub> =125°C	36	43	
		V <sub>GS</sub> =7V, I <sub>D</sub> =6.5A		25	31	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =8A		23		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.66	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				5	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =50V, f=1MHz	1400	1770	2200	pF
C <sub>oss</sub>	Output Capacitance		115	165	215	pF
C <sub>riss</sub>	Reverse Transfer Capacitance		33	55	80	pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	0.3	0.65	1.0	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, I <sub>D</sub> =8A	14	28	42	nC
Q <sub>gs</sub>	Gate Source Charge		4	9	14	nC
Q <sub>gd</sub>	Gate Drain Charge		6	10	14	nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, R <sub>L</sub> =6Ω, R <sub>GEN</sub> =3Ω		12		ns
t <sub>r</sub>	Turn-On Rise Time			4		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			17		ns
t <sub>f</sub>	Turn-Off Fall Time			5		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =8A, dI/dt=500A/μs	11	16	21	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =8A, dI/dt=500A/μs	42	60	78	nC
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =8A, dI/dt=100A/μs	21	27	33	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =8A, dI/dt=100A/μs	20	28	36	nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25° C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to lead R<sub>θJL</sub> and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C. The SOA curve provides a single pulse rating.

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**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

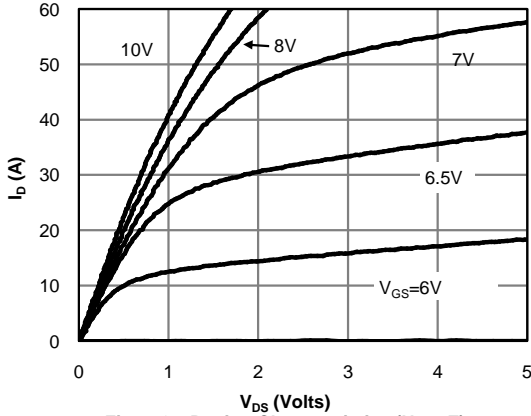


Figure 1: On-Region Characteristics (Note E)

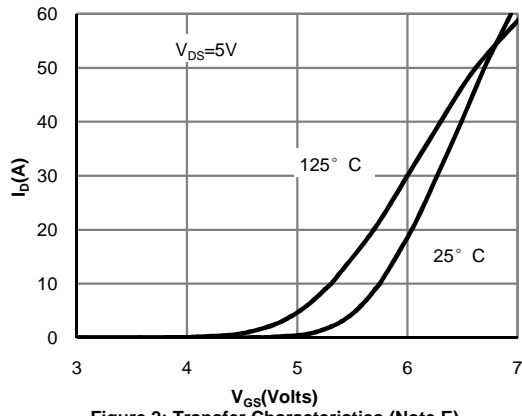


Figure 2: Transfer Characteristics (Note E)

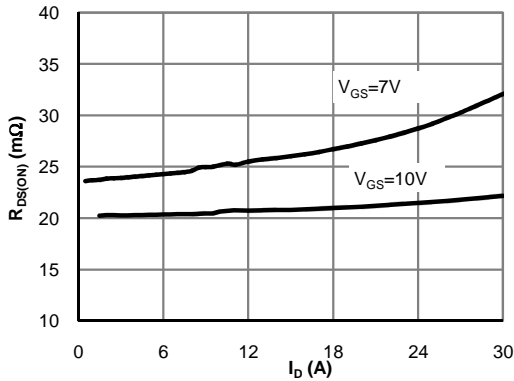


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

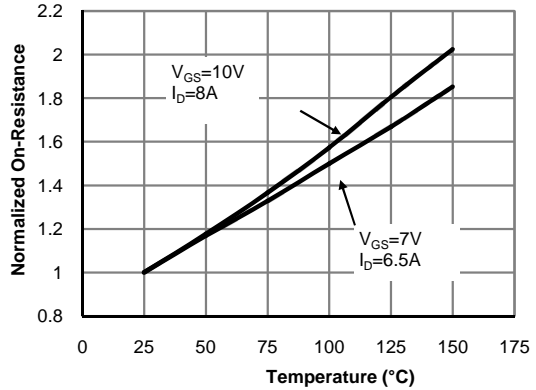


Figure 4: On-Resistance vs. Junction Temperature (Note E)

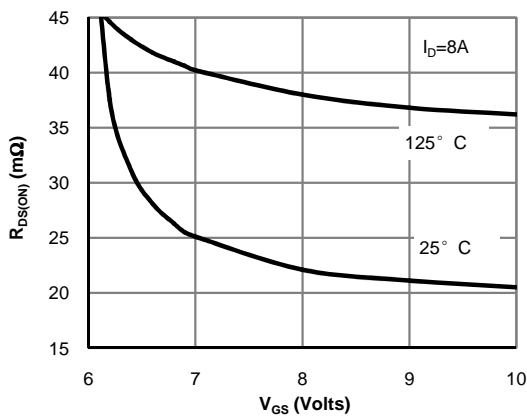


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

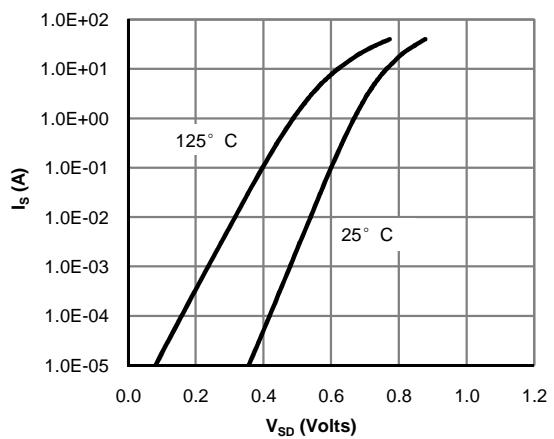
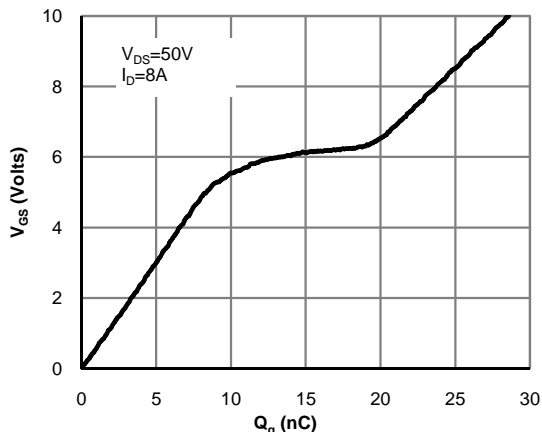
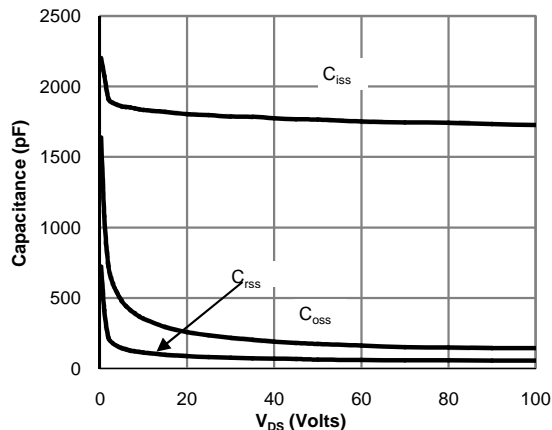


Figure 6: Body-Diode Characteristics (Note E)

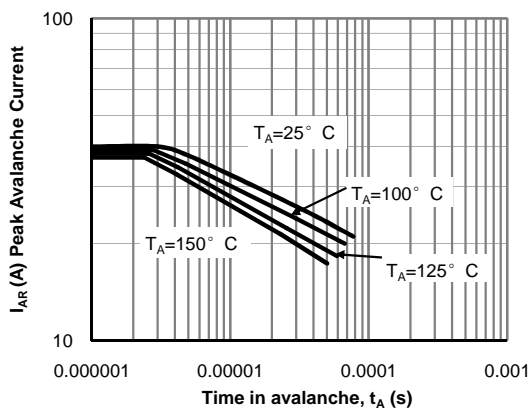
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



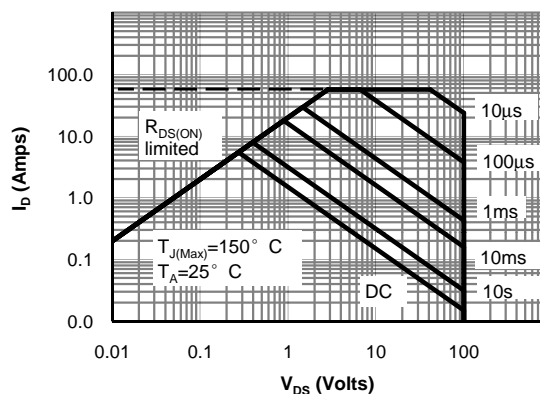
**Figure 7: Gate-Charge Characteristics**



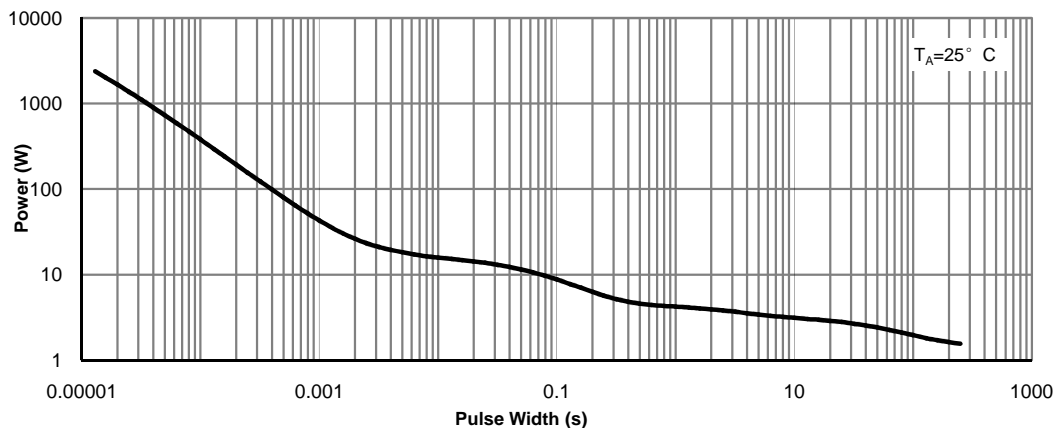
**Figure 8: Capacitance Characteristics**



**Figure 9: Single Pulse Avalanche capability (Note C)**



**Figure 10: Maximum Forward Biased Safe Operating Area (Note F)**



**Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note F)**

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

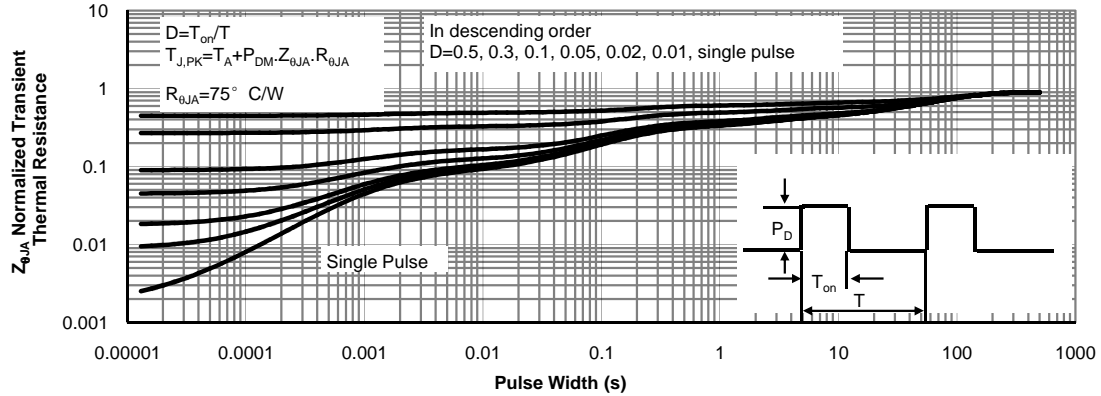


Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)

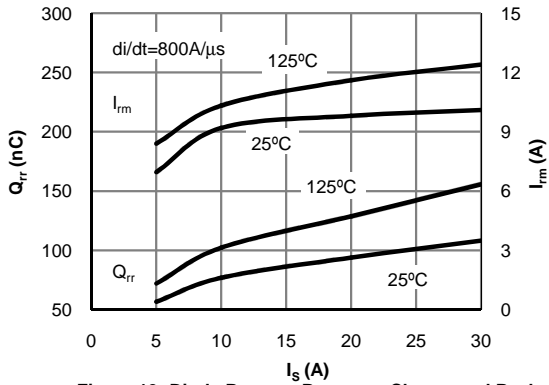


Figure 13: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

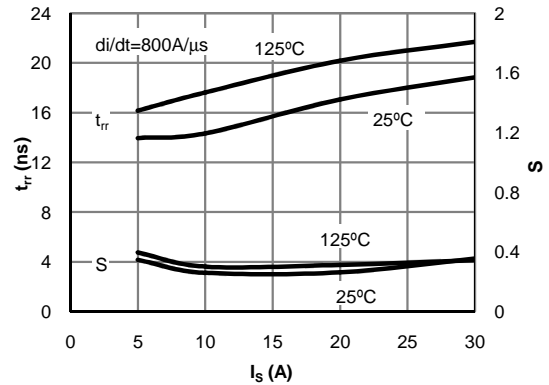


Figure 14: Diode Reverse Recovery Time and Softness Factor vs. Conduction Current

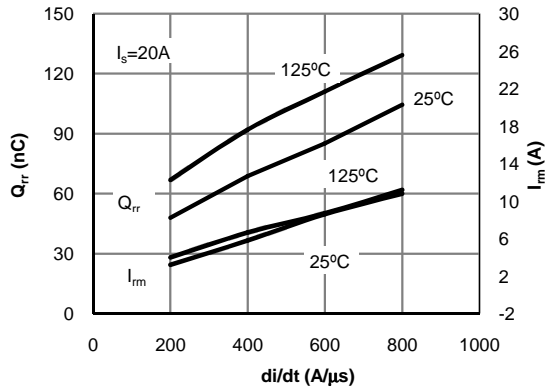


Figure 15: Diode Reverse Recovery Charge and Peak Current vs. di/dt

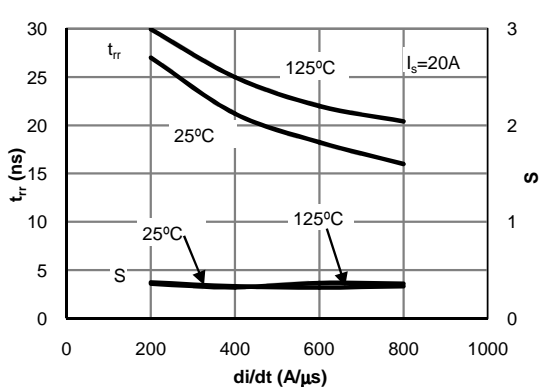
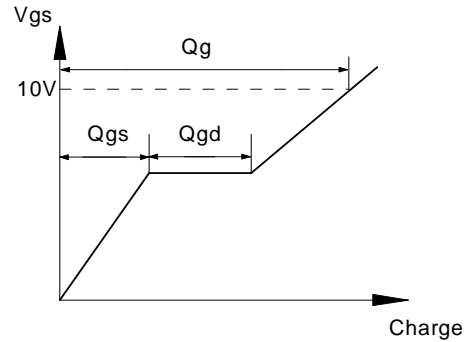
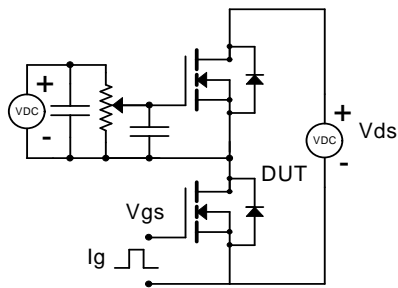
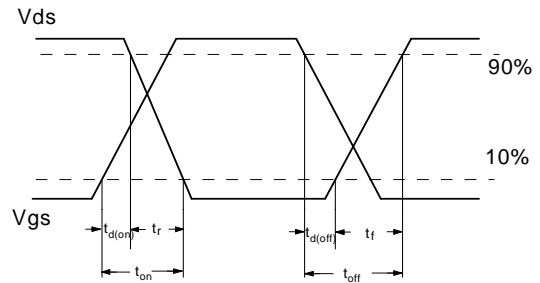
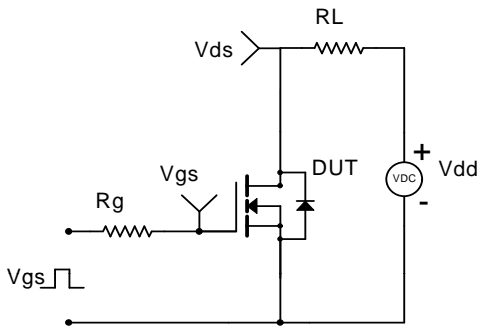


Figure 16: Diode Reverse Recovery Time and Softness Factor vs. di/dt

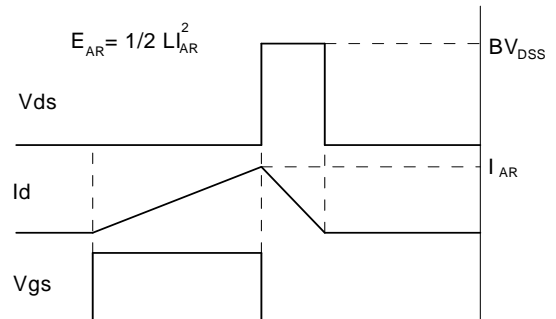
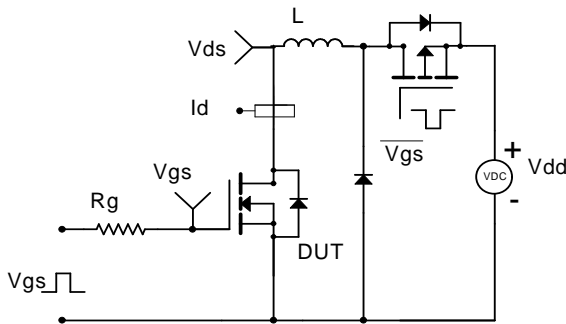
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

