

ID-1 Detection

Description

The CXD2085M is an IC which has the function of detecting ID-1 (EIAJ, CPX1204) from the video signal.

Features

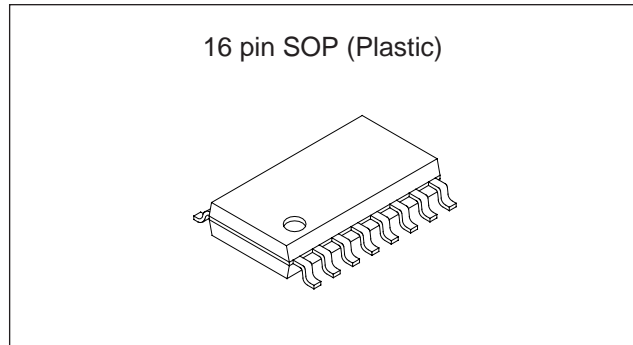
- Can detect the ID-1 signal on the NTSC video signal.
- Includes I²C bus interface. Also, IC can operate without the I²C bus.
- Includes a 2-bit general-purpose I/O port function. (When using I²C bus)

Applications

TVs

Structure

Silicon gate CMOS IC



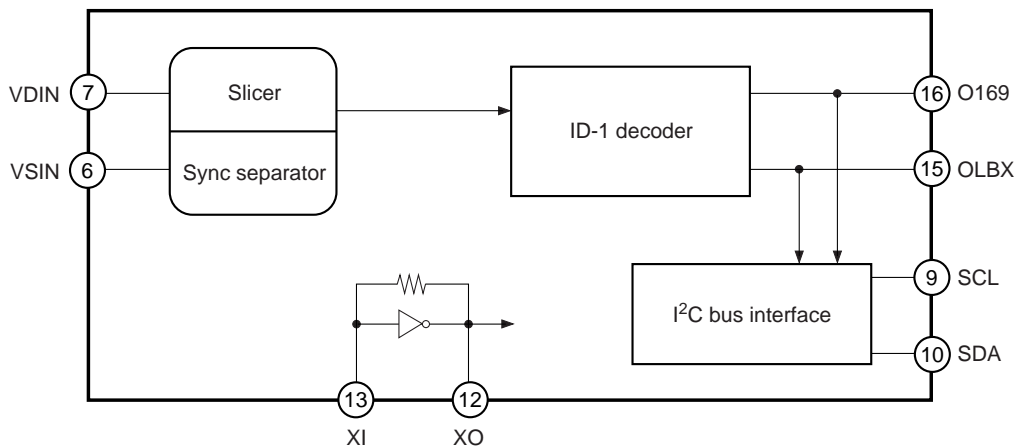
Absolute Maximum Ratings

• Supply voltage	V _{DD}	V _{SS} – 0.5 to +7.0	V
• Input voltage	V _I	V _{SS} – 0.5 to V _{DD} + 0.5	V
• Output voltage	V _O	V _{SS} – 0.5 to V _{DD} + 0.5	V
• Storage temperature	T _{stg}	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V _{DD}	4.75 to 5.25	V
• Operating temperature	T _{opr}	–20 to +70	°C

Block Diagram



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Pin Description

Pin No.	Symbol	I/O	Input level	Description
1	XRST	I	TTL *1, *4	Reset at "0".
2	TST	I	TTL *2	Test input; connect to Vss.
3	MCON	I	CMOS	Switching between use and no use of I ² C bus; No I ² C bus when Low.
4	ISET	I	ANALOG	Bias current setting.
5	AV _{DD}			Analog power supply.
6	VSIN	I	ANALOG	Sync separation input.
7	VDIN	I	ANALOG	Data slicer input.
8	AV _{SS}			Analog GND.
9	SCL	I	CMOS *1	I ² C bus clock.
10	SDA	I/O	CMOS *1, *3	I ² C bus data.
11	V _{DD}			Digital power supply.
12	XO	O		Oscillator connection. (14.318MHz)
13	XI	I	CMOS	Oscillator connection, or clock input.
14	V _{SS}			Digital GND.
15	OLBX	I/O	TTL	Letter-box bit output when ID detection result is output. Or, general-purpose I/O port by the I ² C bus setting.
16	O169	I/O	TTL	Full-mode bit output when ID detection result is output. Or, general-purpose I/O port by the I ² C bus setting.

*1 Schmitt input *2 With pull-down resistor *3 Open drain *4 With pull-up resistor

Connect SCL (Pin 9) to V_{SS} in no I²C bus mode with MCON (Pin 3) to Low. Connect SDA (Pin 10) to V_{SS} or V_{DD} in no I²C bus mode.

Electrical Characteristics

DC Characteristics (Logic section)

(V_{DD} = 5.0V ± 5%, V_{SS} = 0V, T_a = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Output voltage	V _{OH}	I _{OH} = -2mA	V _{DD} - 0.8			V	Pins 15, 16
	V _{OL}	I _{OL} = 4mA			0.4	V	
Output voltage	V _{OH}	I _{OH} = -3mA	V _{DD} /2			V	Pin 12
	V _{OL}	I _{OL} = 3mA			V _{DD} /2	V	
Output voltage	V _{OL}	I _{OL} = 3mA			0.4	V	Pin 10
Input voltage	V _{IH}		2.0			V	Pins 15, 16
	V _{IL}				0.8	V	
Input voltage	V _{IH}		2.2			V	Pins 1, 2
	V _{IL}				0.8	V	
Input voltage	V _{IH}		0.7 × V _{DD}			V	Pins 3, 13
	V _{IL}				0.3 × V _{DD}	V	
Input voltage	V _{IH}		0.8 × V _{DD}			V	Pins 9, 10
	V _{IL}				0.2 × V _{DD}	V	
Input hysteresis width	V _{hys}			0.6		V	Pins 9, 10
				0.4		V	Pin 1
Input leak current	i _i	V _{IN} = V _{SS} or V _{DD}	-10		+10	μA	Pins 3, 9
Output leak current	i _{oz}	V _{IN} = V _{SS} or V _{DD}	-40		+40	μA	Pins 10, 15, 16
Input current	i _i	V _{IN} = V _{SS}	-40	-100	-240	μA	Pin 1
Input current	i _i	V _{IN} = V _{DD}	40	100	240	μA	Pin 2
Feedback resistance	R _{fbk}	XI (Pin 13) = V _{SS} or V _{DD}	250k	1M	2.5M	Ω	Between Pins 12 and 13
Current consumption	I _{DD}	Clock frequency: 14.318MHz		9		mA	Sum of Pins 5 and 11

AC Characteristics

(V_{DD} = 5.0V ± 5%, V_{SS} = 0V, T_a = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Clock frequency	f _{xi}			14.318		MHz	Pin 13 input, or oscillator between Pins 12 and 13

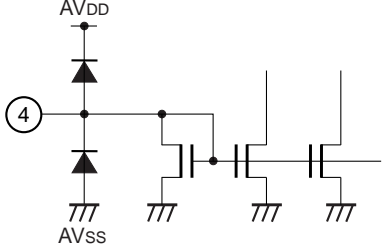
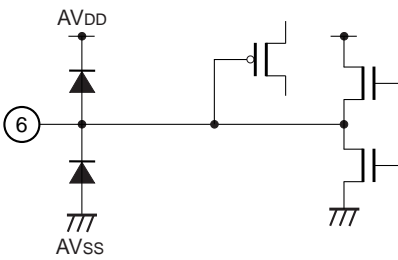
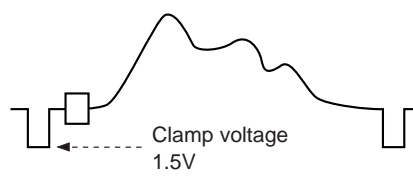
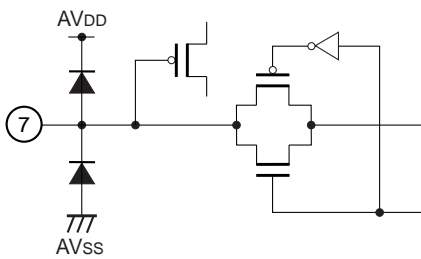
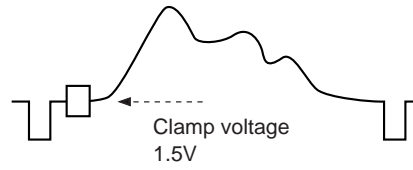
I/O Pin Capacitance

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Input pin capacitance	C _{IN}	V _{DD} = V _I = 0V, f = 1MHz			9	pF	
Output pin capacitance	C _{OUT}	V _{DD} = V _I = 0V, f = 1MHz			11	pF	
I/O pin capacitance	C _{I/O}	V _{DD} = V _I = 0V, f = 1MHz			11	pF	

Pin and Electrical Characteristics

Analog Section

($V_{DD} = 5.0V \pm 5\%$, $V_{SS} = 0V$, $T_a = 25^\circ C$)

Pin No.	Symbol	Equivalent circuit	Description
5	AV _{DD}	Not connected to V _{DD} (Pin 11) in the IC.	Analog power supply. Connect a low-noise power supply from the digital system.
8	AV _{SS}	Not connected to V _{SS} (Pin 14) in the IC.	Analog ground. Connect to the same potential as V _{SS} .
4	ISET		Bias setting. Connect to AV _{DD} (Pin 5) with 33kΩ.
6	VSIN		Sync tip clamp, sync separation input. Input with the capacitance coupled. 
7	VDIN		Pedestal clamp, ID signal data slice input. Input with the capacitance coupled. 

1. Description of ID-1 (transmission system of additional video information, aspect ratio identification)

As shown in the table below, the additional video information consists of 14-bits data, and a 6-bit CRCC is added to the data to form 20-bit data in total. This is carried on lines 20 and 283 in the vertical blanking area of the NTSC video signal.

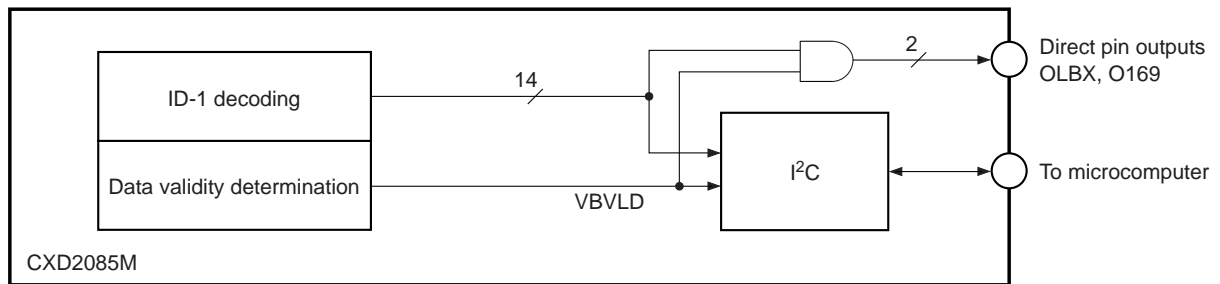
Table 1. Description of ID-1 signal

		Bit No.	Description	"1"	"0"
WORD0	A	1	Transmission aspect ratio	Full-mode (16:9) Letter-box —	4:3 Normal —
		2	Screen display format		
		3	Not defined		
	B	4 5 6	Identification information relating to the video signals and other signals (audio signals, etc.) transmitted simultaneously with the video signals		
WORD1		4bits	Identification signal dependent on WORD0		
WORD2		4bits	Identification signal and other information dependent on WORD0		

(From the Provisional standard of EIAJ, CPX-1204)

In the CXD2085M, the above 14-bit data are obtained in the I²C bus for I²C bus mode. Also, first two bits only can be output to OLBX (Pin 15) and O169 (Pin 16) set as the direct output pins.

2. Difference between ID-1 Data from the I²C Bus and Direct Output Pin



As shown in the figure above, the data validity determination which detects that the valid ID signal is exist or not, and the decoded result are obtained independently during ID-1 decoding. These two results are output to the direct output pins after taking their logical AND.

Processing inside the microcomputer which has acquired the information from the I²C bus is performed either by simply outputting this data directly to the pins or by taking the logical AND as above.

In addition, performing the processing when the data validity determination (VBVLD) is "1" and the decoding results bits 1 and 2 are "0" allows the video to be identified as 4:3 video.

3. General-Purpose I/O Port Function

In I²C bus mode, the CXD2085M can use two pins OLBX (Pin 15) and O169 (Pin 16) as the general-purpose I/O ports. The three types of setting are available; both two pins for inputs, for outputs, and one for input and another for output. While resetting by XRST (Pin 1) in I²C bus mode, two pins are set as the general-purpose input ports. Perform the power-on reset by XRST when there is a possibility that the IC external circuit and the OLBX and O169 signals could collide. Be sure to set the OLBX and O169 pins as the output pins when they are not used.

4. Clock

The CXD2085M requires a 4fsc clock (14.318MHz). When using a crystal oscillator, connect it between XI (Pin 13) and XO (Pin 12).

When inputting the clock from an external source, input it to XI (Pin 13).

5. Various Settings and Data I/O

The various settings and data I/O can be made by using the pin directly or using I²C bus interface.

5-1. I²C bus

By setting MCON (Pin 3) to High, the various settings and data extraction can be made with the I²C bus.

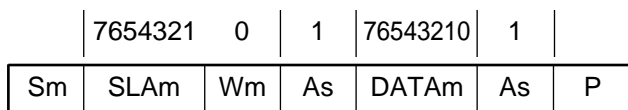
The CXD2085M supports the I²C bus slave RECEIVER and slave TRANSMITTER modes. The slave address is 40 (H).

In addition to standard mode (max. 100K bits/s), this IC also supports high-speed mode (max. 400K bits/s). Even when the power supply falls to 0V, it does not occupy the I²C bus. However, the absolute maximum ratings should not be exceeded.

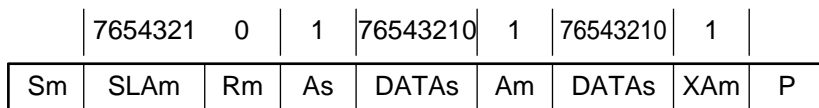
The I²C bus transmission process is shown in the figure below.

The number of transmission data is one byte for write (RECEIVER) and two bytes for read (TRANSMITTER). There is no sub-address setting function. Note that the I²C bus transmission cannot be performed during resetting by the XRST pin (Pin 1).

Data write (RECEIVER mode)



Data read (TRANSMITTER mode)



Symbol	Description
*m	from Master to Slave
*s	from Slave to Master
S	Start Condition
P	Stop Condition
SLA	Slave Address
DATA	Data
W	0: Write Master → Slave
R	1: Read Slave → Master
A	Clock pulse for Acknowledgment (SDA: L)
XA	Acknowledgment none (SDA: H)

Table 2. List of I²C bus controls

R/W		Bit	Symbol	Description										
WR	1st byte	bit7 MSB	POLBX	Output value when the OLBX pin used as the general-purpose output port.										
		bit6	PO169	Output value when the O169 pin used as the general-purpose output port.										
		bit5	PORT2	Settings whether the OLBX and O169 pins are used as the direct output pin of decoding result or as the general-purpose I/O port. <table border="1" style="margin-left: 20px;"> <tr> <td>PORT2</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>PORT1</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> </table>	PORT2	0	0	1	1	PORT1	0	1	0	1
		PORT2	0	0	1	1								
		PORT1	0	1	0	1								
		bit4	PORT1	OLBX pin function	Direct output	General-purpose I/O port Output Input Input								
				O169 pin function	Direct output	General-purpose I/O port Output Output Input								
		bit3	TST	Test signal. Be sure to set to Low.										
		bit2	XJGLK	Normally set to Low. When Low, the decoding result is held during the VCR variable-speed playback for home use. When High, it is not held.										
bit1	LNJ1	Normally set to Low. When Low, the ID signal can be detected not only for the line where it should locate but for one line before and after it. When High, decoding is performed only to the line where the ID signal should locate.												
bit0 LSB	RES	Normally set to Low. When High, the decoding function is reset. Reset immediately after switching the input signal such as for TV channels.												
RD	1st byte	bit7 MSB	ID5	ID decoding result 5th bit.										
		bit6	ID4	ID decoding result 4th bit.										
		bit5	ID3	ID decoding result 3rd bit.										
		bit4	ID1	ID decoding result 1st bit.										
		bit3	ID2	ID decoding result 2nd bit.										
		bit2	VBVLD	High when the valid ID signal is detected.										
		bit1	IOLBX	Input value when OLBX is used as the general-purpose input port.										
		bit0 LSB	IO169	Input value when O169 is used as the general-purpose input port. ID decoding result 14th bit when O169 is used as the general-purpose output port or as the direct output.										
	2nd byte	bit7 MSB	ID13	ID decoding result 13th bit.										
		bit6	ID12	ID decoding result 12th bit.										
		bit5	ID11	ID decoding result 11th bit.										
		bit4	ID10	ID decoding result 10th bit.										
		bit3	ID9	ID decoding result 9th bit.										
		bit2	ID8	ID decoding result 8th bit.										
		bit1	ID7	ID decoding result 7th bit.										
bit0 LSB	ID6	ID decoding result 6th bit.												

5-2. No bus mode

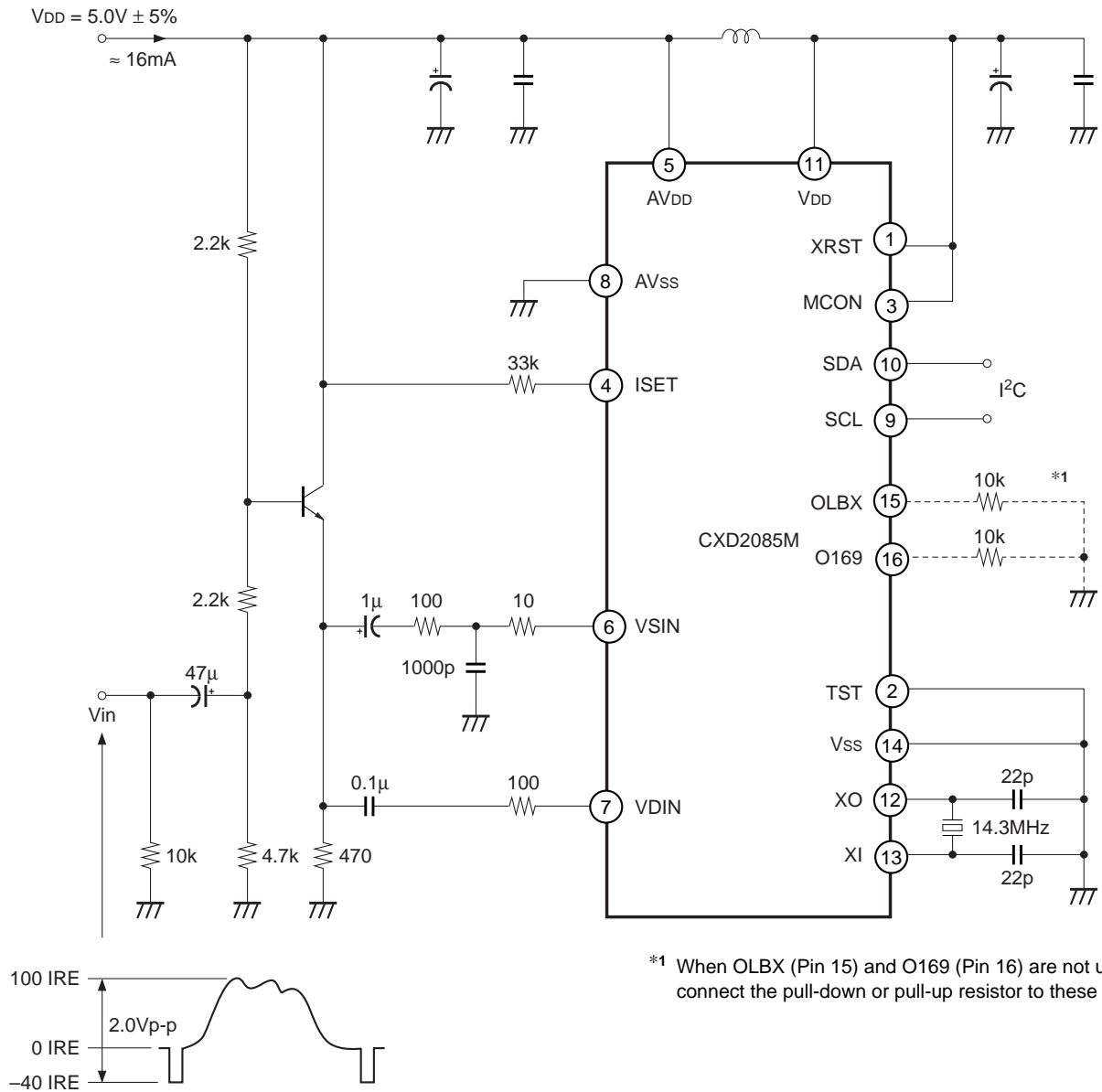
No bus mode is established when setting the MCON pin (Pin 3) to Low and then the CXD2085M can be operated without using the I²C bus.

In this case, the contents to be set by the I²C bus is fixed as shown below. OLBX and O169 obtain the decoding results as they become the direct output pins.

Table 3. Settings in No Bus Mode (Pin 3, MCON = Low)

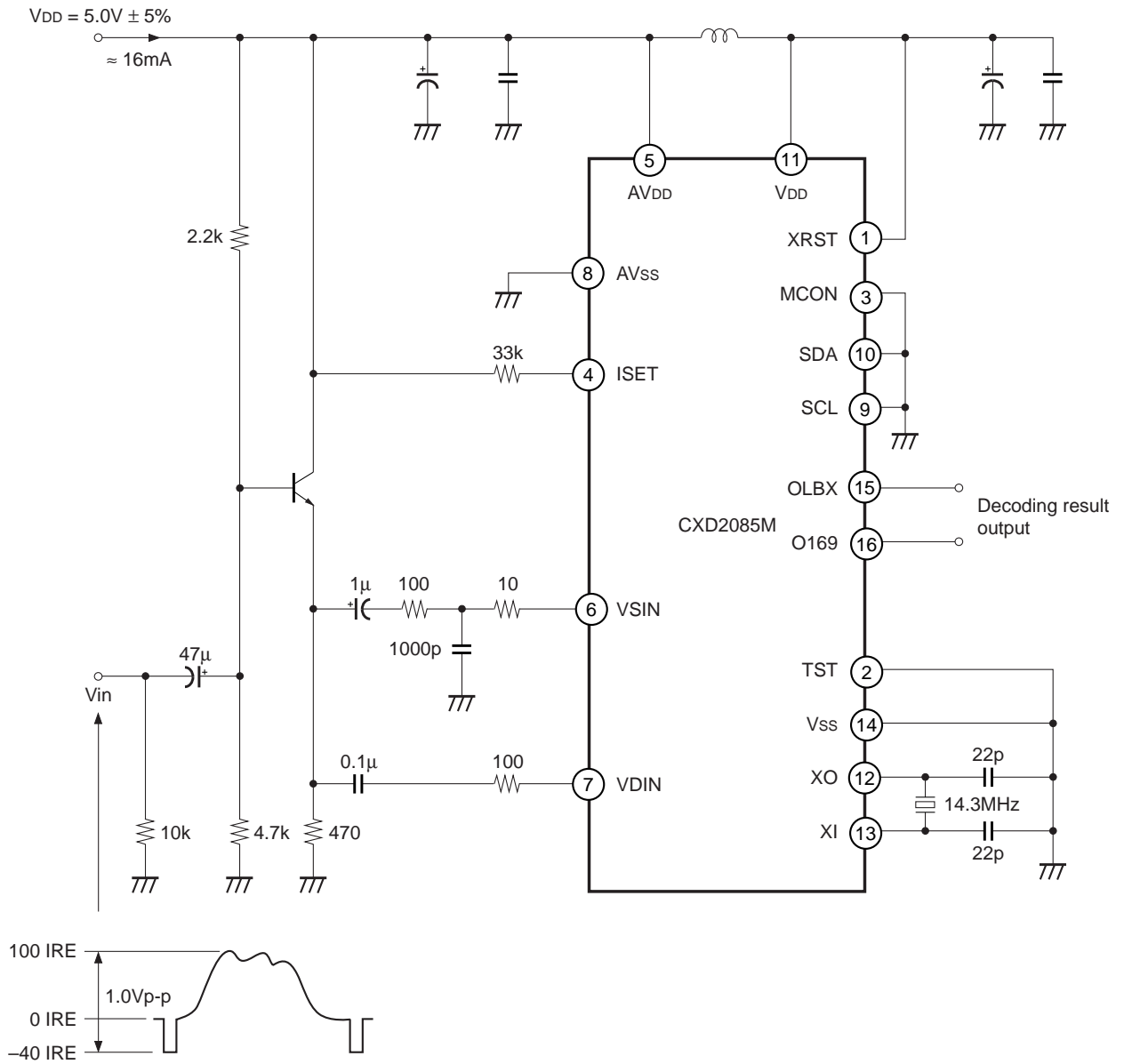
R/W		Bit	Symbol	Contents
WR	1st byte	bit7 MSB	POLBX	Fixed to Low. In no I ² C bus mode, there is no general-purpose I/O port function and this bit's operation is not affected.
		bit6	PO169	
		bit5	PORT2	PORT1 and PROT2 fixed to Low. The OLBX and O169 pins are the direct output pins of the ID decoding result.
		bit4	PORT1	
		bit3	TST	SCL (Pin 9) input reflected as it is. Therefore, connect the SCL pin to Vss in no I ² C bus mode.
		bit2	XJGLK	SCL (Pin 9) input reflected as it is. Fixed to Low as the SCL pin is surely connected to Vss.
		bit1	LNJ1	
		bit0 LSB	RES	Fixed to Low. When resetting is required, use the XRST pin (Pin 1).

Application Circuit For 2Vp-p input amplitude, using the I²C bus



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit For 1Vp-p input amplitude not using the I²C bus

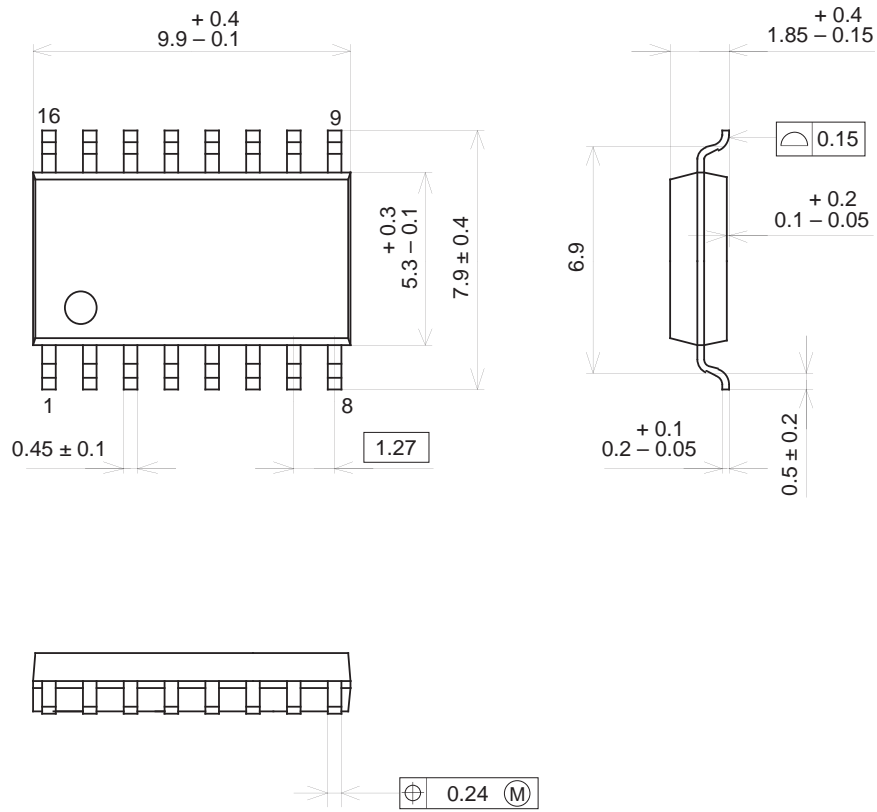


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Package Outline

Unit: mm

16PIN SOP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SOP-16P-L01
EIAJ CODE	SOP016-P-0300
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.2g