



STS10PF30L

P-CHANNEL 30V - 0.012 Ω - 10A SO-8 STripFET™ II POWER MOSFET

Table 1: General Features

TYPE	V _{DSS}	R _{DS(on)}	I _D
STS10PF30L	30V	<0.014 Ω	10 A

- TYPICAL R_{DS(on)} = 0.012 Ω
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- LOW THRESHOLD DRIVE

DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance.

APPLICATIONS

- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT
- LOAD SWITCH

Figure 1: Package

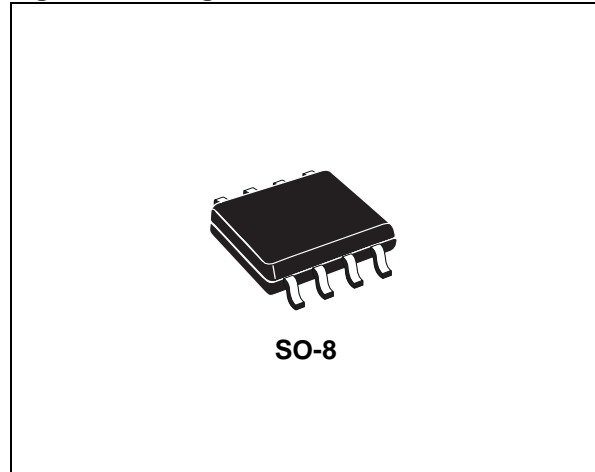


Figure 2: Internal Schematic Diagram

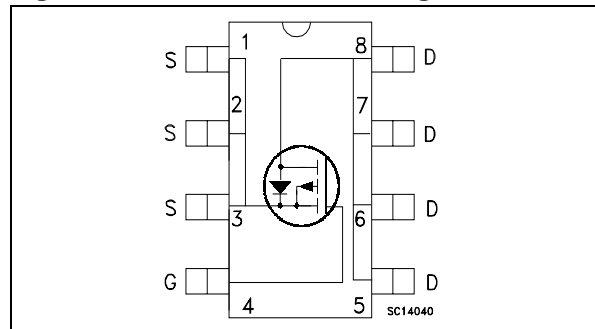


Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STS10PF30L	S10PF30L	SO-8	TAPE & REEL

Table 3: ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	30	V
V _{GS}	Gate-source Voltage	± 16	V
I _D	Drain Current (continuous) at T _C = 25°C	10	A
I _D	Drain Current (continuous) at T _C = 100°C	6	A
I _{DM} (•)	Drain Current (pulsed)	40	A
P _{tot}	Total Dissipation at T _C = 25°C	2.5	W

Note: For the P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed

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Table 4: THERMAL DATA

Rthj-amb	(*) Thermal Resistance Junction-ambient	Max	47	°C/W
Rthj-lead	Thermal Resistance Junction-leads	Max	16	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose	Typ	150	°C
T _{stg}	storage temperature		-55 to 150	°C

(*) When Mounted on 1 inch² FR-4 board, 2 oz of Cu and t ≤ 10 sec.

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Table 5: OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	30			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating T _C = 125°C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 16 V			±100	nA

Table 6: ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 μA	1			V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 5 A V _{GS} = 4.5 V I _D = 5 A		0.012 0.015	0.014 0.018	Ω Ω

Table 7: DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs}	Forward Transconductance	V _{DS} = 10 V I _D = 5 A		31		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		2300		pF
C _{oss}	Output Capacitance			750		pF
C _{rss}	Reverse Transfer Capacitance			115		pF

ELECTRICAL CHARACTERISTICS (continued)

Table 8: SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 15\text{ V}$ $I_D = 5\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, Figure 15)		72 87		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 15\text{ V}$ $I_D = 10\text{ A}$ $V_{GS} = 4.5\text{ V}$ (see test circuit, Figure 16)		29 6.8 7.6	39	nC nC nC

Table 9: SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 15\text{ V}$ $I_D = 5\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 4.5\text{ V}$ (Resistive Load, Figure 15)		89 27		ns ns

Table 10: SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain Current Source-drain Current (pulsed)				10 40	A A
$V_{SD}^{(*)}$	Forward On Voltage	$I_{SD} = 10\text{ A}$ $V_{GS} = 0$			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 10\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 15\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 17)		48.5 68 2.8		ns nC A

(*) Pulse width $\leq 300\ \mu\text{s}$, duty cycle 1.5 %.

(*) Pulse width limited by T_{JMAX}

Figure 3: Safe Operating Area

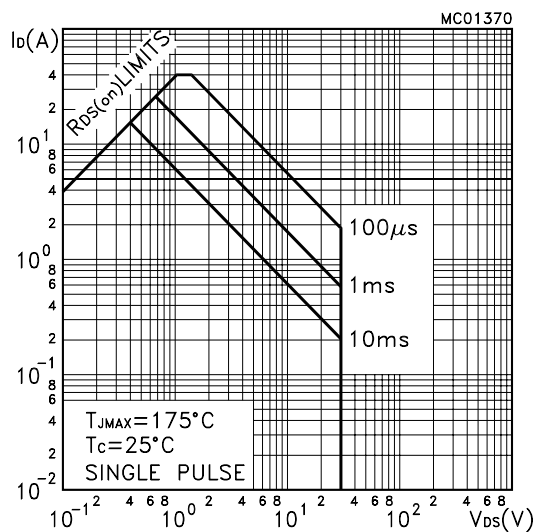


Figure 4: Thermal Impedance

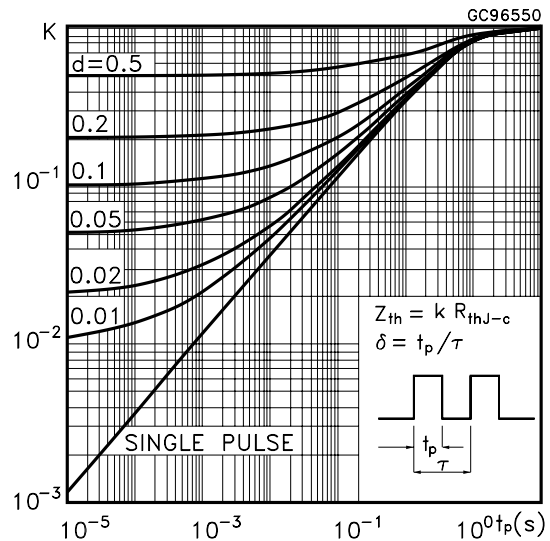


Figure 5: Output Characteristics

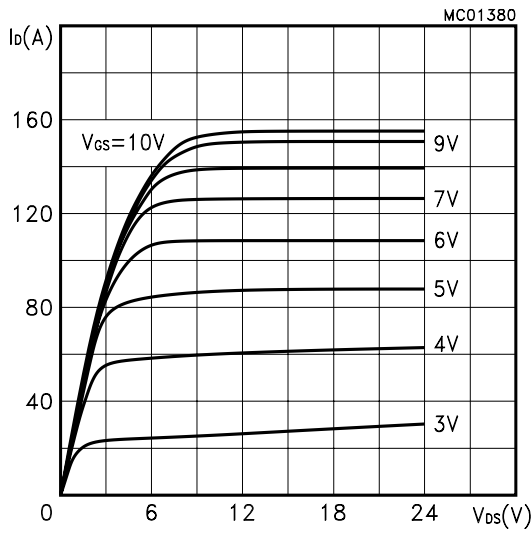


Figure 6: Transfer Characteristics

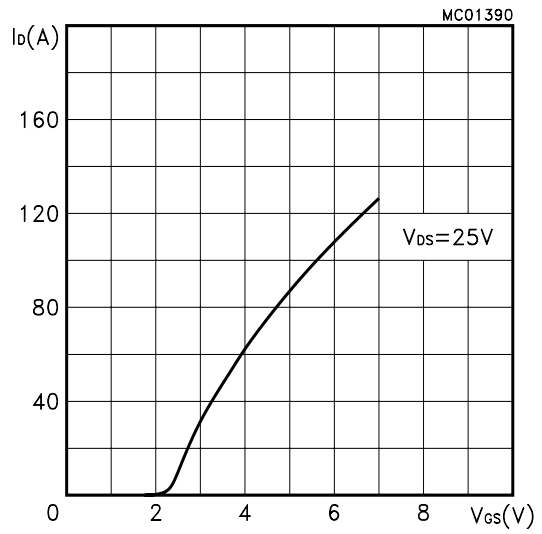


Figure 7: Transconductance

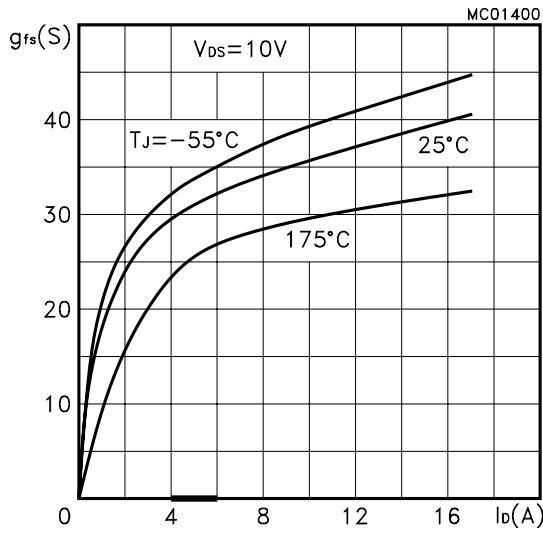


Figure 8: Static Drain-source On Resistance

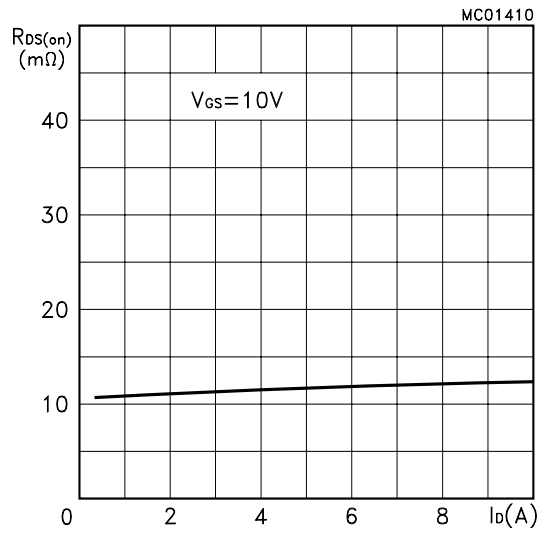


Figure 9: Gate Charge vs Gate-source Voltage

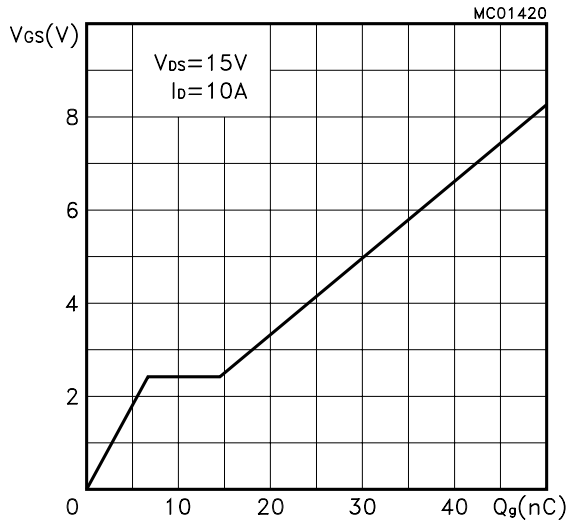


Figure 10: Capacitance Variations

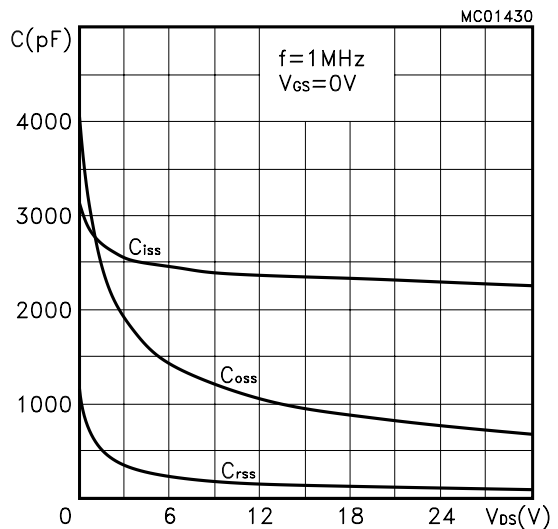


Figure 11: Normalized Gate Threshold Voltage vs Temperature

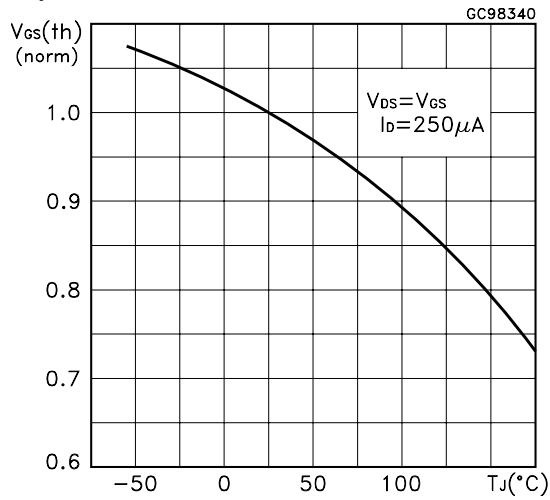


Figure 12: Normalized on Resistance vs Temperature

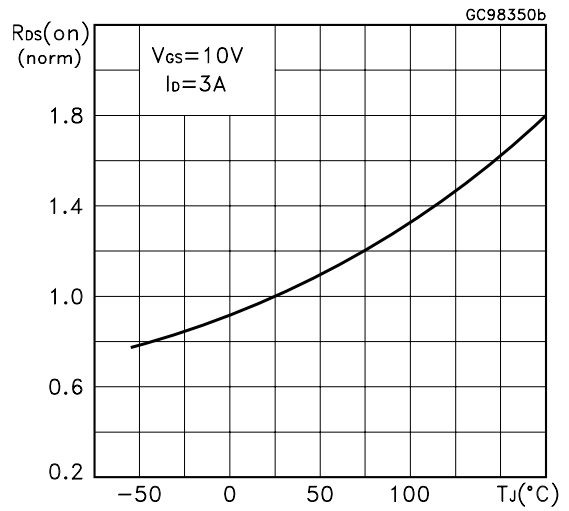


Figure 13: Source-drain Diode Forward Characteristics

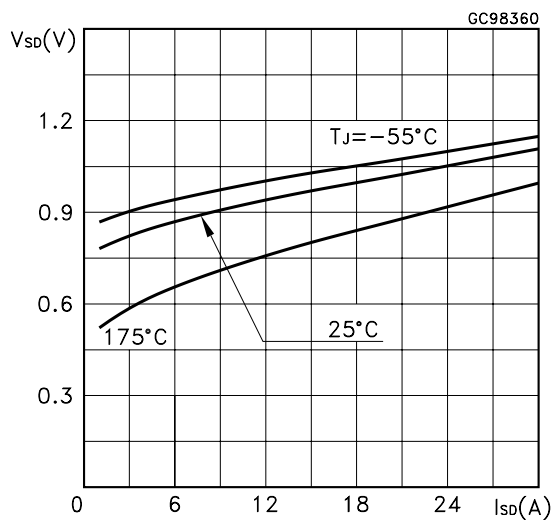


Figure 14: Normalized Breakdown Voltage vs Temperature.

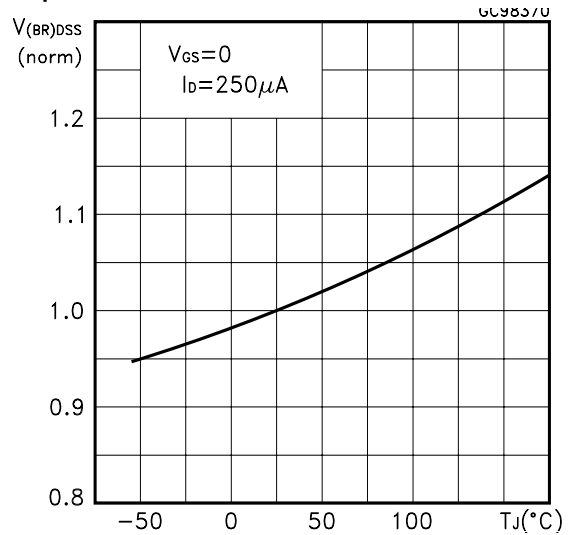


Fig. 15: Switching Times Test Circuits For Resistive Load

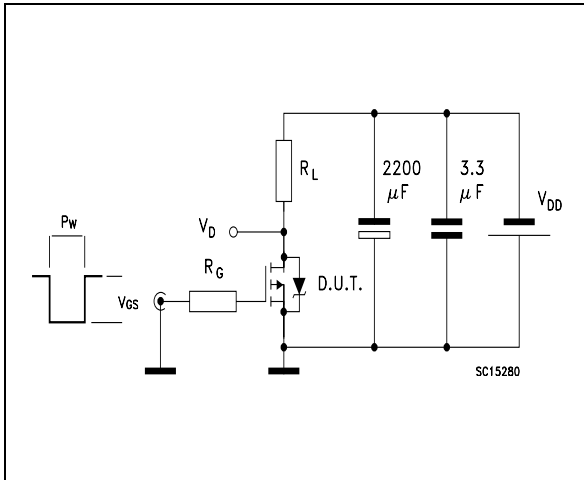


Fig. 16: Gate Charge test Circuit

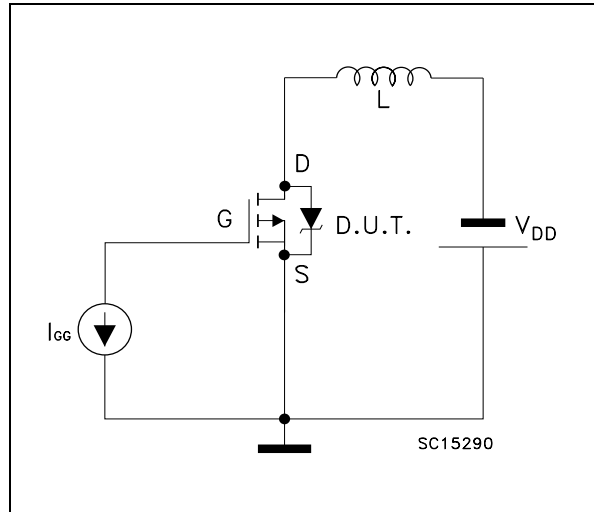
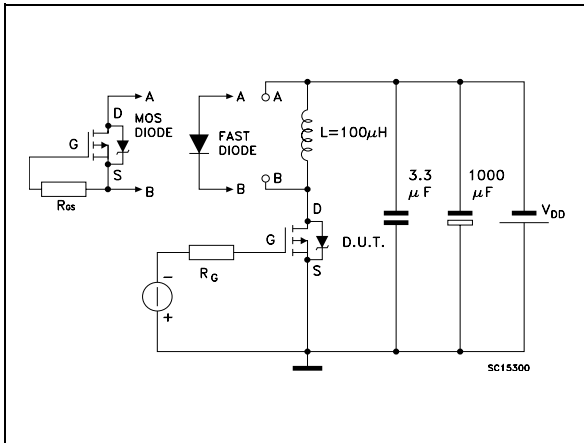
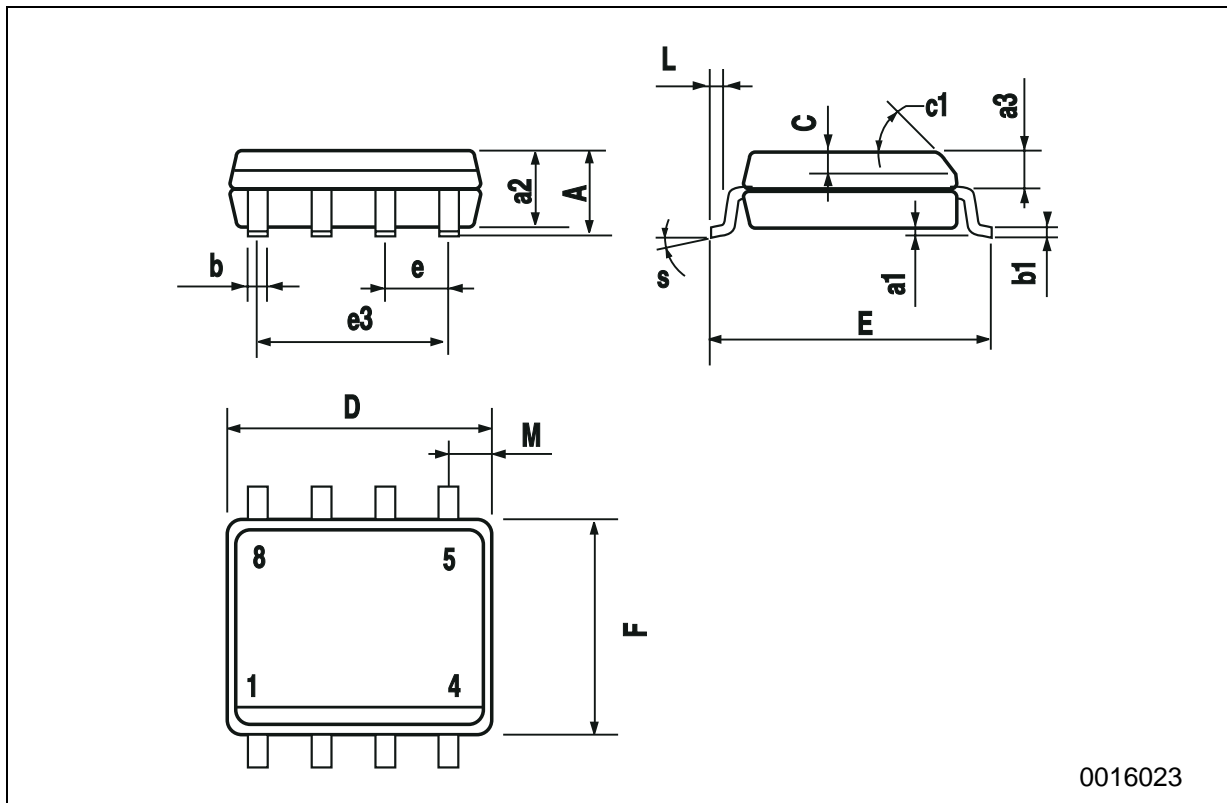


Fig. 17: Test Circuit For Diode Recovery Behaviour



SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



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Table 11:Revision History

Date	Revision	Description of Changes
May 2005	2.0	completed whit curves

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