



# 74LCX374

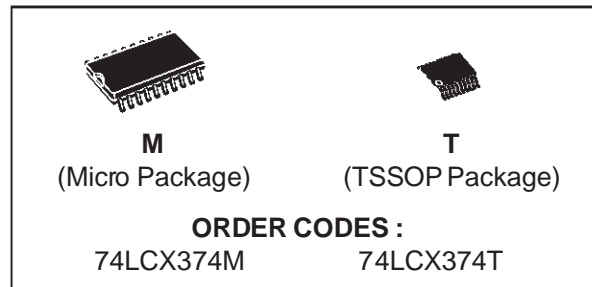
## OCTAL D-TYPE FLIP FLOP NON INVERTING (3-STATE) WITH 5V TOLERANT INPUTS AND OUTPUTS

- 5V TOLERANT INPUTS AND OUTPUTS
- HIGH SPEED:  
 $f_{MAX} = 150 \text{ MHz (MIN.) at } V_{CC} = 3\text{V}$
- POWER-DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 24 \text{ mA (MIN)}$
- PCI BUS LEVELS GUARANTEED AT 24mA
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:  
 $V_{CC} \text{ (OPR)} = 2.0\text{V to } 3.6\text{V (1.5V Data Retention)}$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 374
- LATCH-UP PERFORMANCE EXCEEDS 500mA
- ESD PERFORMANCE:  
 $\text{HBM} > 2000\text{V}; \text{MM} > 200\text{V}$

### DESCRIPTION

The LCX374 is a low voltage CMOS OCTAL D-TYPE FLIP FLOP with 3 STATE OUTPUT NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology. It is ideal for low power and high speed applications; it can be interfaced to 5V signal environment for both inputs and outputs.

These 8 bit D-Type flip-flops are controlled by a clock input (CK) and an output enable input ( $\overline{\text{OE}}$ ). On the positive transition of the clock, the Q



outputs will be set to the logic state that were setup at the D inputs.

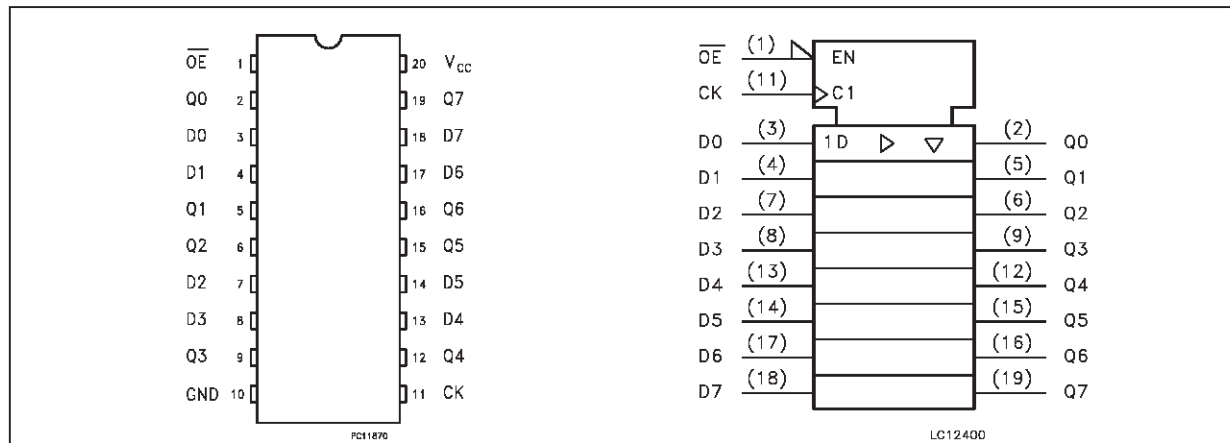
While the ( $\overline{\text{OE}}$ ) input is low, the 8 outputs will be in a normal state (high or low logic level) and while high level the outputs will be in a high impedance state.

The output control does not affect the internal operation of flip flops; that is, the old data can be retained or the new data can be entered even while the outputs are off.

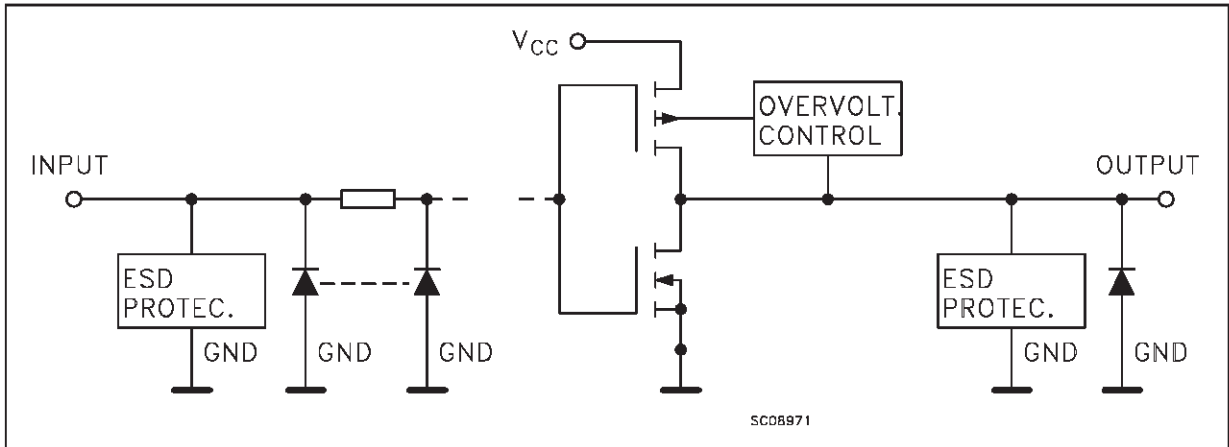
It has same speed performance at 3.3V than 5V, AC/ACT family, combined with a lower power consumption. It has better speed performance at 3.3V than 5V LSTTL family combined with the true CMOS low power consumption.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

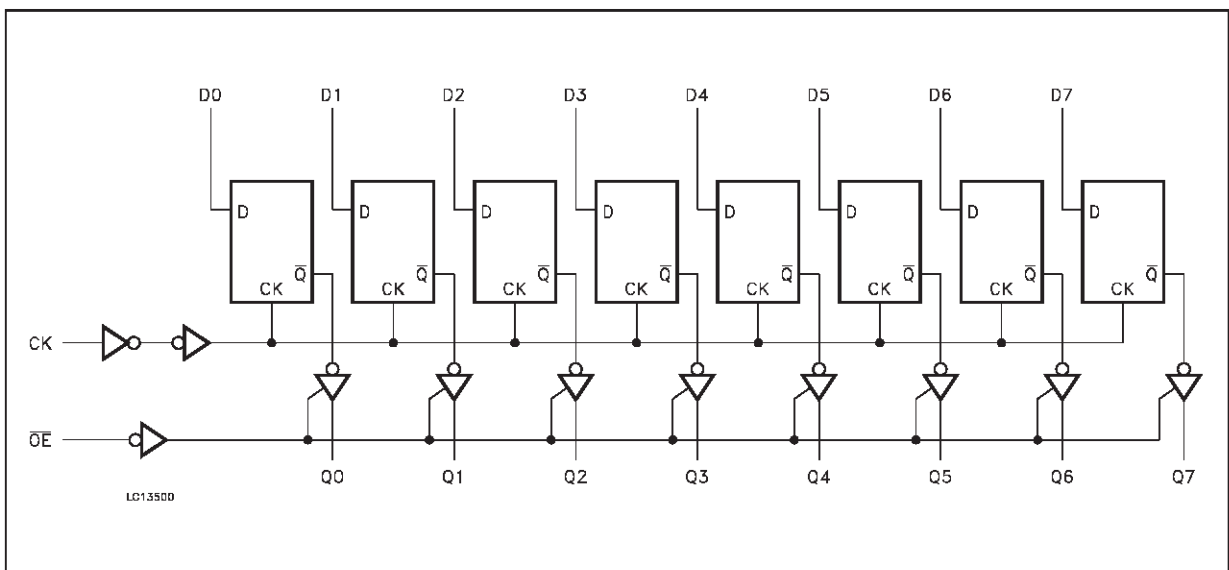
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State Output Enable Input (Active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 to Q7	3 State Outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data Inputs
11	CLOCK	Clock Input (LOW to HIGH, edge triggered)
10	GND	Ground (0V)
20	V <sub>CC</sub>	Positive Supply Voltage

TRUTH TABLE

INPUTS			OUTPUTS
$\overline{OE}$	CK	D	Q
H	X	X	Z
L		X	NO CHANGE
L		L	L
L		H	H

X: "H" or "L"  
Z: High Impedance

LOGIC DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	-0.5 to +7.0	V
V <sub>I</sub>	DC Input Voltage	-0.5 to +7.0	V
V <sub>O</sub>	DC Output Voltage (OFF state)	-0.5 to +7.0	V
V <sub>O</sub>	DC Output Voltage (High or Low State) (note1)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	DC Input Diode Current	- 50	mA
I <sub>OK</sub>	DC Output Diode Current (note2)	± 50	mA
I <sub>O</sub>	DC Output Source/Sink Current	± 50	mA
I <sub>CC</sub>	DC Supply Current per Supply Pin	± 100	mA
I <sub>GND</sub>	DC Ground Current per Supply Pin	± 100	mA
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

1) I<sub>O</sub> absolute maximum rating must be observed

2) V<sub>O</sub> < GND, V<sub>O</sub> > V<sub>CC</sub>

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage (note 1)	2.0 to 3.6	V
V <sub>I</sub>	Input Voltage	0 to 5.5	V
V <sub>O</sub>	Output Voltage (OFF state)	0 to 5.5	V
V <sub>O</sub>	Output Voltage (High or Low State)	0 to V <sub>CC</sub>	V
I <sub>OH</sub> , I <sub>OL</sub>	High or Low Level Output Current (V <sub>CC</sub> = 3.0 to 3.6V)	± 24	mA
I <sub>OH</sub> , I <sub>OL</sub>	High or Low Level Output Current (V <sub>CC</sub> = 2.7 to 3.0V)	± 12	mA
T <sub>op</sub>	Operating Temperature:	-40 to +85	°C
dt/dv	Input Transition Rise or Fall Rate (V <sub>CC</sub> = 3.0V) (note 2)	0 to 10	ns/V

1) Truth Table guaranteed: 1.5V to 3.6V

2) V<sub>IN</sub> from 0.8V to 2.0V

## DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value		Unit
		V <sub>CC</sub> (V)		-40 to 85 °C		
				Min.	Max.	
V <sub>IH</sub>	High Level Input Voltage	2.7 to 3.6		2.0		V
V <sub>IL</sub>	Low Level Input Voltage				0.8	V
V <sub>OH</sub>	High Level Output Voltage	2.7 to 3.6	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> =-100 μA	V <sub>CC</sub> -0.2	V
		2.7		I <sub>O</sub> =-12 mA	2.2	
		3.0		I <sub>O</sub> =-18 mA	2.4	
				I <sub>O</sub> =-24 mA	2.2	
V <sub>OL</sub>	Low Level Output Voltage	2.7 to 3.6	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> =100 μA	0.2	V
		2.7		I <sub>O</sub> =12 mA	0.4	
		3.0		I <sub>O</sub> =16 mA	0.4	
		3.0		I <sub>O</sub> =24 mA	0.55	
I <sub>I</sub>	Input Leakage Current	2.7 to 3.6	V <sub>I</sub> = 0 to 5.5 V		±5	μA
I <sub>OZ</sub>	3 State Output Leakage Current	2.7 to 3.6	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = 0 to 5.5V		±5	μA
I <sub>off</sub>	Power Off Leakage Current	0	V <sub>I</sub> or V <sub>O</sub> = 5.5V		100	μA
I <sub>CC</sub>	Quiescent Supply Current	2.7 to 3.6	V <sub>I</sub> = V <sub>CC</sub> or GND		10	μA
			V <sub>I</sub> or V <sub>O</sub> = 3.6 to 5.5V		±10	
ΔI <sub>CC</sub>	ICC incr. per input	2.7 to 3.6	V <sub>IH</sub> = V <sub>CC</sub> -0.6V		500	μA

## DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value			Unit
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25 °C			
				Min.	Typ.	Max.	
V <sub>OLP</sub>	Dynamic Low Voltage Quiet Output (note 1)	3.3	C <sub>L</sub> = 50 pF V <sub>IL</sub> = 0 V V <sub>IH</sub> = 3.3V		0.8		V
V <sub>OLV</sub>					-0.8		

1) Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.

**AC ELECTRICAL CHARACTERISTICS** ( $C_L = 50 \text{ pF}$ ,  $R_L = 500 \text{ } \Omega$ , Input  $t_r = t_f = 2.5 \text{ ns}$ )

Symbol	Parameter	Test Condition		Value		Unit
		$V_{CC}$ (V)	Waveform	-40 to 85 °C		
				Min.	Max.	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time	2.7 3.0 to 3.6	1	1.5 1.5	9.5 8.5	ns
$t_{PZL}$ $t_{PZH}$	Output Enable Time to HIGH and LOW level	2.7 3.0 to 3.6	2	1.5 1.5	9.5 8.5	ns
$t_{PLZ}$ $t_{PHZ}$	Output Disable Time from HIGH and LOW level	2.7 3.0 to 3.6	2	1.5 1.5	8.5 7.5	ns
$t_s$	Setup Time, HIGH or LOW level Dn to CK	2.7 3.0 to 3.6	1	2.5 2.5		ns
$t_h$	Hold Time, HIGH or LOW level Dn to CK	2.7 3.0 to 3.6	1	1.5 1.5		ns
$t_w$	CK Pulse Width, HIGH or LOW	2.7 3.0 to 3.6	3	3.3 3.3		ns
$f_{MAX}$	Clock Pulse Frequency	3.0 to 3.6	1	150		MHz
$t_{OSLH}$ $t_{OSHL}$	Output to Output Skew Time (note 1, 2)	3.0 to 3.6			1.0	ns

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ( $t_{OSLH} = |t_{PLHm} - t_{PLHr}|$ ,  $t_{OSHL} = |t_{PHLm} - t_{PHLr}|$ )

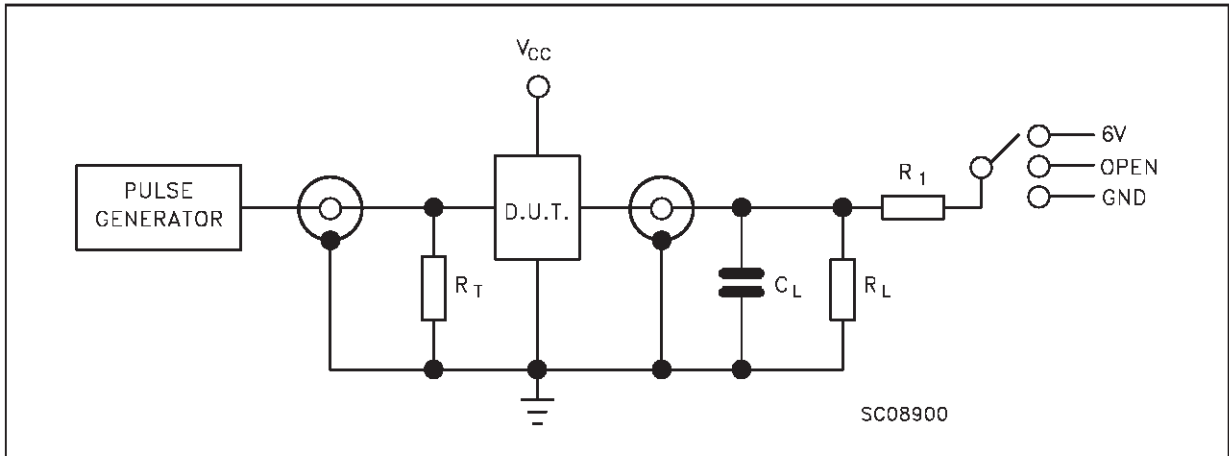
2) Parameter guaranteed by design

**CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Test Conditions		Value			Unit
		$V_{CC}$ (V)		$T_A = 25 \text{ } ^\circ\text{C}$			
				Min.	Typ.	Max.	
$C_{IN}$	Input Capacitance	3.3	$V_{IN} = 0 \text{ to } V_{CC}$		6		pF
$C_{OUT}$	Output Capacitance	3.3	$V_{IN} = 0 \text{ to } V_{CC}$		12		pF
$C_{PD}$	Power Dissipation Capacitance (note 1)	3.3	$f_{IN} = 10\text{MHz}$ $V_{IN} = 0 \text{ or } V_{CC}$		32		pF

1)  $C_{PD}$  is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the following equation.  $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$  (per Flip-Flop)

TEST CIRCUIT



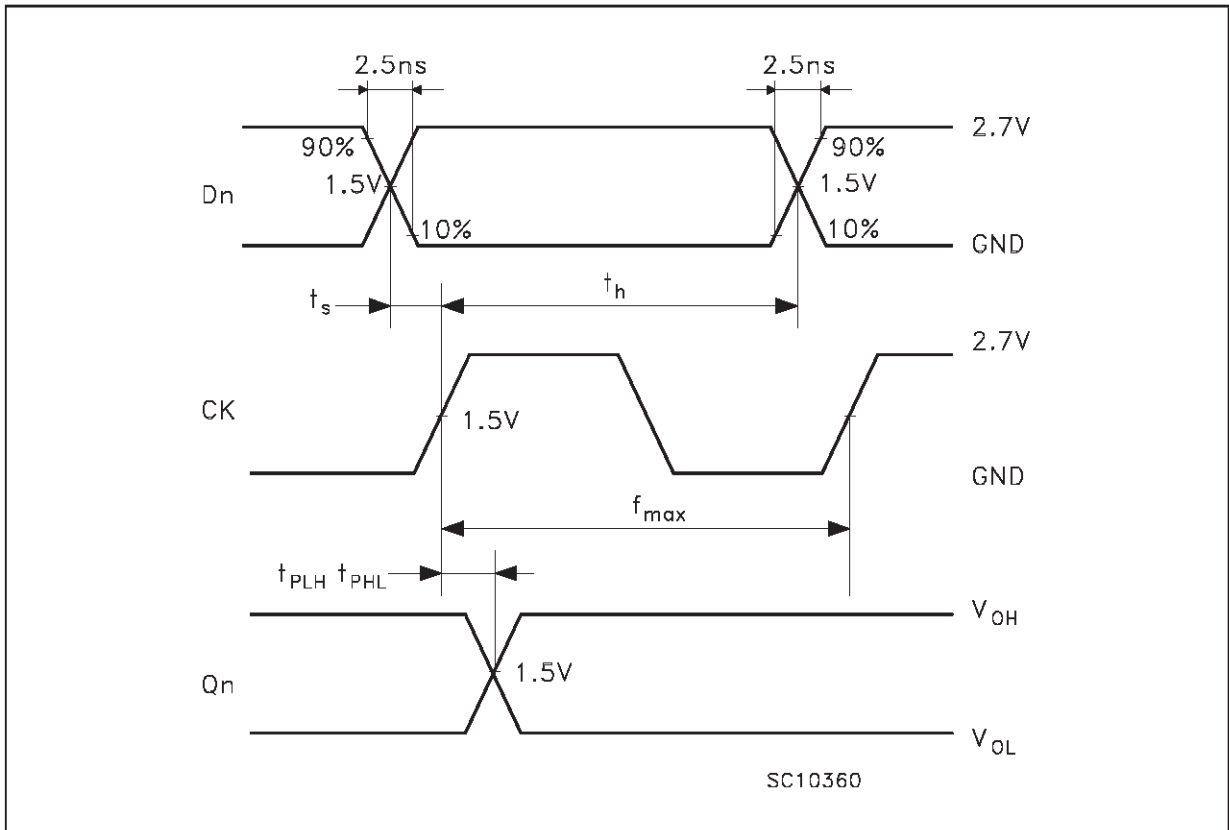
TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	6V
$t_{PZH}$ , $t_{PHZ}$	GND

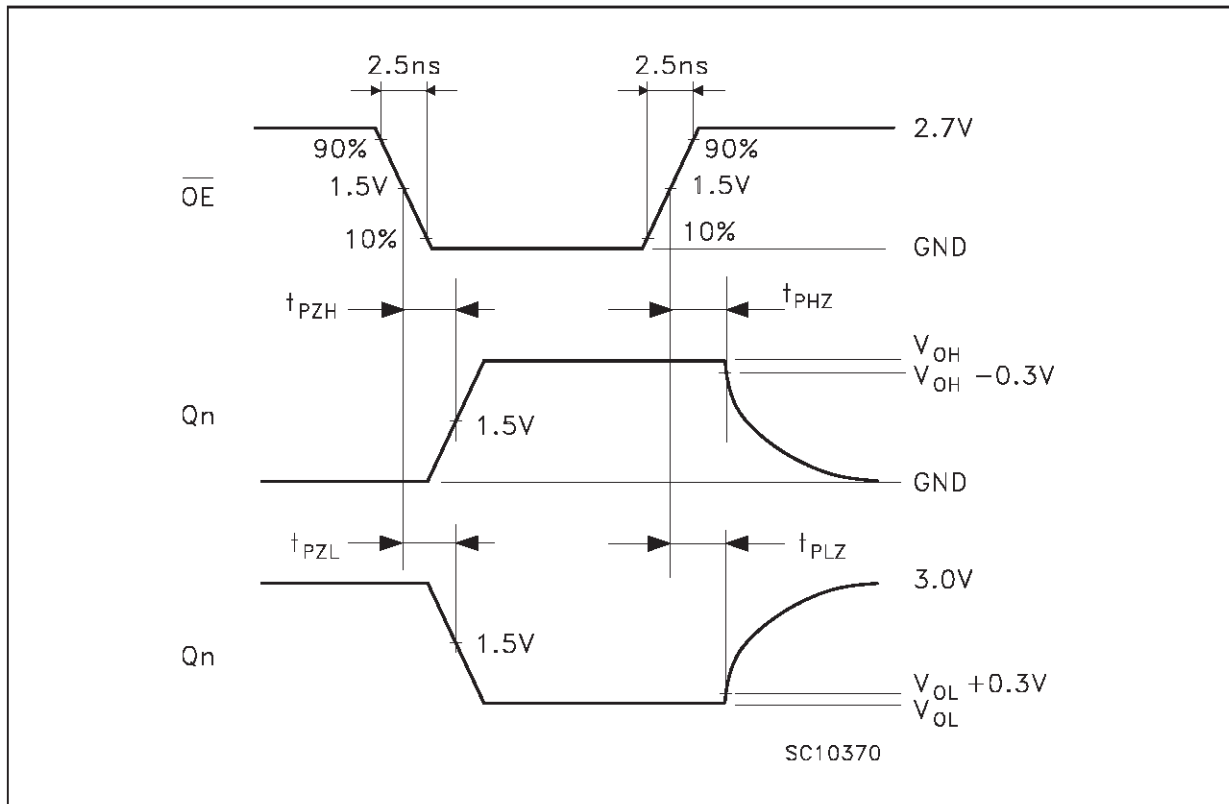
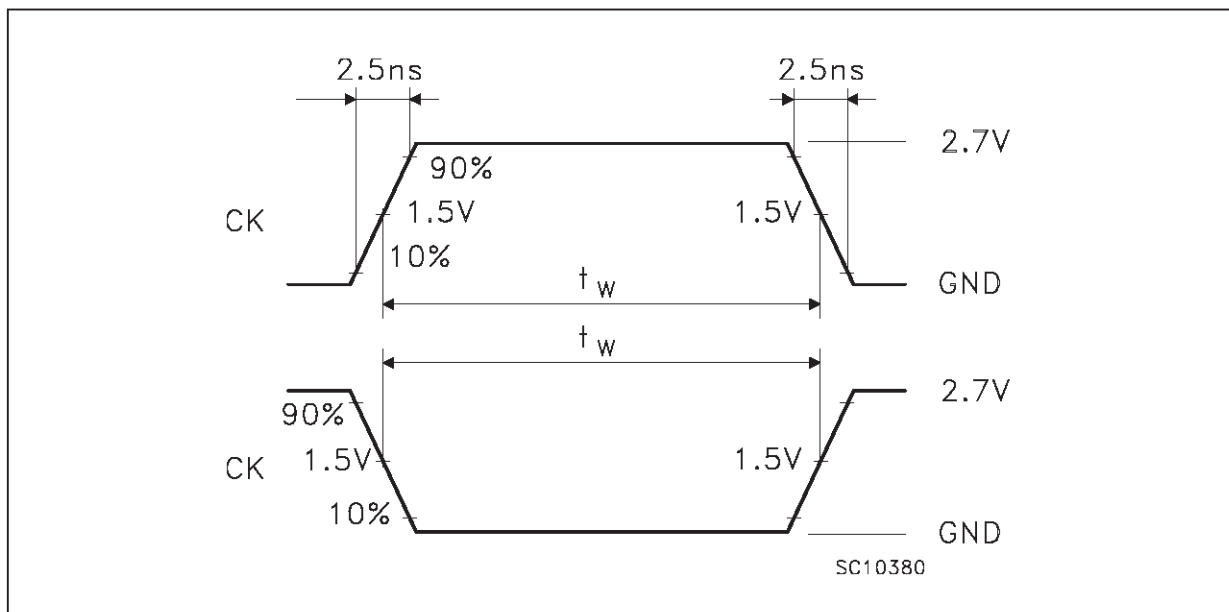
$C_L$  = 50 pF or equivalent (includes jig and probe capacitance)

$R_L$  =  $R_1$  = 500Ω or equivalent

$R_T$  =  $Z_{out}$  of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAYS, SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)



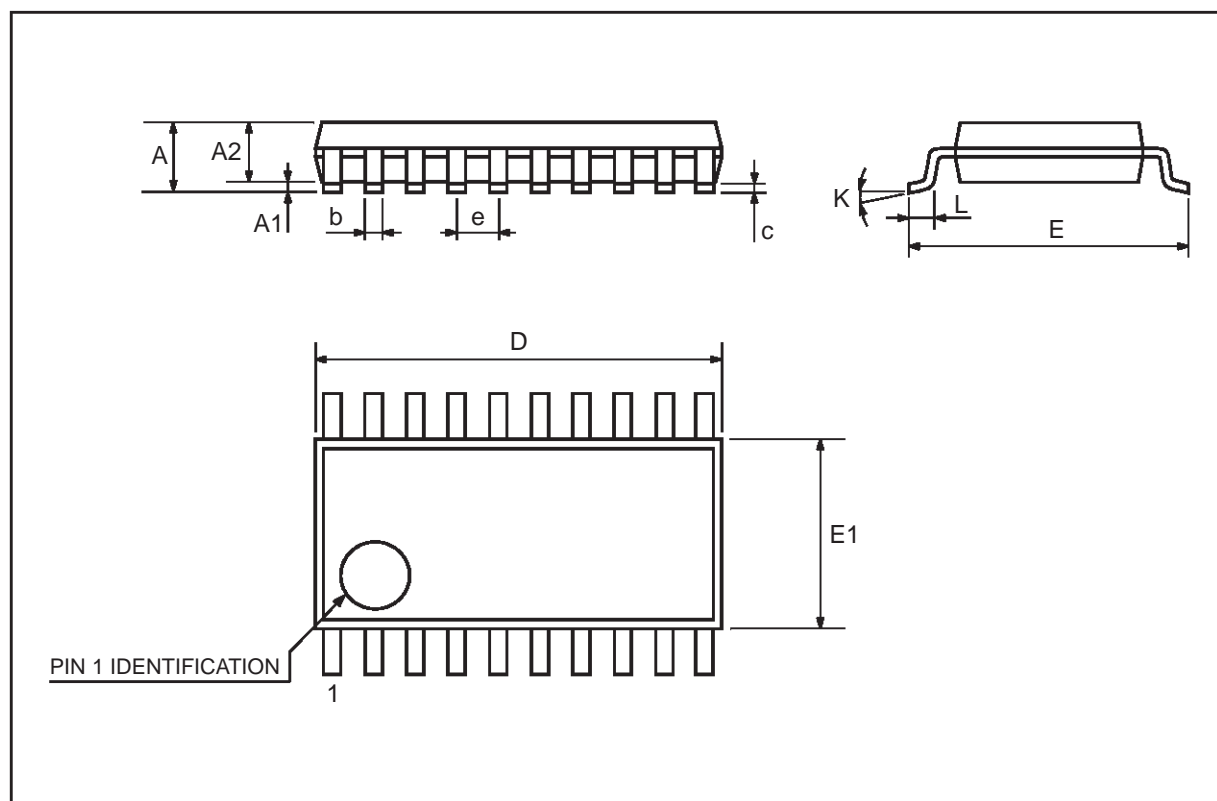
**WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIMES** ( $f=1\text{MHz}$ ; 50% duty cycle)**WAVEFORM 3: PULSE WIDTH**





## TSSOP20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.2	0.0035		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



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