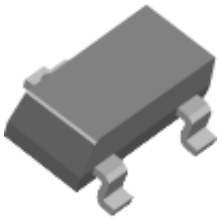
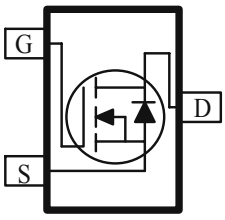
N-Channel 60V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are power switch, power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Low Gate Charge
- Fast Switch
- Miniature SOT-23 Surface Mount Package Saves Board Space

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.194 @ V_{GS} = 10 V	2.2
	0.273 @ V_{GS} = 4.5V	1.8





ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current[a]	T_A=25°C	I_D	2.2	A
	T_A=70°C		1.7	
Pulsed Drain Current[b]		I_{DM}	±15	
Continuous Source Current (Diode Conduction)[a]		I_S	1.7	A
Power Dissipation[a]	T_A=25°C	P_D	1.3	W
	T_A=70°C		0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient[a]	t <= 5 sec	R_{THJA}	100	°C/W
	Steady-State		166	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

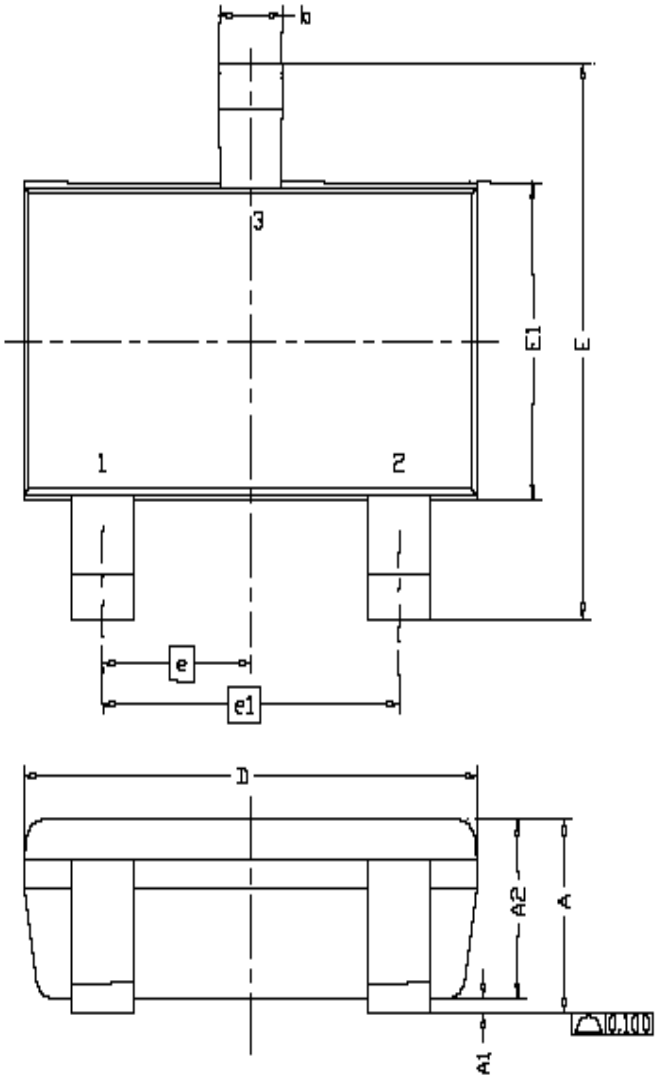
SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Conditions**	**Limits**			**Unit**
			Min	**Typ**	**Max**	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 uA	1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			1	uA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 55°C			50	
On-State Drain Current[A]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	10			A
Drain-Source On-Resistance[A]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 2.2 A			194	mΩ
		V_{GS} = 4.5 V, I_D = 1.8 A			273	
Forward Tranconductance[A]	g_{fs}	V_{DS} = 4.5 V, I_D = 2.2 A		8		S
Diode Forward Voltage	V_{SD}	I_S = 1.7 A, V_{GS} = 0 V			1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 30 V, V_{GS} = 5 V, I_D = 2.2 A		4.0		nC
Gate-Source Charge	Q_{gs}			4.0		
Gate-Drain Charge	Q_{gd}			2.0		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, R_L = 30 Ω, I_D = 1 A, V_{GEN} = 10 V		10		ns
Rise Time	t_r			10		
Turn-Off Delay Time	$t_{d(off)}$			20		
Fall-Time	t_f			10		
Source-Ddrain Reverse Recovery Time	t_{rr}	I_F = 1.7 A, di/dt = 100 A/uS		50		

Notes

a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.

Package Information



DIM.	MILLIMETERS		
	MIN	NOM	MAX
A	0.935	0.95	1.10
A1	0.01	---	0.10
A2	0.85	0.90	0.925
b	0.30	0.40	0.50
c	0.10	0.15	0.25
D	2.70	2.90	3.10
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.40	0.60
L1	0.60REF		
L2	0.25BSC		
R	0.10	---	---
θ	0°	4°	8°
θ1	7°NOM