

74ABT162245A; 74ABTH162245A

16-bit bus transceiver with 30 Ω series termination resistors;
3-state

Rev. 3 — 31 August 2017

Product data sheet

1 General description

The 74ABT162245A is a high-performance BiCMOS product, which combines low static and dynamic power dissipation with high speed.

This device is a 16-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features two output enable inputs ($n\overline{OE}$) for easy cascading and two direction inputs ($n\overline{DIR}$) for direction control.

The 74ABT162245A is designed with 30 Ω series resistance in both the upper and lower output structures. This design reduces line noise in applications such as memory address drivers, clock drivers and bus receivers and transmitters.

Two options are available, 74ABT162245A which does not have the bus hold feature and the 74ABTH162245A which incorporates the bus hold feature.

2 Features and benefits

- 16-bit bidirectional bus interface
- Multiple V_{CC} and GND pins minimize switching noise
- 3-state buffers
- Output capability: +12 mA/–32 mA
- 74ABTH162245A incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Integrated 30 Ω termination resistors
- Power-up 3-state
- Latch-up performance: JESD 78 Class II exceeds 500 mA
- ESD protection:
 - HBM JESD-A114E exceeds 2000 V
 - CDM JESD22-C101C exceeds 1000 V
- Specified from -40 °C to +85 °C

3 Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74ABT162245ADL	-40 °C to +85 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1
74ABTH162245ADL				
74ABT162245ADGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74ABTH162245ADGG				

4 Functional diagram

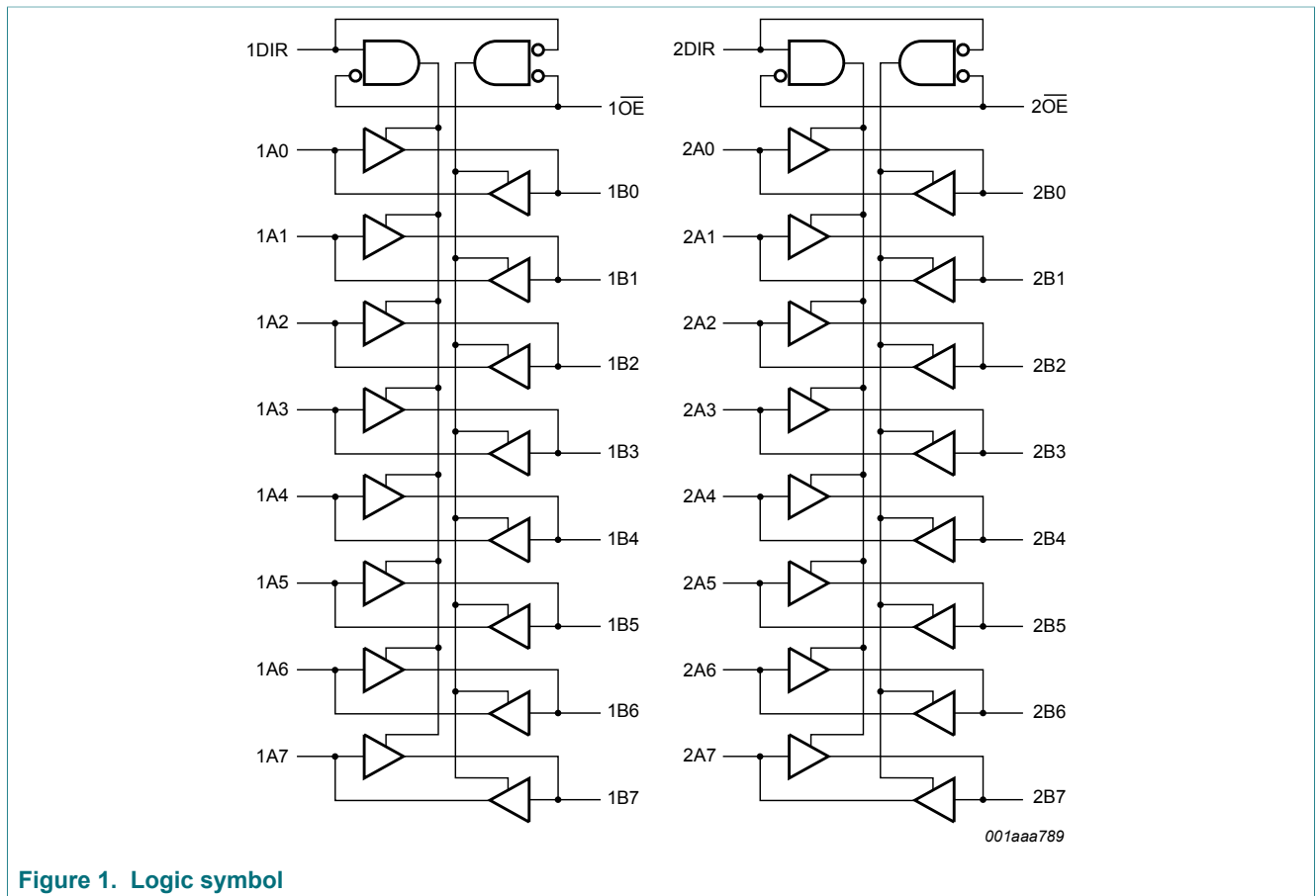


Figure 1. Logic symbol

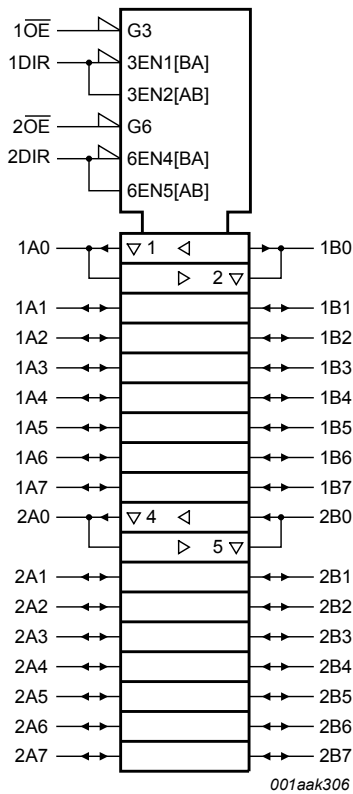


Figure 2. IEC logic symbol

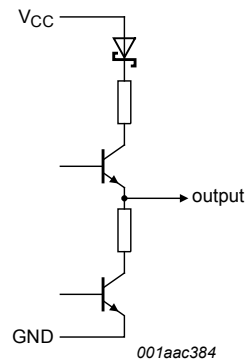


Figure 3. Schematic of each output

5 Pinning information

5.1 Pinning

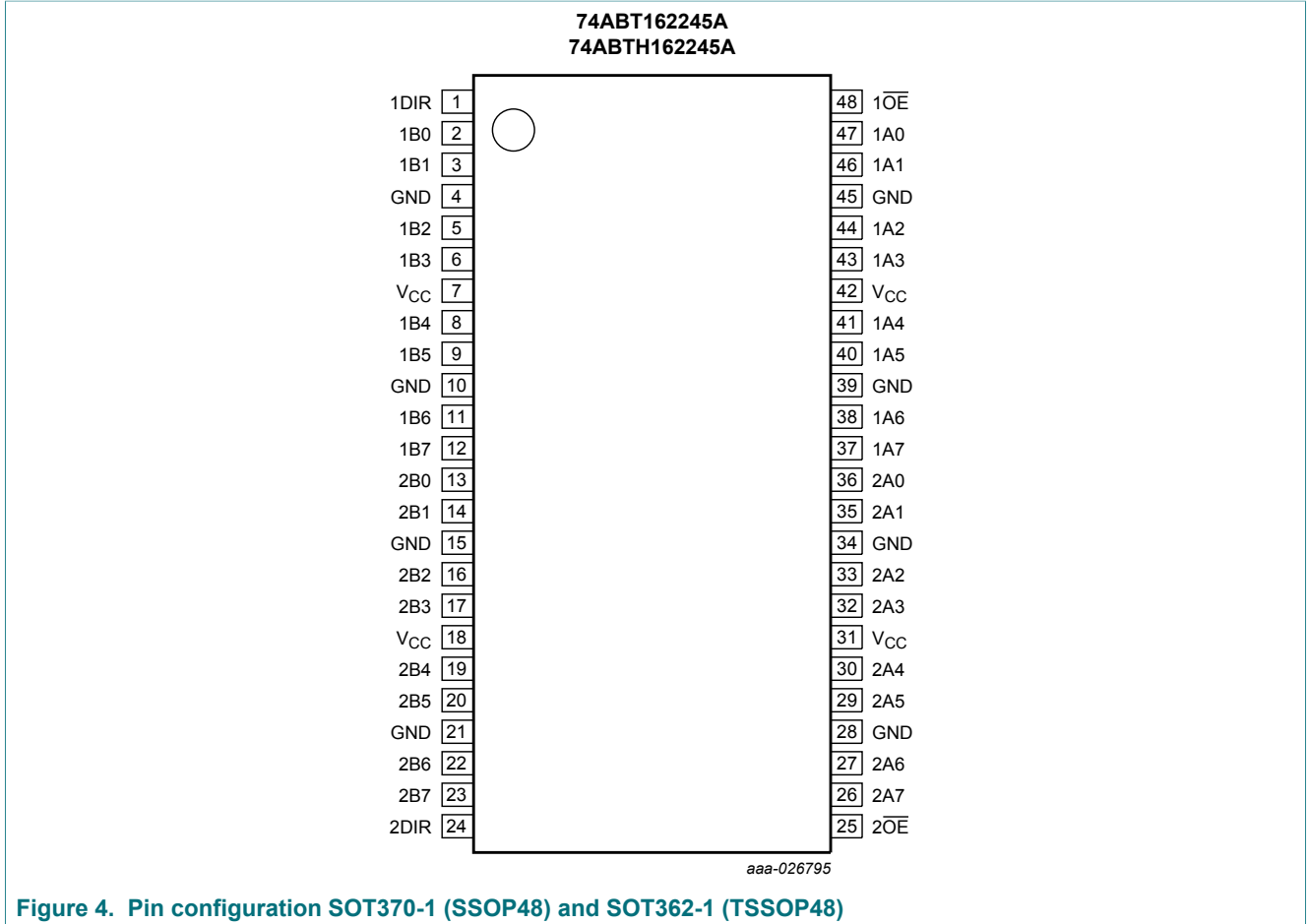


Figure 4. Pin configuration SOT370-1 (SSOP48) and SOT362-1 (TSSOP48)

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1DIR, 2DIR	1, 24	direction control input
1A0, 1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7	47, 46, 44, 43, 41, 40, 38, 37	data input/output
2A0, 2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7	36, 35, 33, 32, 30, 29, 27, 26	data input/output
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
1B0, 1B1, 1B2, 1B3, 1B4, 1B5, 1B6, 1B7	2, 3, 5, 6, 8, 9, 11, 12	data input/output
2B0, 2B1, 2B2, 2B3, 2B4, 2B5, 2B6, 2B7	13, 14, 16, 17, 19, 20, 22, 23	data input/output
1OE, 2OE	48, 25	output enable input
V _{CC}	7, 18, 31, 42	supply voltage

6 Functional description

Table 3. Function table ^[1]

Control		Input/output	
nOE	nDIR	nAn	nBn
L	L	output nAn = nBn	input
L	H	input	output nBn = nAn
H	X	Z	Z

- [1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
Z = high-impedance OFF-state.

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
V _I	input voltage		^[1] -1.2	+7.0	V
V _O	output voltage	output in OFF-state or HIGH-state	^[1] -0.5	+5.5	V
I _{IK}	input clamping current	V _I < 0 V	-18	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
I _O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
T _j	junction temperature		^[2] -	150	°C
T _{stg}	storage temperature		-65	+150	°C

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

- [2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

8 Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		4.5	-	5.5	V
V _I	input voltage		0	-	V _{CC}	V
I _{OH}	HIGH-level output current		-32	-	-	mA
I _{OL}	LOW-level output current		-	-	12	mA
$\Delta t/\Delta V$	input transition rise and fall rate		0	-	10	ns/V
T _{amb}	ambient temperature	in free air	-40	-	+85	°C

9 Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V _{IK}	input clamping voltage	V _{CC} = 4.5 V; I _{IK} = -18 mA	-1.2	-0.9	-	-1.2	-	V
V _{IH}	HIGH-level input voltage		2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage		-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _{CC} = 4.5 V; I _{OH} = -3 mA; V _I = V _{IL} or V _{IH}	2.5	2.9	-	2.5	-	V
		V _{CC} = 5.0 V; I _{OH} = -3 mA; V _I = V _{IL} or V _{IH}	3.0	3.4	-	3.0	-	V
		V _{CC} = 4.5 V; I _{OH} = -32 mA; V _I = V _{IL} or V _{IH}	2.0	2.4	-	2.0	-	V
V _{OL}	LOW-level output voltage	V _{CC} = 4.5 V; I _{OL} = 8 mA; V _I = V _{IL} or V _{IH}	-	0.46	0.65	-	0.65	V
		V _{CC} = 4.5 V; I _{OL} = 12 mA; V _I = V _{IL} or V _{IH}	-	0.5	0.8	-	0.8	V
I _I	input leakage current	n $\overline{\text{OE}}$, nDIR; V _{CC} = 5.5 V; V _I = GND or 5.5 V	-	±0.01	±1	-	±1	μA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O ≤ 4.5 V	-	±5.0	±100	-	±100	μA
I _{BHL}	bus hold LOW current	V _{CC} = 4.5 V; V _I = 0.8 V	[1] 50	-	-	50	-	μA
I _{BHH}	bus hold HIGH current	V _{CC} = 5.5 V; V _I = 2.0 V	[1] -75	-	-	-75	-	μA
I _{BHLO}	bus hold LOW overdrive current	V _{CC} = 5.5 V; V _I = 0 V to 5.5 V	[1] [2] 500	-	-	-	-	μA
I _{BHHO}	bus hold HIGH overdrive current	V _{CC} = 5.5 V; V _I = 0 V to 5.5 V	[1] [2] -500	-	-	-	-	μA
I _{O(pu/pd)}	power-up/ power-down output current	V _{CC} = 2.0 V; V _O = 0.5 V; V _I = GND or V _{CC} ; n $\overline{\text{OE}}$ = don't care	[3] -	±5.0	±50	-	±50	μA
I _{OZ}	OFF-state output current	V _{CC} = 5.5 V; V _I = V _{IL} or V _{IH}						
		V _O = 5.5 V	-	0.5	10	-	10	μA
		V _O = 0.0 V	-	-0.5	-10	-	-10	μA
I _{CEX}	output high leakage current	V _{CC} = 5.5 V; V _O = 5.5 V; V _I = GND or V _{CC}	-	5.0	50	-	50	μA
I _O	output current	V _{CC} = 5.5 V; V _O = 2.5 V	[4] -50	-92	-180	-50	-180	mA

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
I_{CC}	supply current	$V_{CC} = 5.5 \text{ V}$; $V_I = \text{GND}$ or V_{CC}						
		outputs HIGH	-	0.3	0.7	-	0.7	mA
		outputs LOW	-	10	19	-	19	mA
		outputs 3-state	-	0.3	0.7	-	0.7	mA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 5.5 \text{ V}$; one input at 3.4 V, other inputs at V_{CC} or GND ^[5]						
		outputs enabled	-	400	700	-	700	μA
		74ABT162245A; outputs 3-state	-	1.0	50	-	50	μA
		74ABTH162245A; outputs 3-state	-	100	250	-	250	μA
		$n\overline{\text{OE}}$, nDIR	-	400	700	-	700	μA
C_I	input capacitance	$V_I = 0 \text{ V}$ or V_{CC}	-	3	-	-	-	pF
$C_{I/O}$	input/output capacitance	$V_O = 0 \text{ V}$ or V_{CC} ; outputs 3-state	-	7	-	-	-	pF

[1] Valid for data inputs of bus hold parts only (74ABTH162245A)

[2] This is the bus hold overdrive current required to force the input to the opposite logic state.

[3] This parameter is valid for any V_{CC} between 0 V and 2.1 V with a transition time of up to 10 ms. From $V_{CC} = 2.1 \text{ V}$ to $V_{CC} = 4.5 \text{ V}$ to 5.5 V a transition time of 100 μs is permitted.

[4] Not more than one output should be tested at a time and the duration of the test should not exceed one second

[5] This is the increase in supply current for each input at 3.4 V.

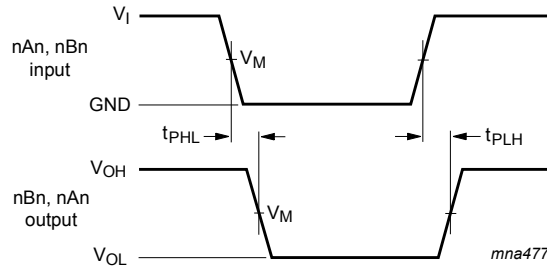
10 Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	$T_{\text{amb}} = 25 \text{ }^\circ\text{C}$; $V_{CC} = 5.0 \text{ V}$			$T_{\text{amb}} = -40 \text{ }^\circ\text{C}$ to $85 \text{ }^\circ\text{C}$; $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	LOW to HIGH propagation delay	nAn to nBn or nBn to nAn; see Figure 5	1.0	2.0	3.3	1.0	3.5	ns
t_{PHL}	HIGH to LOW propagation delay	nAn to nBn or nBn to nAn; see Figure 5	1.5	3.0	4.5	1.5	4.9	ns
t_{PZH}	OFF-state to HIGH propagation delay	$n\overline{\text{OE}}$ to nAn or nBn; see Figure 6	1.5	3.1	4.3	1.5	5.0	ns
t_{PZL}	OFF-state to LOW propagation delay	$n\overline{\text{OE}}$ to nAn or nBn; see Figure 6	2.0	5.0	6.1	2.0	7.0	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$n\overline{\text{OE}}$ to nAn or nBn; see Figure 6	1.7	3.5	4.8	1.7	5.4	ns
t_{PLZ}	LOW to OFF-state propagation delay	$n\overline{\text{OE}}$ to nAn or nBn; see Figure 6	1.5	3.2	4.5	1.5	4.9	ns

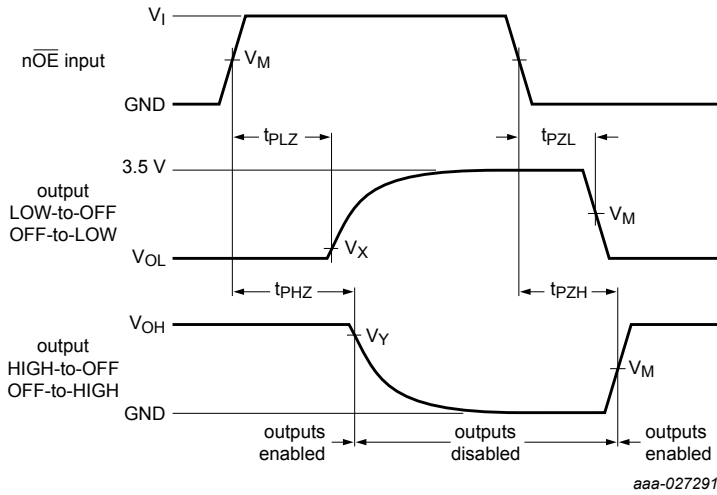
10.1 Waveforms and test circuit



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 5. Input (An or Bn) to output (Bn or An) propagation delays



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 6. 3-state output enable and disable times

Table 8. Measurement points

Input		Output		
V_I	V_M	V_M	V_X	V_Y
3.0 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$

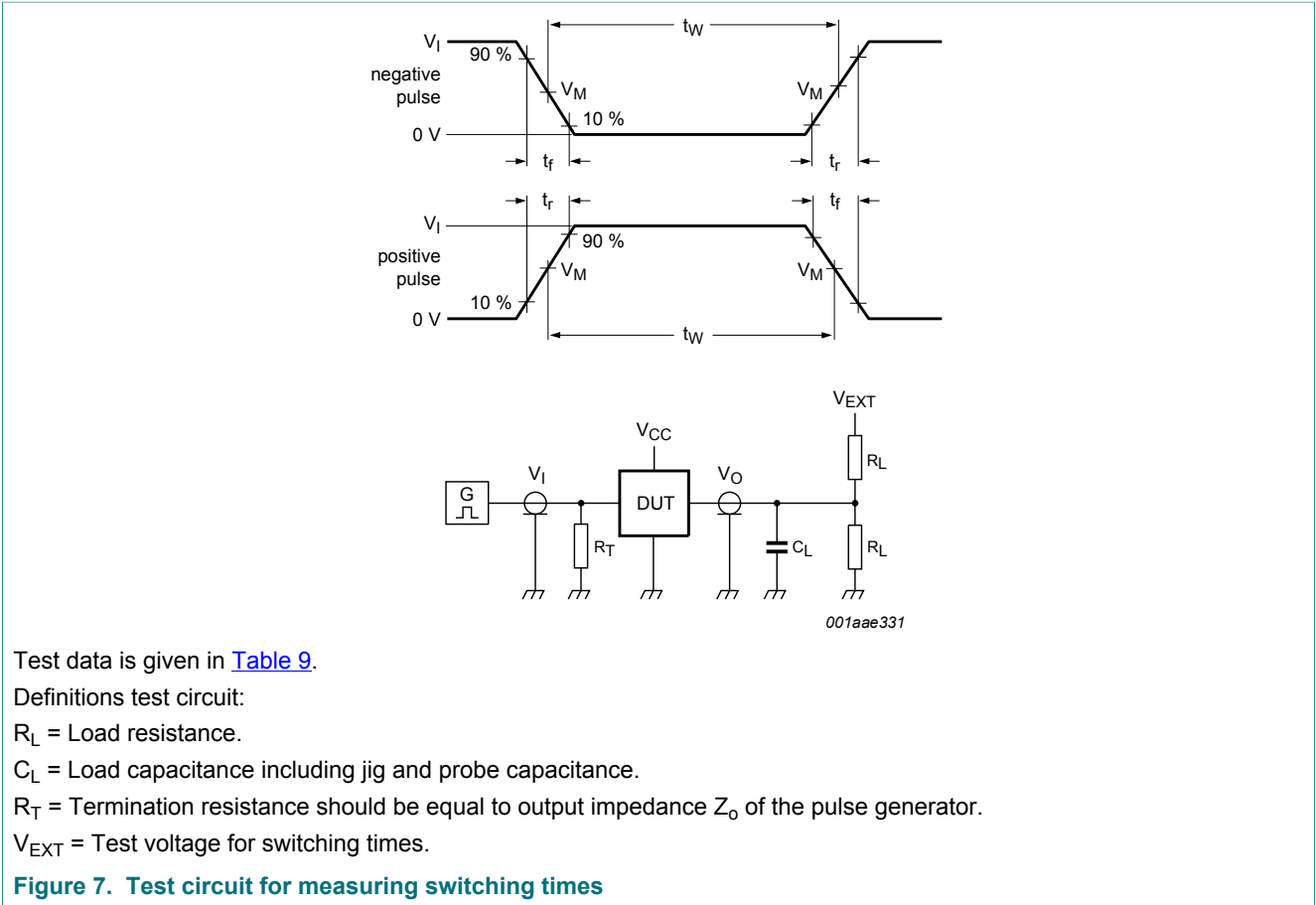


Table 9. Test data

Input				Load	V_{EXT}				
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}	
3.0 V	≤ 1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open	7 V	open	

11 Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1

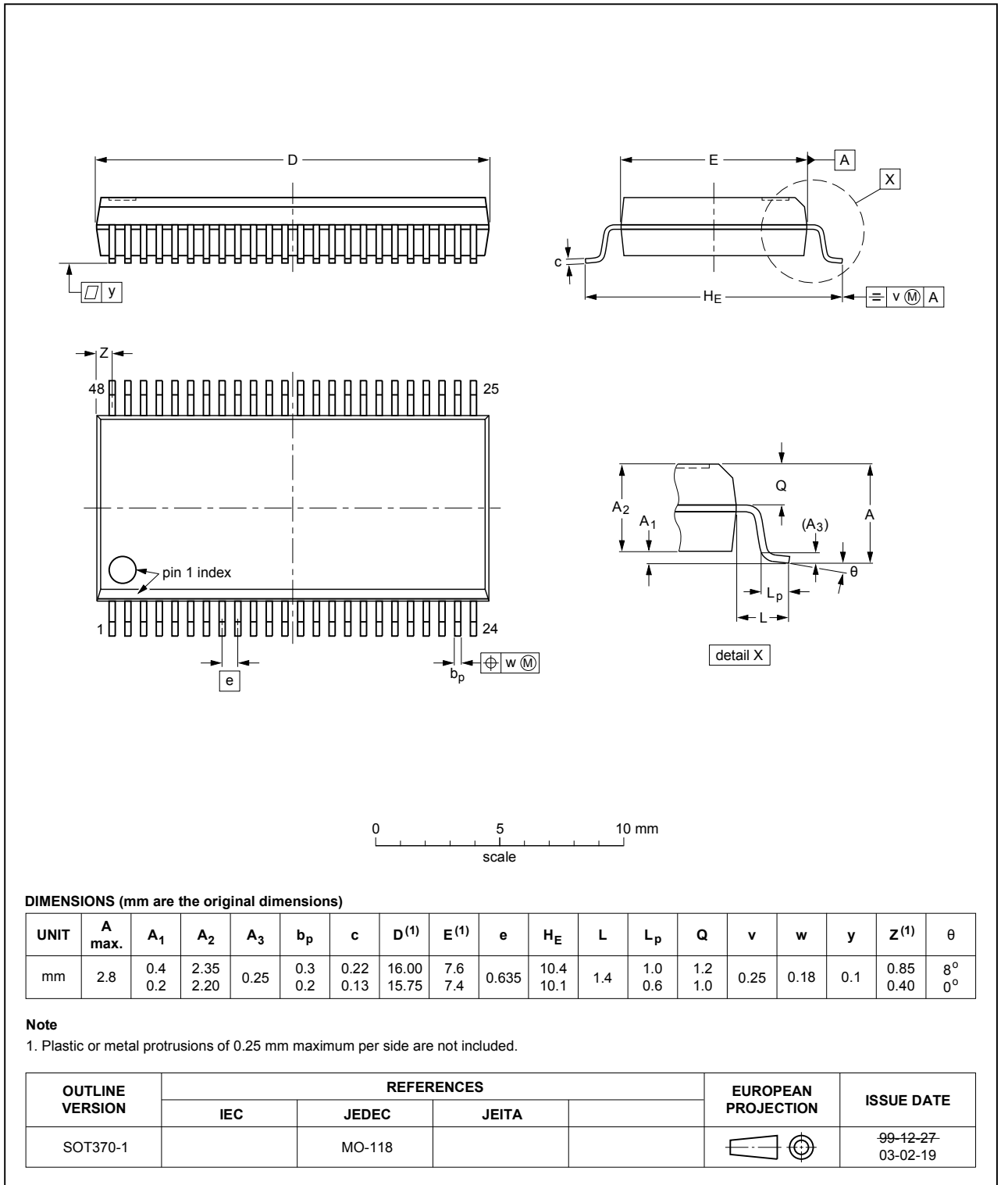


Figure 8. Package outline SOT370-1 (SSOP48)

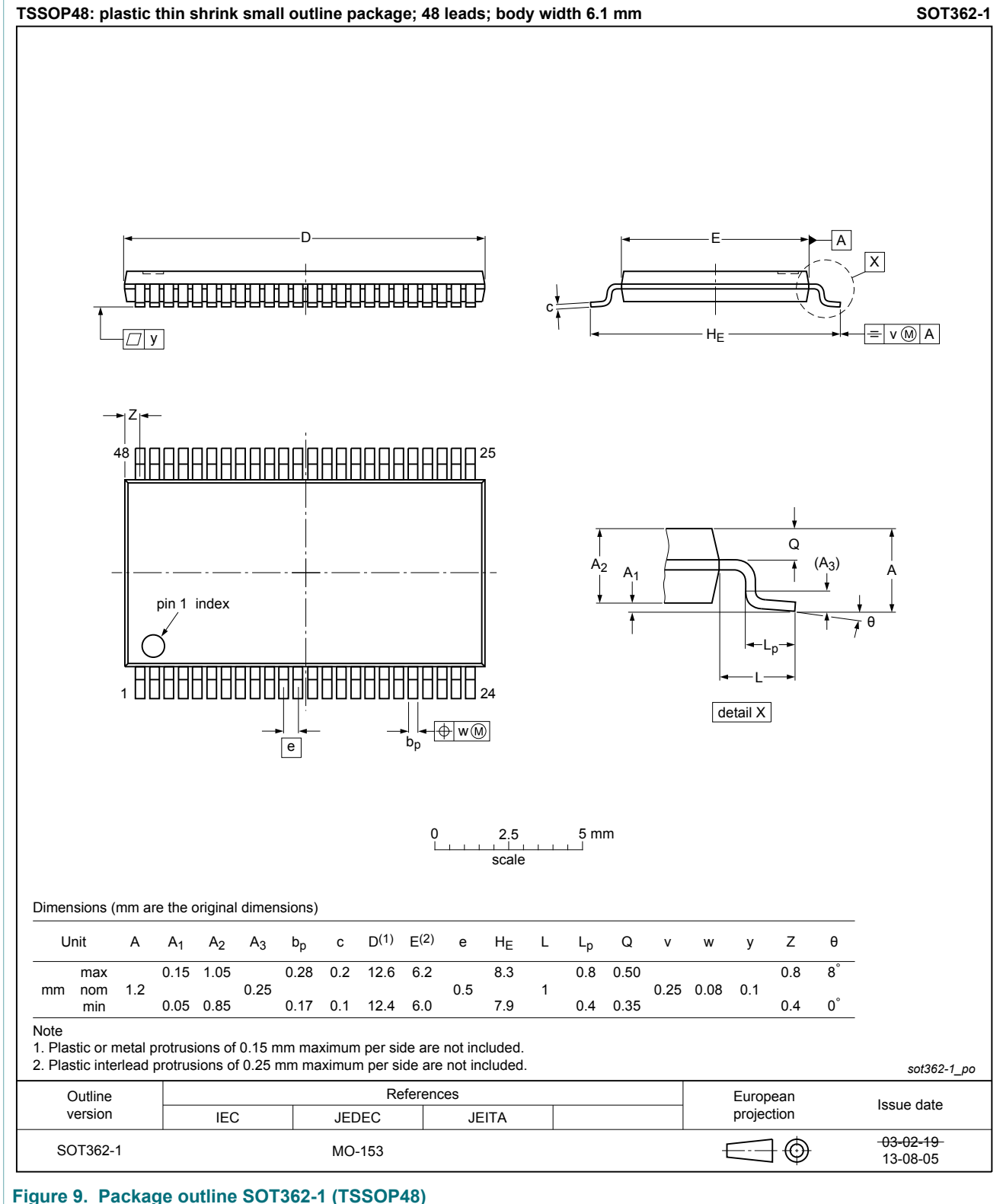


Figure 9. Package outline SOT362-1 (TSSOP48)

12 Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CDM	Charged Device Model
DUT	Device Under Test
HBM	Human Body Model
ESD	ElectroStatic Discharge

13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT_H162245A v.3	20170831	Product data sheet	-	74ABT_H162245A v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74ABT_H162245A v.2	19980225	Product specification	-	74ABT_H162245A v.1
74ABT_H162245A v.1	19961120	Product specification	-	-

14 Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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