

MC3405

Dual Operational Amplifier and Dual Comparator

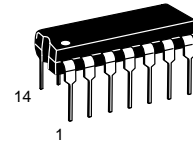
The MC3405 contains two differential-input operational amplifiers and two comparators, each set capable of single supply operation. This operational amplifier-comparator circuit fulfills its applications as a general purpose product for automotive and consumer circuits as well as an industrial building block.

The MC3405 is specified over the commercial operating temperature range of 0° to +70°C.

- Operational Amplifier Equivalent in Performance to MC3403
- Comparator Similar in Performance to LM339
- Single Supply Operation: 3.0 V to 36 V
- Split Supply Operation: ± 1.5 V to ± 18 V
- Low Supply Current Drain
- Operational Amplifier is Internally Frequency Compensated
- Comparator TTL and CMOS Compatible

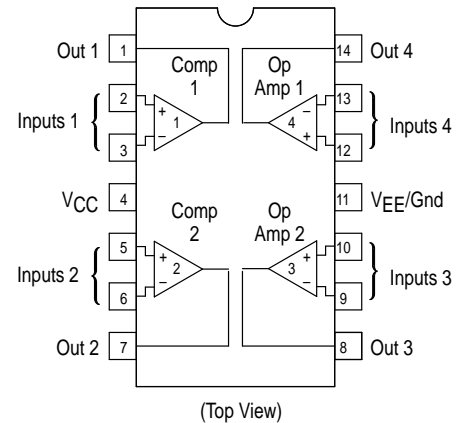
DUAL OPERATIONAL AMPLIFIER / DUAL VOLTAGE COMPARATOR

SEMICONDUCTOR TECHNICAL DATA

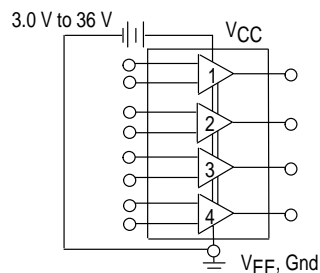


P SUFFIX
PLASTIC PACKAGE
CASE 646

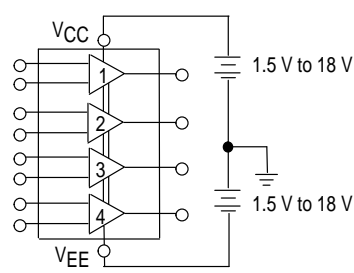
PIN CONNECTIONS



Single Supply



Split Supplies



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3405P	$T_A = 0^\circ$ to $+70^\circ\text{C}$	Plastic DIP

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OPERATIONAL AMPLIFIER SECTION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage – Single Supply Split Supplies	V_{CC} V_{CC}, V_{EE}	36 ± 18	Vdc
Input Differential Voltage Range	V_{IDR}	± 36	Vdc
Input Common Mode Voltage Range	V_{ICR}	± 18	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Operating Junction Temperature Range	T_J	150	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0$ V, $V_{EE} = \text{Gnd}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	–	2.0	10	mV
Input Offset Current	I_{IO}	–	30	50	nA
Input Bias Current	I_{IB}	–	-200	-500	nA
Large-Signal, Open Loop Voltage Gain ($R_L = 2.0$ k Ω)	A_{VOL}	20	200	–	V/mV
Power Supply Rejection	PSR	–	–	150	$\mu\text{V/V}$
Output Voltage Range (Note 1) ($R_L = 10$ k Ω , $V_{CC} = 5.0$ V) ($R_L = 10$ k Ω , 5.0 V $\leq V_{CC} \leq 30$ V)	V_{OR}	3.3 $V_{CC} - 2.0$	3.5 $V_{CC} - 1.7$	– –	V_{pp}
Power Supply Current (Notes 2 and 3)	I_{CC}	–	2.5	7.0	mA
Channel Separation, $f = 1.0$ kHz to 20 kHz (Input Referenced)	–	–	-120	–	dB

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15$ V, $V_{EE} = -15$ V, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($T_A = T_{low} + T_{high}$) (Note 4)	V_{IO}	– –	2.0 –	10 12	mV
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	15	–	$\mu\text{V}/^\circ\text{C}$
Input Offset Current ($T_A = T_{low}$ to T_{high}) (Note 4)	I_{IO}	– –	– –	50 200	nA
Input Bias Current ($T_A = T_{low}$ to T_{high}) (Note 4)	I_{IB}	– –	-200 –	-500 -800	nA
Input Common Mode Voltage Range	V_{ICR}	+13 $-V_{EE}$	–	–	Vdc
Large Signal, Open Loop Voltage Gain ($V_O = \pm 10$ V, $R_L = 2.0$ k Ω) ($T_A = T_{low}$ to T_{high}) (Note 4)	A_{VOL}	20 15	200 100	– –	V/mV
Common Mode Rejection	CMR	70	90	–	dB
Power Supply Rejection Ratio	PSRR	–	30	150	$\mu\text{V/V}$
Output Voltage ($R_L = 10$ k Ω) ($R_L = 2.0$ k Ω) ($R_L = 2.0$ k Ω , $T_A = T_{low}$ to T_{high}) (Note 4)	V_O	± 12 ± 10 ± 10	± 13.5 ± 13 –	– – –	Vdc
Output Short Circuit Current	I_{SC}	± 10	± 20	± 45	mA
Power Supply Current (Notes 2 and 3)	I_{CC}, I_{EE}	–	2.8	7.0	mA
Phase Margin	ϕ_m	–	60	–	Degrees
Small-Signal Bandwidth ($A_V = 1$, $R_L = 10$ k Ω , $V_O = 50$ mV)	BW	–	1.0	–	MHz

- NOTES:**
- Output will swing to ground.
 - Not to exceed maximum package power dissipation.
 - For operational amplifier and comparator.
 - $T_{low} = 0^\circ\text{C}$, $T_{high} = +70^\circ\text{C}$

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ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Bandwidth ($A_V = 1$, $R_L = 2.0\text{ k}\Omega$, $V_O = 20\text{ V}_{pp}$, THD = 5%)	BWp	–	9.0	–	kHz
Rise Time/Fall Time	t_{TLH} , t_{THL}	–	0.35	–	μs
Overshoot ($A_V = 1$, $R_L = 10\text{ k}\Omega$, $V_O = 50\text{ mV}$)	os	–	20	–	%
Slew Rate	SR	–	0.6	–	$\text{V}/\mu\text{s}$

COMPARATOR SECTION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage – Single Supply Split Supplies	V_{CC} V_{CC} , V_{EE}	36 ± 18	Vdc
Input Differential Voltage Range	V_{IDR}	± 36	Vdc
Input Common Mode Voltage Range	V_{ICR}	–0.3 to +36	Vdc
Sink Current	I_{Sink}	20	mA
Operating Ambient Temperature Range	T_A	0 to +70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	–55 to +125	$^\circ\text{C}$
Operating Junction Temperature Range	T_J	150	$^\circ\text{C}$

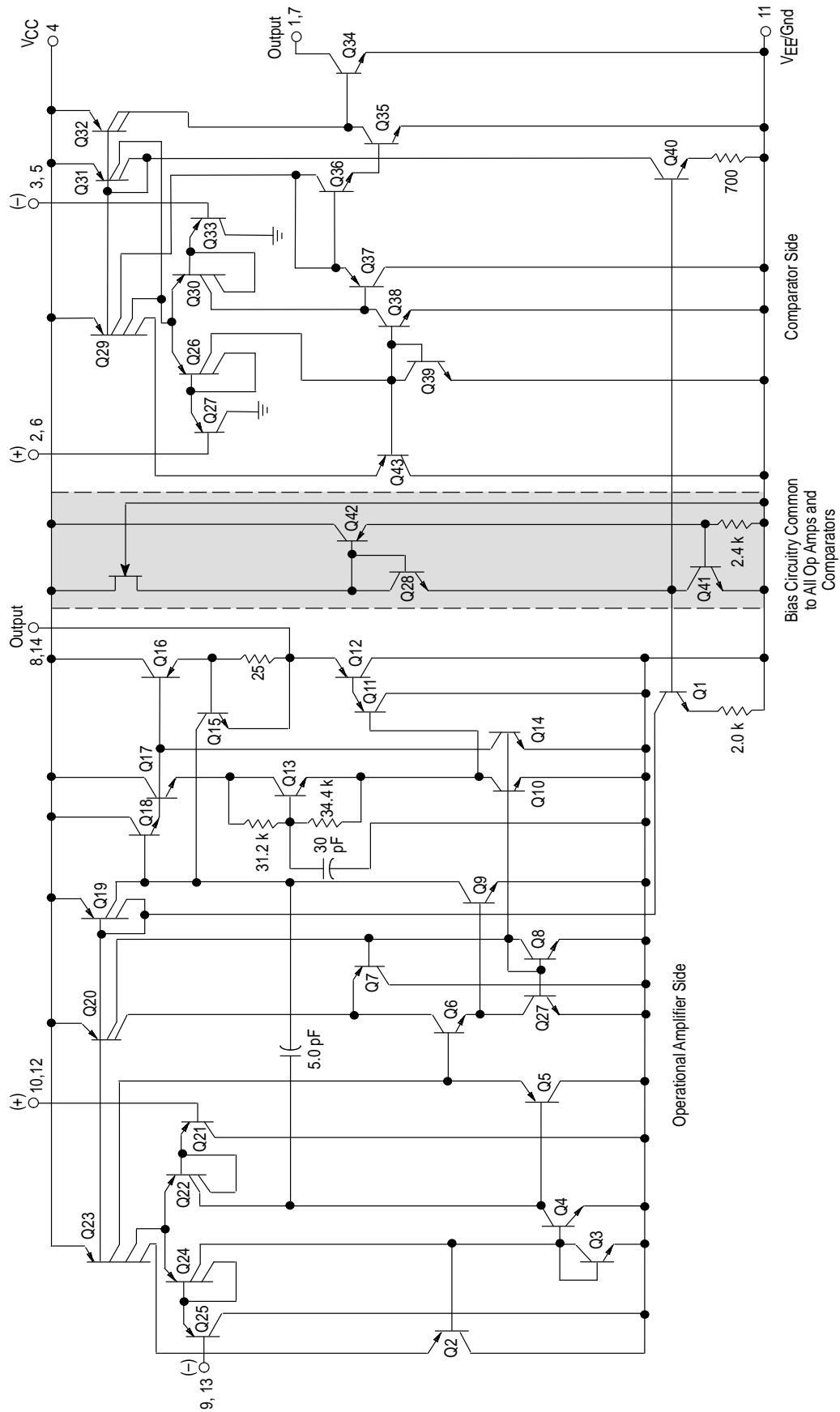
ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $V_{EE} = \text{Gnd}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($T_A = T_{low}$ to T_{high}) (Notes 1 and 2)	V_{IO}	– –	2.0 –	10 12	mV
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	15	–	$\mu\text{V}/^\circ\text{C}$
Input Offset Current ($T_A = T_{low}$ to T_{high}) (Note 1)	I_{IO}	– –	50 –	100 200	nA
Input Bias Current ($T_A = T_{low}$ to T_{high}) (Note 1)	I_{IB}	– –	–125 –	–500 –800	nA
Input Common Mode Voltage Range ($T_A = T_{low}$ to T_{high}) (Note 1)	V_{ICR}	0 0	$V_{CC} - 1.5$ $V_{CC} - 1.7$	$V_{CC} - 1.7$ $V_{CC} - 2.0$	Vpp
Input Differential Voltage (All $V_{in} \geq 0\text{ Vdc}$)	V_{ID}	–	–	36	V
Large-Signal, Open Loop Voltage Gain ($R_L = 15\text{ k}\Omega$)	A_{VOL}	–	200	–	V/mV
Output Sink Current ($-V_{in} \geq 1.0\text{ Vdc}$, $+V_{in} = 0$, $V_O \leq 1.5\text{ V}$)	I_{Sink}	6.0	16	–	mA
Low Level Output Voltage ($+V_{in} = 0\text{ V}$, $-V_{in} = 1.0\text{ V}$, $I_{Sink} = 4.0\text{ mA}$) ($T_A = T_{low}$ to T_{high}) (Note 1)	V_{OL}	– –	350 –	500 700	μA
Output Leakage Current ($+V_{in} \geq 1.0\text{ Vdc}$, $-V_{in} = 0$, $V_O = 5.0\text{ Vdc}$) ($T_A = T_{low}$ to T_{high}) (Note 1)	I_{OL}	– –	0.1 0.1	1.0 1.0	μA
Large-Signal Response	–	–	300	–	ns
Response Time (Note 3) ($V_{RL} = 5.0\text{ Vdc}$, $R_L = 5.1\text{ k}\Omega$)	–	–	1.3	–	μs

- NOTES:** 1. $T_{low} = 0^\circ\text{C}$, $T_{high} = +70^\circ\text{C}$
 2. $V_O \cong 1.4\text{ V}$, $R_S = 0\ \Omega$ with V_{CC} from 5.0 Vdc to 30 Vdc, and over the input common mode range 0 to $V_{CC} - 1.7\text{ V}$.
 3. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals 300 ns is typical.

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Representative Schematic Diagram
(1/2 of Circuit Shown)



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OPERATIONAL AMPLIFIER SECTION

Figure 1. Sine Wave Response

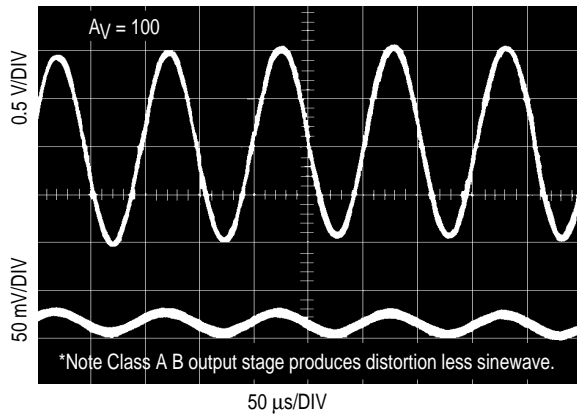


Figure 2. Open Loop Frequency Response

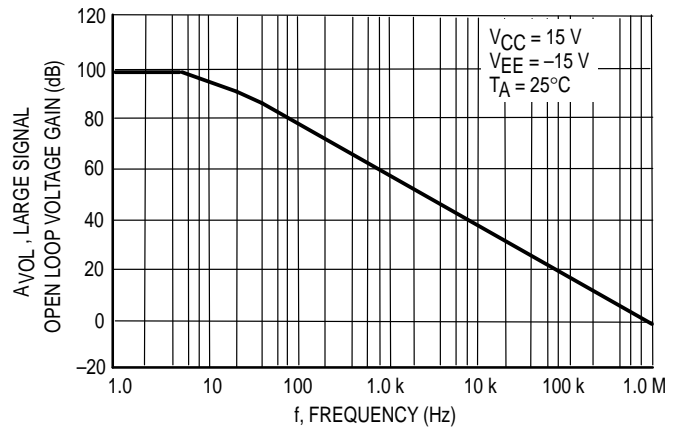


Figure 3. Power Bandwidth

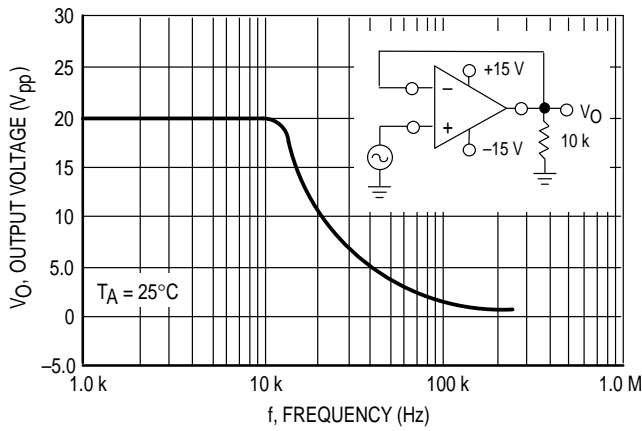


Figure 4. Output Swing versus Supply Voltage

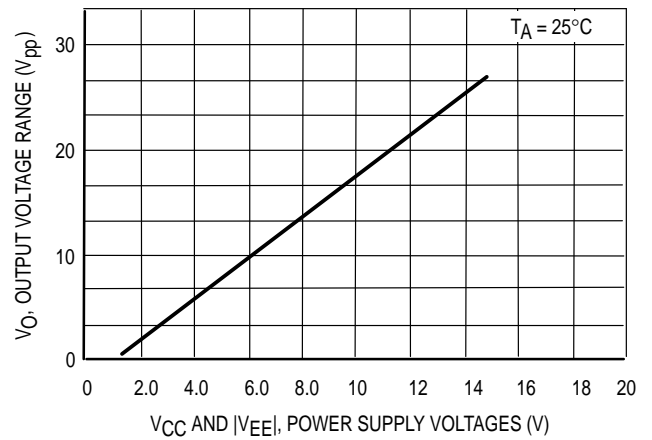


Figure 5. Input Bias Current versus Temperature

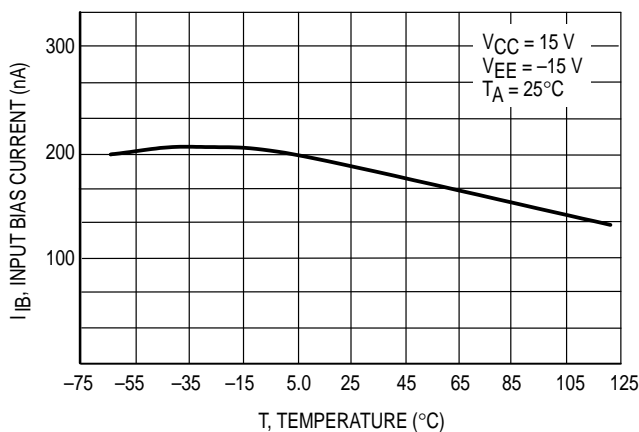
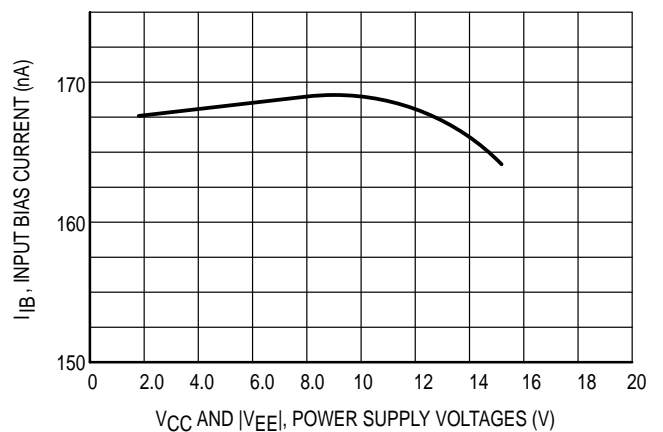


Figure 6. Input Bias Current versus Supply Voltage



COMPARATOR SECTION

Figure 7. Normalized Input Offset Voltage

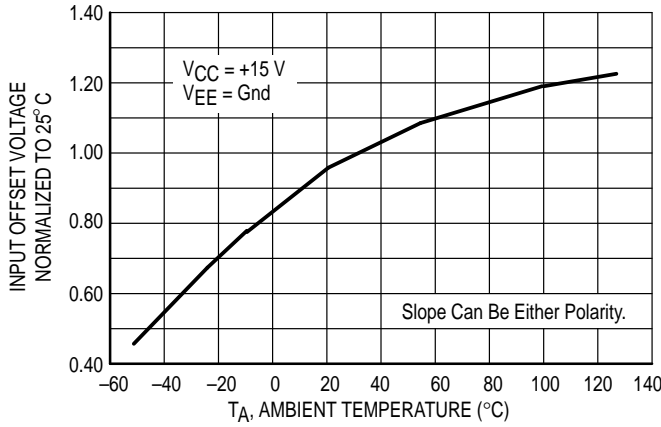


Figure 8. Input Bias Current

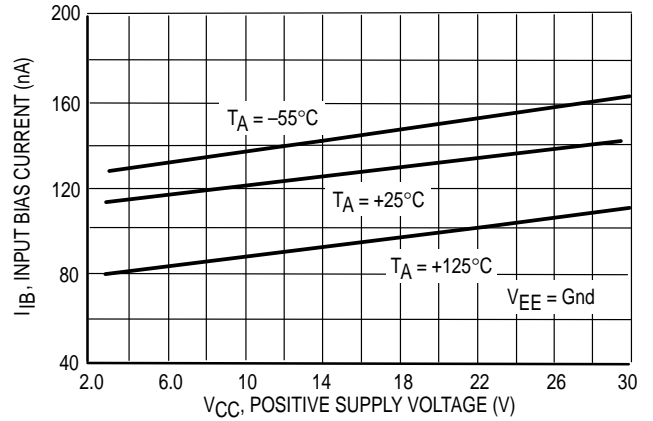


Figure 9. Normalized Input Offset Current

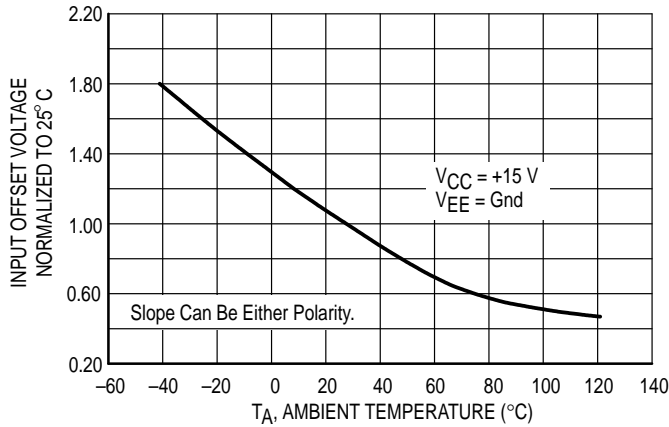


Figure 10. Output Sink Current versus Output Voltage

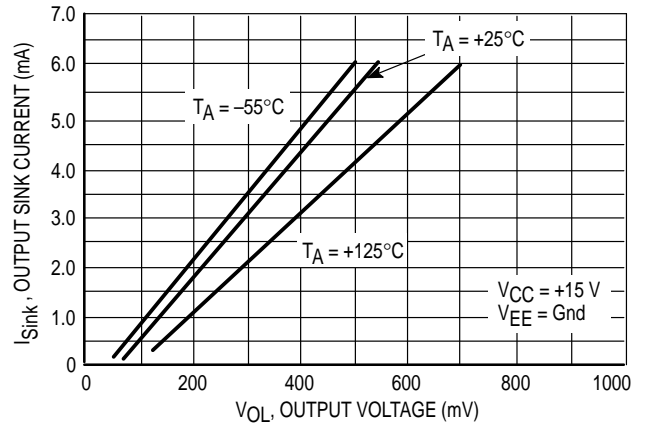
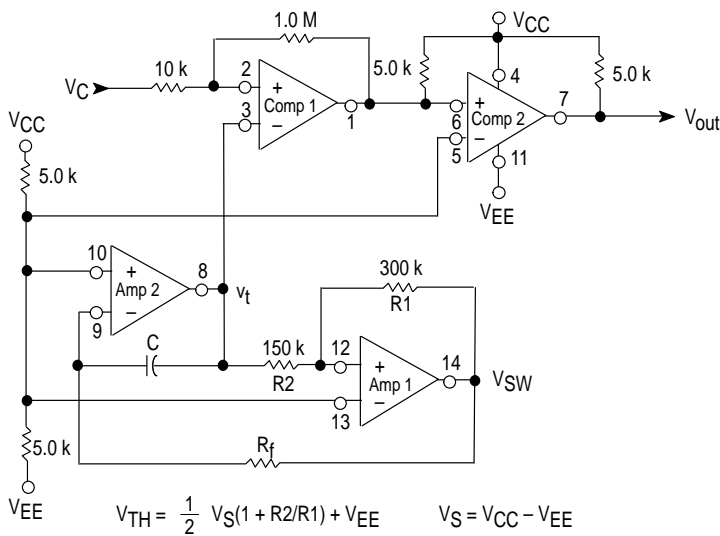


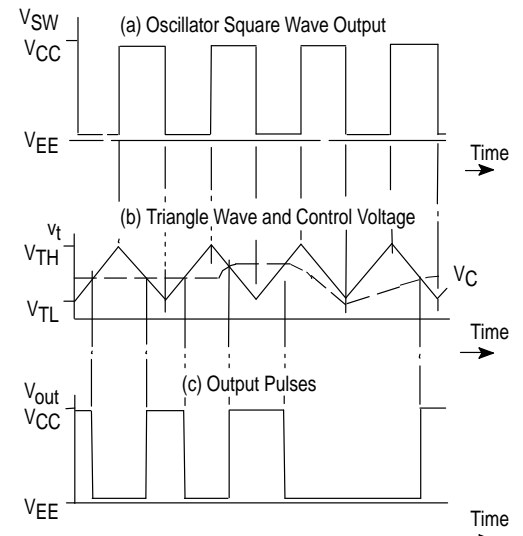
Figure 11. Pulse Width Modulator Schematic and Waveforms



$$V_{TH} = \frac{1}{2} V_S(1 + R_2/R_1) + V_{EE} \quad V_S = V_{CC} - V_{EE}$$

$$V_{TL} = \frac{1}{2} V_S(1 - R_2/R_1) + V_{EE}$$

$$\text{Oscillator Frequency } f = \frac{R_1}{4R_fCR_2}$$



$$\text{Pulse Width} = \left(\frac{1}{f} \right) \left(\frac{V_C - V_{TL}}{V_{TH} - V_{TL}} \right) \text{ when: } V_{TL} < V_C < V_{TH}$$

$$\text{Duty Cycle in \%} = \left(\frac{V_C - V_{TL}}{V_{TH} - V_{TL}} \right) (100)$$

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Figure 12. Window Comparator

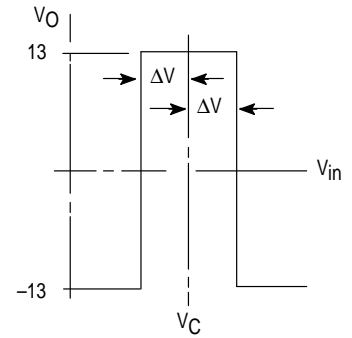
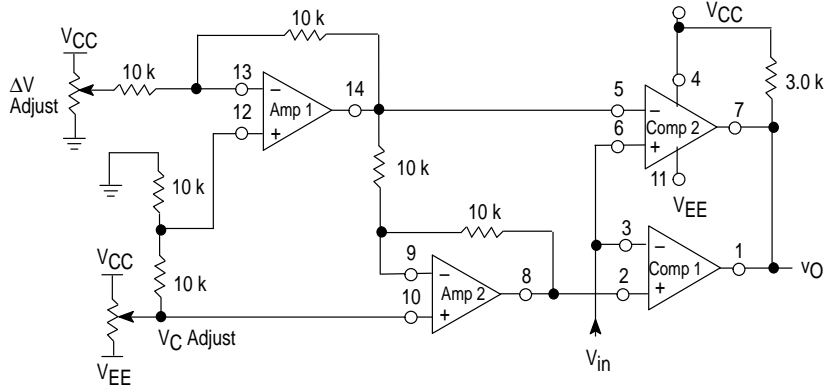


Figure 13. Squelch Circuit for AM or FM

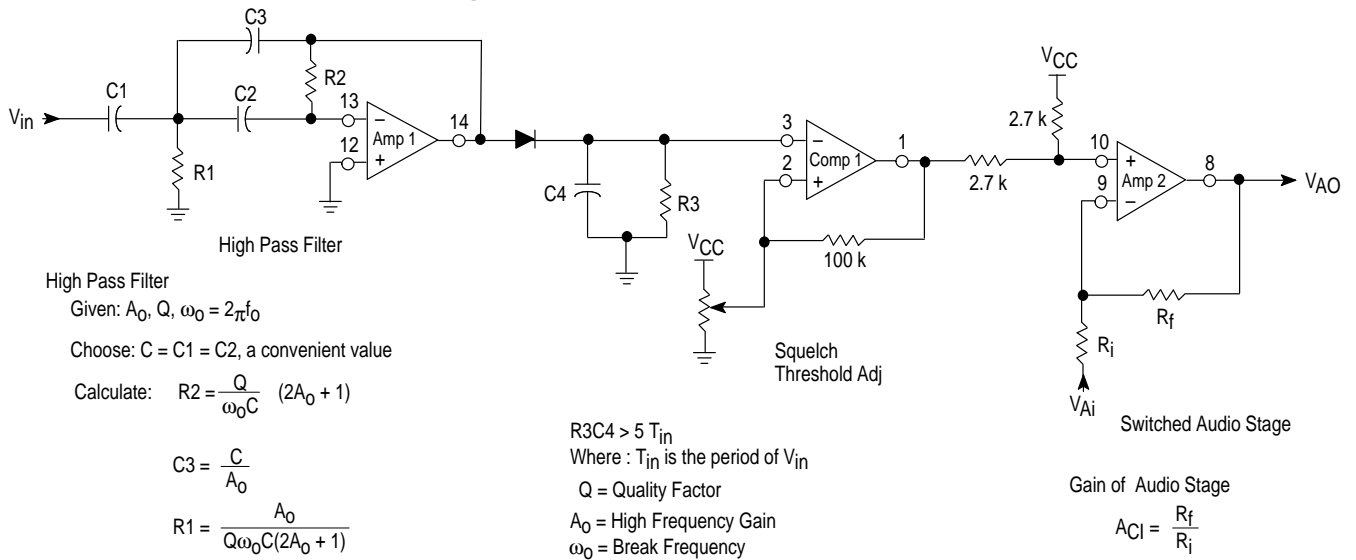
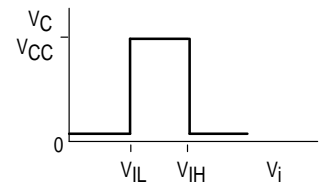
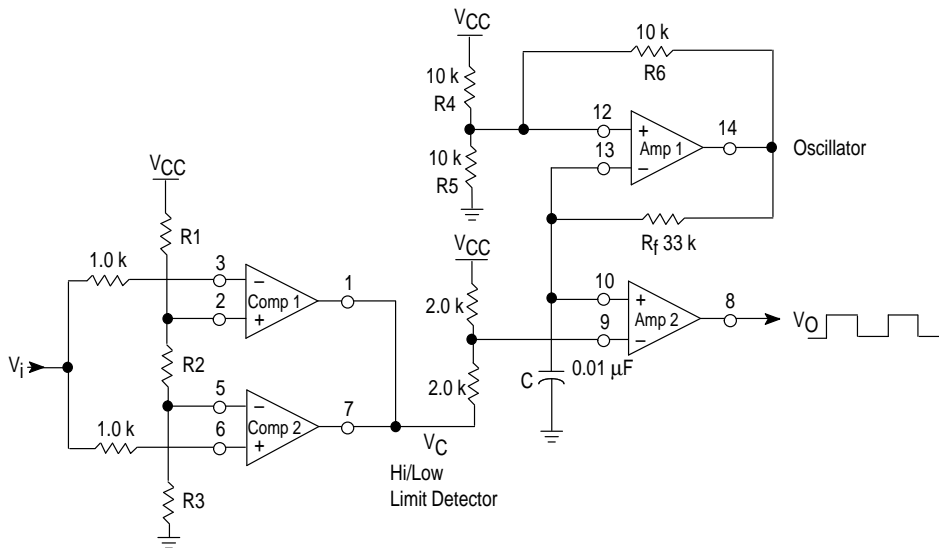


Figure 14. High/Low Limit Alarm



$$V_{IL} = V_{CC} \frac{R_3}{R_1 + R_2 + R_3}$$

$$V_{IH} = V_{CC} \frac{R_2 + R_3}{R_1 + R_2 + R_3}$$

Oscillator

If $R4 = R5 = R6$

$$f = 0.72/R_f C$$

As shown, $f = 2.2 \text{ kHz}$

V_O will oscillate if $V_{IH} < V_i$, or $V_{IL} > V_i$

V_O will be low if $V_{IL} < V_i < V_{IH}$

Figure 15. Zero Crossing Detector with Temperature Sensor

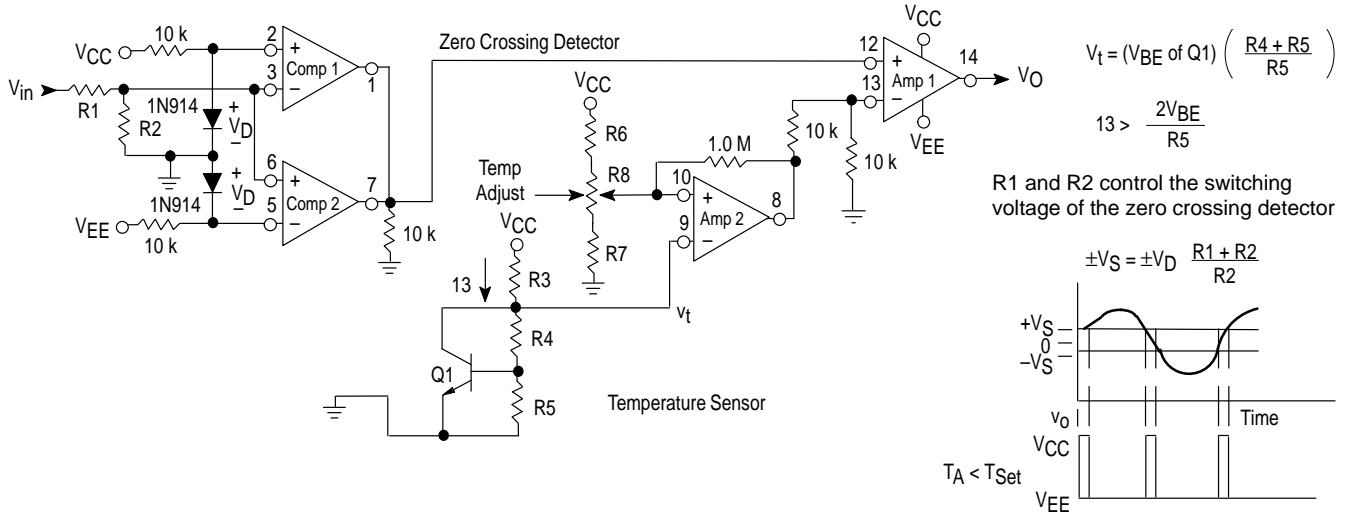
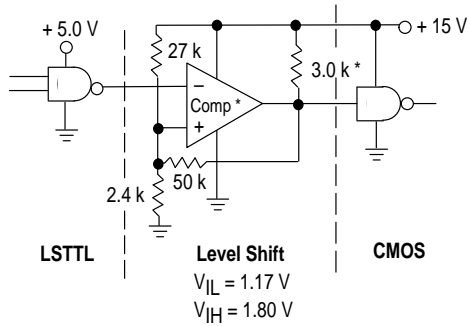
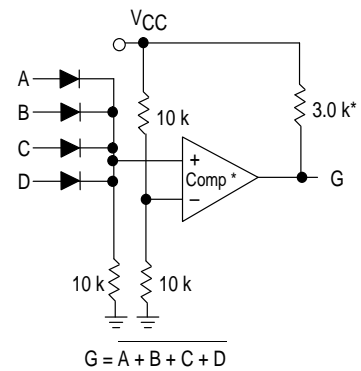


Figure 16. LSTTL to CMOS Interface with Hysteresis



* The same configuration may be used with an op amp if the 3.0 k resistor is removed.

Figure 17. NOR Gate

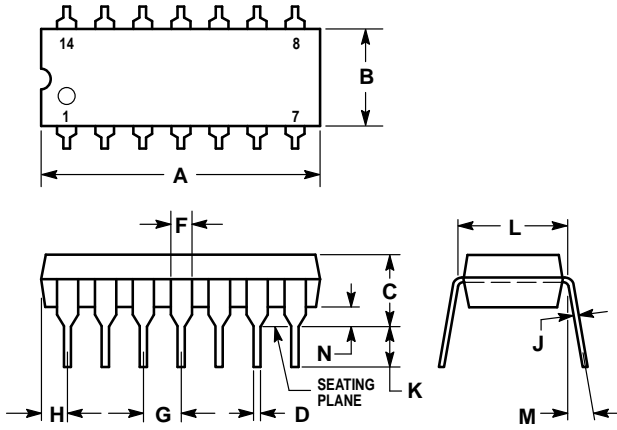


* The same configuration may be used with an op amp if the 3.0 k resistor is removed.

MC3405

OUTLINE DIMENSIONS

P SUFFIX
PLASTIC PACKAGE
 CASE 646-06
 ISSUE L



NOTES:

1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

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