Order this document
by MC68HC05F5AD/D

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC68HC05F5

Addendum to
MC68HC05F5
HCMOS Microcontroller Unit
Technical Data

This addendum adds information to *MC68HC05F5 Technical Data* (Motorola document number MC68HC05F5/D) as follows:

Page 1-1, **SECTION 1 GENERAL DESCRIPTION**, the following data replaces the second paragraph:

From: On-chip memory of the MC68HC05F5 includes 5632 bytes of user ROM and 224 bytes of user RAM.

To: On-chip memory of the MC68HC05F5 includes 5744 bytes of user ROM and 224 bytes of user RAM.

Page 1-1, **1.1 Features**, the following data replaces the third and eighth bulleted MCU features:

From: 5632 Bytes of User ROM including 8 Locations for User Vectors

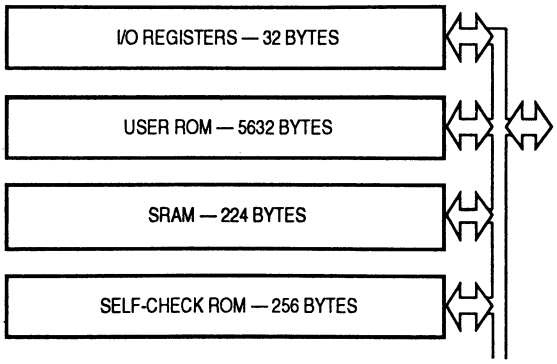
To: 5744 Bytes of User ROM including 12 Locations for User Vectors

From: Fully Static Operation with no Minimum Clock Speed

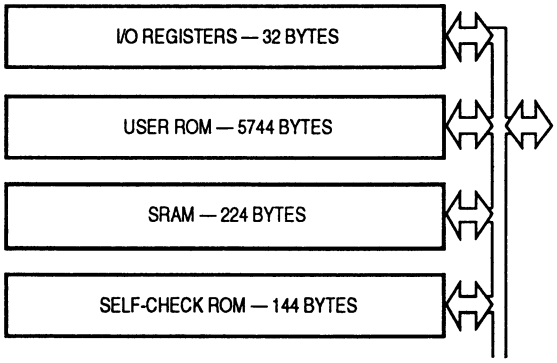
To: Fully Static Operation with no Minimum Clock Speed (**Digital Section Only**)

Page 1-3, **Figure 1-1. MC68HC05F5 Block Diagram**, correct as follows:

From:

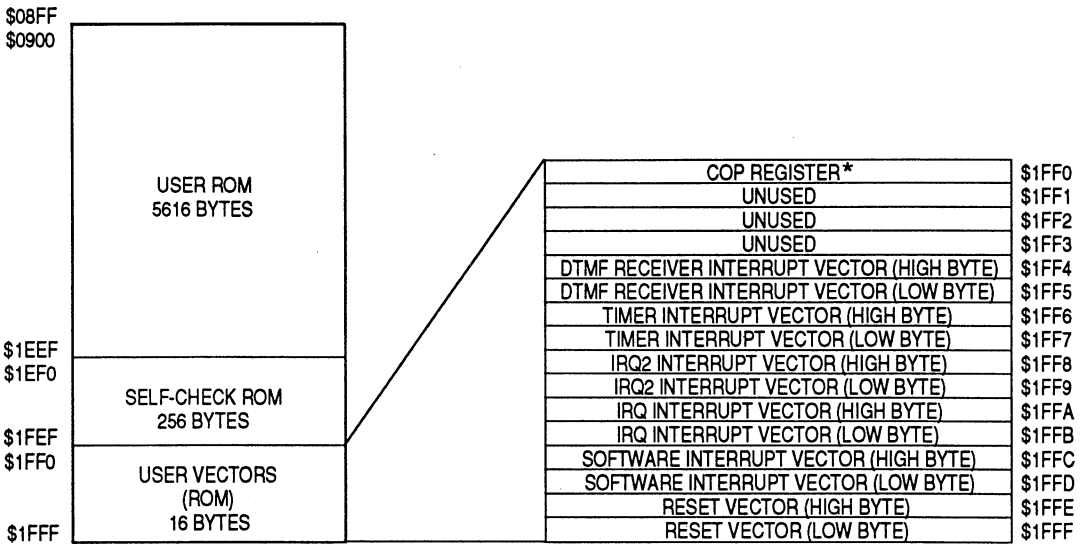


To:

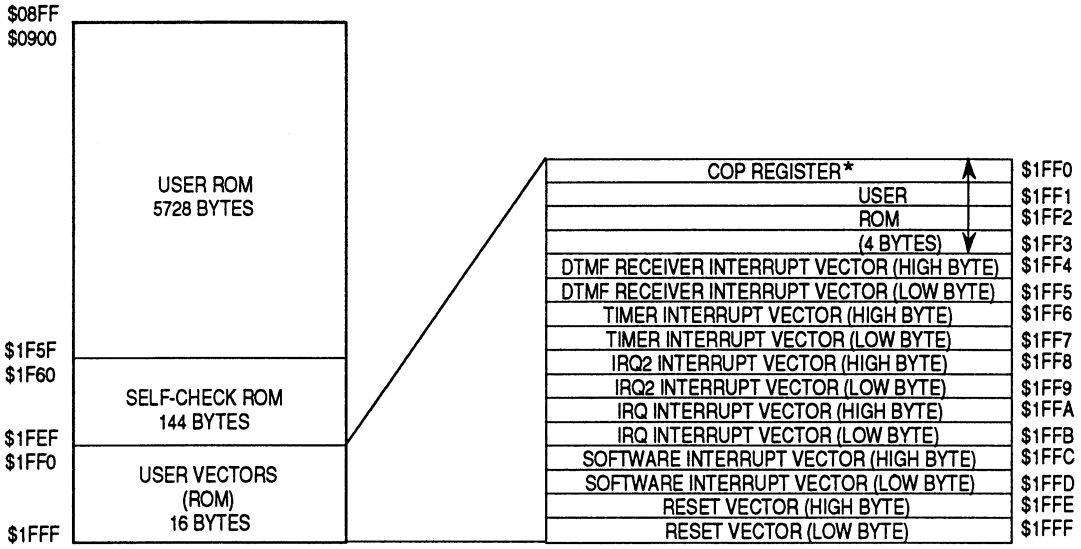


Page 2-2, **Figure 2-1. Memory Map**, correct as follows:

From:



To:



Page 2-4, **2.4 ROM**, correct as follows:

From:

The memory map includes the following three ROM sections:

- $0900–$1EEF — 5616 bytes of user ROM
- $1EF0–$1FEF — 256 bytes reserved for self-check ROM
- $1FF0–$1FFF — 16 bytes reserved for interrupt and reset vectors.

To:

The memory map includes the following three ROM sections:

- $0900–$1F5F — 5616 bytes of user ROM
- $1F60–$1FEF — 144 bytes reserved for self-check ROM
- $1FF0–$1FFF — 16 bytes reserved for interrupt and reset vectors.

Pages 8-2 to 8-3, **8.1 Timer Status and Control Register (TSCR)**, correct as follows:

From:

	Bit 7	6	5	4	3	2	1	Bit 0
	TOF	RTIF	TOIE	RTIE	TOFR	RTIFR	RT1	RT0
RESET:	0	0	0	0	U	U	1	1

To:

	Bit 7	6	5	4	3	2	1	Bit 0
	TOF	RTIF	TOIE	RTIE	0	0	RT1	RT0
RESET:	0	0	0	0	—	—	1	1

From:

TOF — Timer Overflow Flag

Clear TOF by writing a logic one to the TOFR bit.

To:

TOF — Timer Overflow Flag

Clear TOF by writing a logic zero to the TOF bit.

From:

RTIF — Real-Time Interrupt Flag

Clear RTIF by writing a logic one to the RTIFR bit.

To:

RTIF — Real-Time Interrupt Flag

Clear RTIF by writing a logic zero to the RTIF bit.

From:

TOFR — Timer Overflow Flag Reset

Writing a logic one to this write-only bit clears the TOF bit. TOFR always reads as logic zero.

To: [DELETED]

From:

RTIFR — Real-Time Interrupt Flag Reset

Setting this write-only bit clears the RTIF bit. RTIFR always reads as logic zero.

To: [DELETED]

Page 9-1, **9.1 DTMF Receiver Operation**, add the following note after **Figure 9-1. DTMF Keypad**:

NOTE

The DTMF receiver is designed to operate at internal bus speeds of 2.0 MHz **only**. The CLK bit in the DTMF Receiver Control Register (see **Figure 9-5. DTMF Receiver Control Register (DCR)**) is a provision for future digital bus speeds of 4.0 MHz.

Page 10-1, **10.1 Self-Check Tests**, correct as follows:

From:

To check for proper MCU operation, the self-check ROM performs the following tests:

- I/O test — A functional exercise of ports A, B, C, and D
- RAM test — A complement test of each RAM byte
- Timer test — A test of the counter register and the TOF and RTIF flags
- ROM test — An exclusive OR odd parity check
- DTMF test — A test of DTMF digital logic
- Interrupt test — A test of external and timer interrupts

To:

To check for proper MCU operation, the self-check ROM performs the following tests:

- RAM test — A complement test of each RAM byte
- ROM test — An exclusive OR odd parity check
- DTMF test — A test of DTMF digital logic
- Interrupt test — A test of external and timer interrupts

Page 10-1, **10.2 Self-Check Results**, correct Table 10-1 as follows:

From:

Table 10-1. Self-Check Circuit LED Codes

PC3	PC2	PC1	PC0	Problem
ON	ON	ON	OFF	I/O FAILURE
ON	ON	OFF	ON	RAM FAILURE
ON	ON	OFF	OFF	TIMER FAILURE
ON	OFF	ON	ON	ROM FAILURE
ON	OFF	ON	OFF	DTMF LOGIC FAILURE
ON	OFF	OFF	ON	INTERRUPT FAILURE
ON	Flashing			NO FAILURES
All Others				DEVICE FAILURE

NOTES:

1. With no DTMF signal applied to the A_{IN} pin, the LEDs display the self-check code continuously.
2. With a DTMF signal applied to the A_{IN} pin, the LEDs periodically pause the self-check code display to display the DTMF receiver data code for about one second. (See Table 9-1.)

To:

Table 10-1. Self-Check Circuit LED Codes

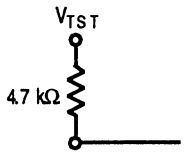
PC3	PC2	PC1	PC0	Problem
ON	ON	ON	OFF	RAM FAILURE
ON	ON	OFF	ON	ROM FAILURE
ON	ON	OFF	OFF	DTMF LOGIC FAILURE
ON	OFF	ON	ON	INTERRUPT FAILURE
ON	Flashing			NO FAILURES
All Others				DEVICE FAILURE

NOTES:

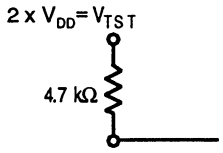
1. With no DTMF signal applied to the A_{IN} pin, the LEDs display the self-check code continuously.
2. With a DTMF signal applied to the A_{IN} pin, the LEDs periodically pause the self-check code display to display the DTMF receiver data code for about one second. (See Table 9-1.)

Page 10-3, **10.3 Self-Check Circuit**, correct as follows:

From:



To:



From:

1. Apply V_{TST} to the $\overline{IRQ}$ pin.

To:

1. Apply V_{TST} = 2 x V_{DD} to the $\overline{IRQ}$ pin.

Page 12-3, **Table 12-3. DC Electrical Characteristics (V_{DD} = 5.0 Vdc)** contains new values for the supply current:

From:

Supply Current (See NOTES.)					
Run	I_{DD}	—	1.8	TBD	mA
Wait		—	550	TBD	µA
Stop					
25 °C		—	2	TBD	µA
0 to +70 °C (Standard)		—	4	TBD	µA
-40 to +85 °C (Extended)			5	TBD	µA

To:

Supply Current (See NOTES.)					
Run	I_{DD}	—	1.8	5	mA
Wait		—	0.5	2	mA
Stop					
25 °C		—	2	5	µA
0 to +70 °C (Standard)		—	4	9	µA
-40 to +85 °C (Extended)			5	10	µA

Page 12-3, **Table 12-3. DC Electrical Characteristics (V_{DD} = 5.0 Vdc)** contains new values for the analog supply current:

From:

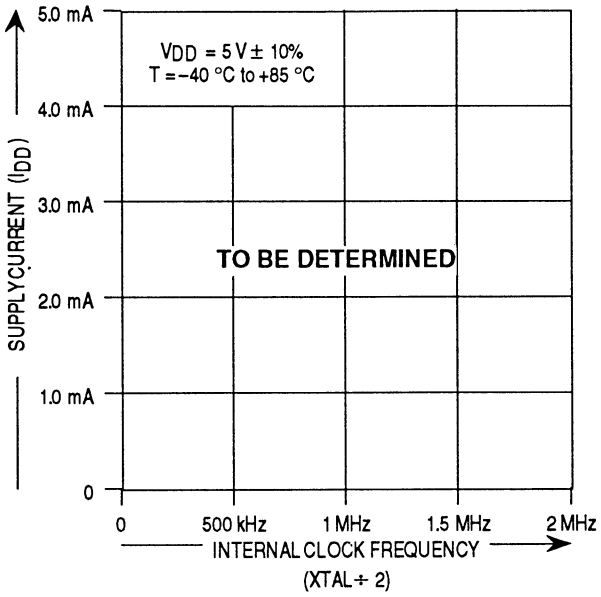
Analog Supply Current					
25 °C	AI_{DD}	—	5	—	mA
-40 to +85 °C		—	5.5	—	mA

To:

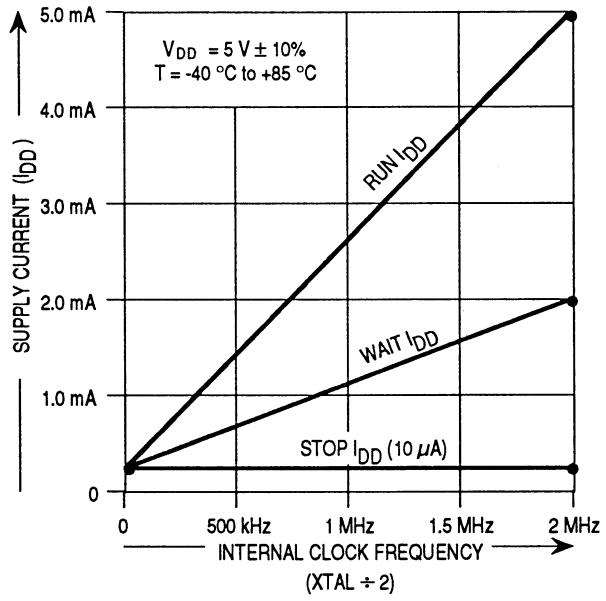
Analog Supply Current					
25 °C	AI_{DD}	—	5	6	mA
-40 to +85 °C		—	5.5	6.5	mA

Page 12-5, **Figure 12-5. Maximum Supply Current vs Clock Frequency**, correct as follows:

From:



To:



Page 12-6, **Table 12-4. Analog Characteristics**, correct as follows:

From:

Characteristic	Min	Typ	Max	Unit
Signal Level for Detection, A_{IN} (NOTE 2)	-35	—	-2	dBm
Twist (High Tone/Low Tone)	-10	—	10	dB
Frequency Detect Bandwidth (NOTES 3, 4)	+(1.5 + 2 Hz)	±2.3	—	% of F_0
60 Hz Tolerance	—	—	0.8	V rms
Dial Tone Tolerance (Dial Tone 330+440; NOTE 5)	—	—	0	dB
Noise Tolerance (NOTES 5, 6, 7)	—	—	-12	dB
Power Supply Noise (Wide Band)	—	—	TBD	mV p-p
Talk Off (NOTE 7)	—	TBD	—	Hits

NOTES:
1. V_{DD} = 5.0 Vdc ± 10%; V_{SS} = 0 Vdc; T_a = -40 °C to +85 °C unless otherwise noted.
2. Z = 600 Ω.
3. F_0 is the center frequency of the bandpass filters.
4. Referenced to lower amplitude tone.
5. Bandwidth limited (0 to 3.4 kHz) Gaussian noise.
6. Using Mitel Tape #CM7290.

To:

Characteristic	Min	Typ	Max	Unit
Signal Level for Detection, A_{IN} (NOTE 2)	-32	—	-2	dBm
Twist (High Tone/Low Tone) (NOTE 4)	-10	—	10	dB
Frequency Detect Bandwidth (NOTE 3)	+(1.5 + 2 Hz)	±2.3	—	% of F_0
60 Hz Tolerance	—	—	0.8	V rms
Dial Tone Tolerance (Dial Tone 330+440; NOTE 5)	—	—	0	dB
Noise Tolerance (NOTES 4, 5, 6)	—	—	-12	dBc
Talk Off (NOTE 6)	—	TBD	—	Hits

NOTES:
1. V_{DD} = 5.0 Vdc ± 10%; V_{SS} = 0 Vdc; f_{OSC} = 4.0 MHz; T_a = -40 °C to +85 °C unless otherwise noted.
2. Z = 600 Ω.
3. F_0 is the center frequency of the bandpass filters.
4. Referenced to lower amplitude tone.
5. Bandwidth limited (0 to 3.4 kHz) Gaussian noise.
6. Using Mitel Tape #CM7290.

Page 12-7, **Table 12-5. DTMF Receiver Timing**, correct as follows:

From:

Receiver Propagation Delay	t_{PROP}	—	TBD	—	ms

NOTE: V_{DD} = 5.0 Vdc ±10%; V_{SS} = 0 Vdc; T_A = –40 °C to +85 °C unless otherwise noted.

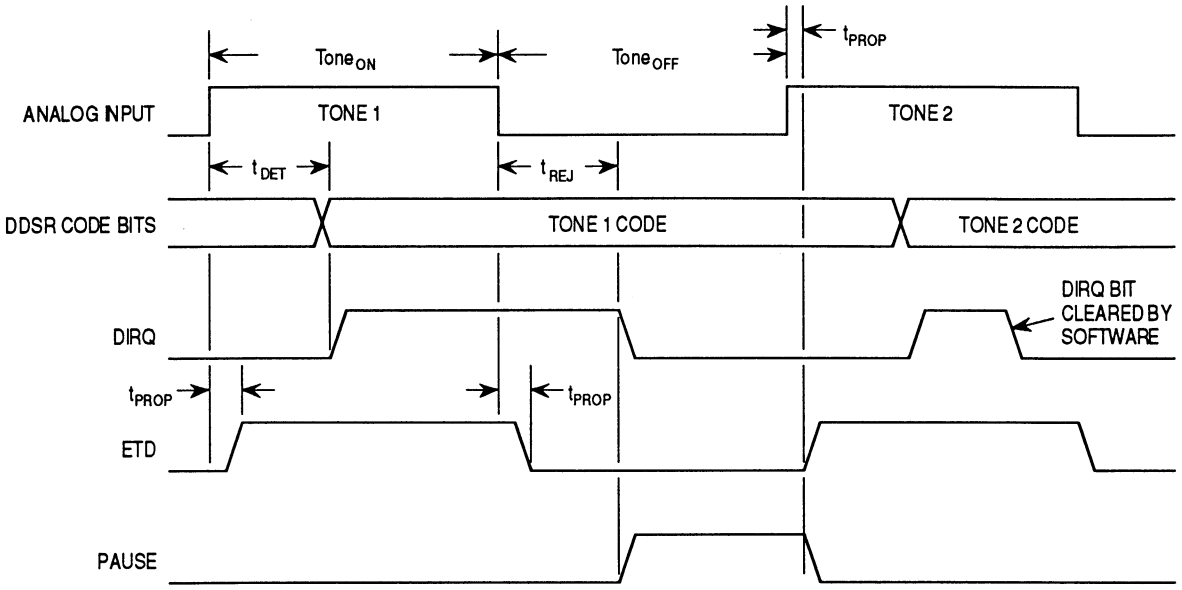
To:

Receiver Propagation Delay	t_{PROP}	—	12	—	ms

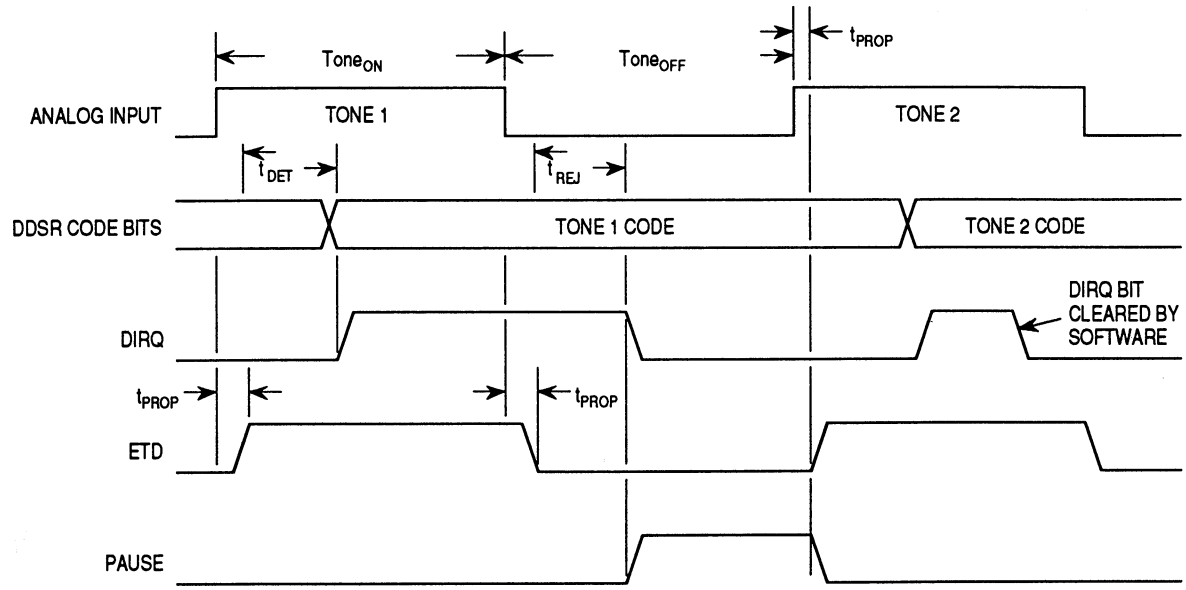
NOTE: V_{DD} = 5.0 Vdc ±10%; V_{SS} = 0 Vdc; f_{OSC} = 4.0 MHz; T_A = –40 °C to +85 °C unless otherwise noted.

Page 12-7, **Figure 12-7. DTMF Receiver Timing**, correct as follows:

From:



To:



Order this document
by MC68HC05F5AD/D

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC68HC05F5

Addendum to
MC68HC05F5
HCMOS Microcontroller Unit
Technical Data

This addendum adds information to *MC68HC05F5 Technical Data* (Motorola document number MC68HC05F5/D) as follows:

Page 1-1, **SECTION 1 GENERAL DESCRIPTION**, the following data replaces the second paragraph:

From: On-chip memory of the MC68HC05F5 includes 5632 bytes of user ROM and 224 bytes of user RAM.

To: On-chip memory of the MC68HC05F5 includes 5744 bytes of user ROM and 224 bytes of user RAM.

Page 1-1, **1.1 Features**, the following data replaces the third and eighth bulleted MCU features:

From: 5632 Bytes of User ROM including 8 Locations for User Vectors

To: 5744 Bytes of User ROM including 12 Locations for User Vectors

From: Fully Static Operation with no Minimum Clock Speed

To: Fully Static Operation with no Minimum Clock Speed (**Digital Section Only**)