



MOTOROLA

PLL FREQUENCY SYNTHESIZERS

The MC145104, MC145107, MC145109, and MC145112 are phase locked loop (PLL) frequency synthesizer parts constructed with CMOS devices on a single monolithic structure. These synthesizers find applications in such areas as CB and FM transceivers. The device contains an oscillator/amplifier, a 2¹⁰ or 2¹¹ divider chain for the oscillator signal, a programmable divider chain for the input signal and a phase detector. The MC145104/5112 have circuitry for a 10.24 MHz oscillator or may operate with an external signal. The MC145107/5109 require the external reference signal. Several of the circuits provide a 5.12 MHz output signal, which can be used for frequency tripling. A 2⁹ (MC145109/5112) or 2⁸ (MC145104/5107) programmable divider divides the input signal frequency for channel selection. The inputs to the programmable divider are standard ground-to-supply binary signals. Pull-down resistors on these inputs normally set these inputs to ground enabling these programmable inputs to be controlled from a mechanical switch or electronic circuitry.

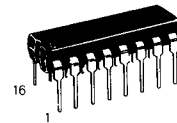
The phase detector may control a VCO and yields a high level signal when input frequency is low, and a low level signal when input frequency is high. An out of lock signal provided from the on-chip lock detector with a "0" level for the out of lock condition.

- Single Power Supply
- Wide Supply Range: 4.5 to 12 V
- 16 or 18 Pin Plastic Packages
- 10.24 MHz Oscillator on Chip
- 5.12 MHz Output
- Programmable Division Binary Input Selects up to 2⁹
- On-Chip Pull Down Resistors on Programmable Divider Inputs
- Selectable Reference Divider, 2¹⁰ or 2¹¹

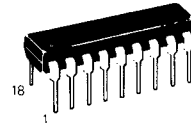
**MC145104
MC145107
MC145109
MC145112**

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)
**PLL
FREQUENCY SYNTHESIZERS**



**P SUFFIX
PLASTIC PACKAGE
CASE 648**



**P SUFFIX
PLASTIC PACKAGE
CASE 707**

**NOT RECOMMENDED FOR NEW DESIGNS
PRODUCT BEING PHASED OUT**

Closest equivalent is the MC145106

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq V_{in}$ or $V_{out} \leq V_{DD}$.

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