

HIGH PERFORMANCE	40	45	50	60
Max. $\overline{\text{RAS}}$ Access Time, (t_{RAC})	40 ns	45 ns	50 ns	60 ns
Max. Column Address Access Time, (t_{CAA})	20 ns	22 ns	24 ns	30 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	15 ns	17 ns	19 ns	27 ns
Min. Read/Write Cycle Time, (t_{RC})	75 ns	80 ns	90 ns	110 ns

Features

- 128K x 16-bit organization
- EDO Page Mode for a sustained data rate of 67 MHz
- $\overline{\text{RAS}}$ access time: 40, 45, 50, 60 ns
- Dual $\overline{\text{CAS}}$ Inputs
- Low Power Dissipation
- Read-Modify-Write, $\overline{\text{RAS}}$ -Only Refresh, $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh
- Refresh Interval: 512 cycles/8ms
- Available in 40-pin 400 mil SOJ and 40/44L-pin 400 mil TSOP-II packages
- Single +5V \pm 10% Power Supply
- TTL Interface

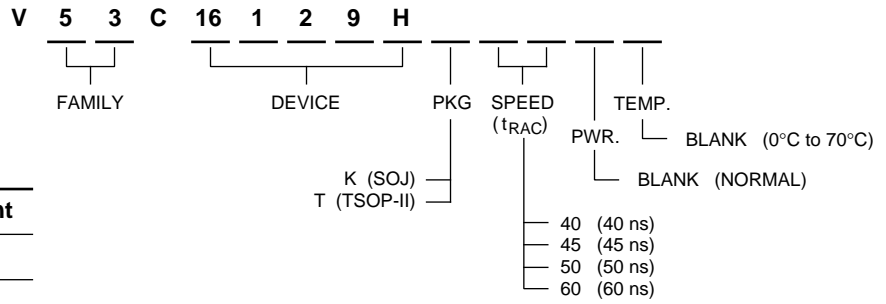
Description

The V53C16129H is a 131,072 x 16 bit high-performance CMOS dynamic random access memory. The V53C16129H offers Page mode with Extended Data Output. EDO Page Mode operation allows random access up to 512 x 16 bits, within a page, with cycle times as short as 15 ns. An address, $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ input capacitances are reduced to minimize the loading. The V53C16129H has asymmetric address 8-bit row and 9-bit column.

All inputs are TTL compatible. The V53C16129H is best suited for graphics, and DSP applications requiring high performance memories.

Device Usage Chart

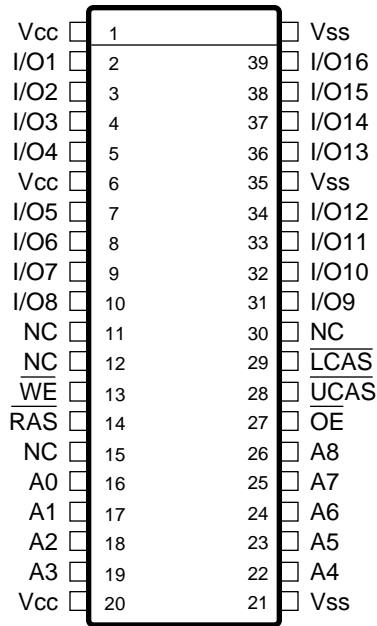
Operating Temperature Range	Package Outline		Access Time (ns)				Power	Temperature Mark
	K	T	40	45	50	60	Std.	
0°C to 70°C	•	•	•	•	•	•	•	Blank



Description	Pkg.	Pin Count
SOJ	K	40
TSOP-II	T	40/44L

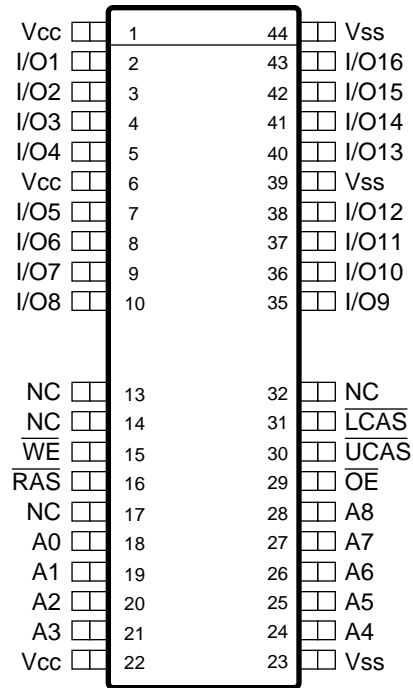
16129H-01

**40-Pin Plastic SOJ
PIN CONFIGURATION
Top View**



16129H-02

**40/44L-Pin Plastic TSOP-II
PIN CONFIGURATION
Top View**



16129H-03

Pin Names

A ₀ -A ₈	Address Inputs
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{UCAS}}$	Column Address Strobe/Upper Byte Control
$\overline{\text{LCAS}}$	Column Address Strobe/Lower Byte Control
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
I/O ₁ -I/O ₁₆	Data Input, Output
V _{CC}	+5V Supply
V _{SS}	0V Supply
NC	No Connect

Absolute Maximum Ratings*

Ambient Temperature
 Under Bias -10°C to +80°C
 Storage Temperature (plastic) -55°C to +125°C
 Voltage Relative to V_{SS} -1.0 V to +7.0 V
 Data Output Current 50 mA
 Power Dissipation 1.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

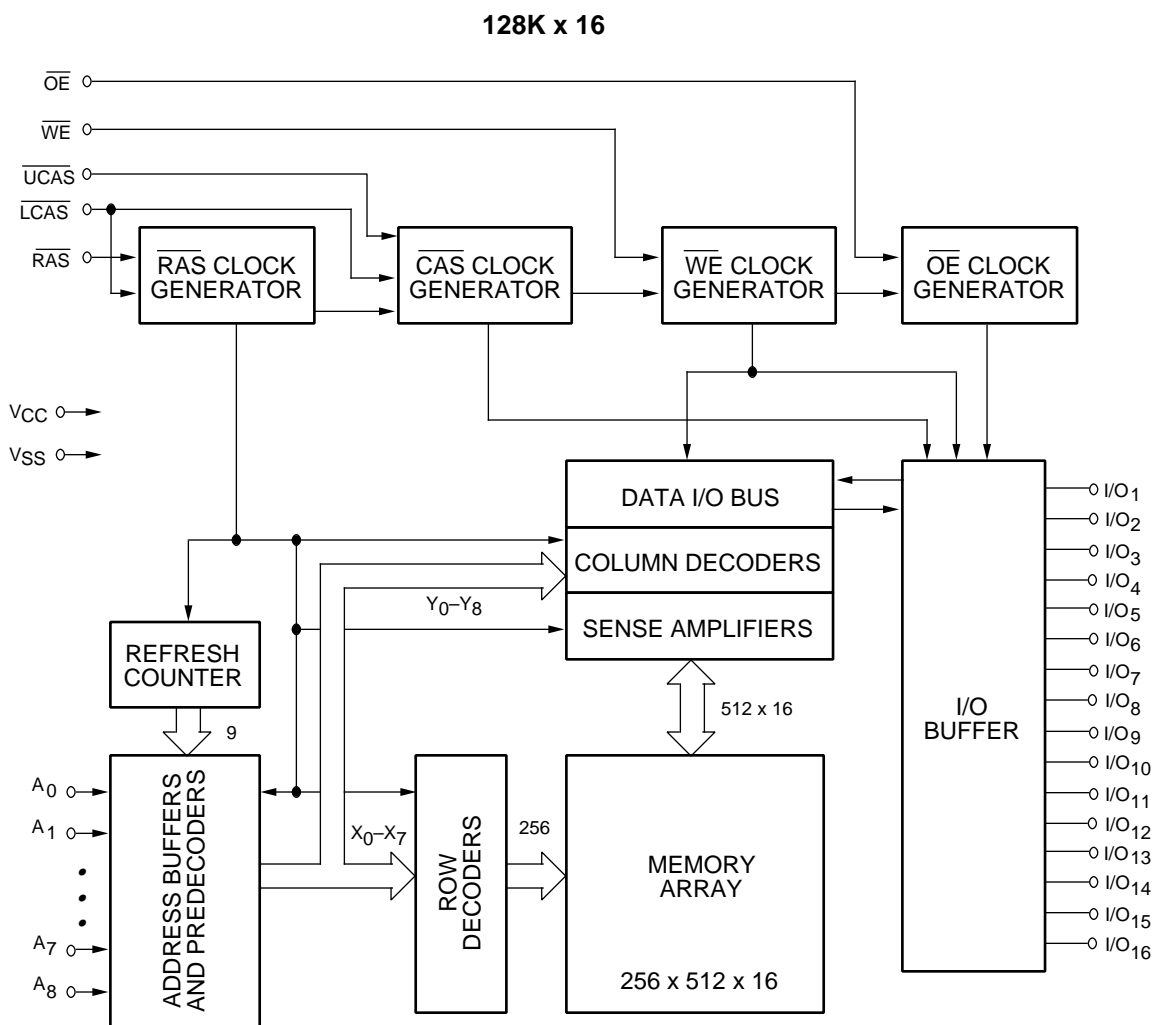
Capacitance*

T_A = 25°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C _{IN1}	Address Input	3	4	pF
C _{IN2}	RAS, UCAS, LCAS, WE, OE	4	5	pF
C _{OUT}	Data Input/Output	5	7	pF

*Note: Capacitance is sampled and not 100% tested

Block Diagram



16129H-04

DC and Operating Characteristics (1-2)

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, unless otherwise specified.

Symbol	Parameter	Access Time	V53C16129H			Unit	Test Conditions	Notes
			Min.	Typ.	Max.			
I_{LI}	Input Leakage Current (any input pin)		-10		10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$	
I_{LO}	Output Leakage Current (for High-Z State)		-10		10	μA	$V_{SS} \leq V_{OUT} \leq V_{CC}$ $\overline{\text{RAS}}, \overline{\text{CAS}}$ at V_{IH}	
I_{CC1}	V_{CC} Supply Current, Operating	40			180	mA	$t_{RC} = t_{RC}(\text{min.})$	1, 2
		45			170			
		50			160			
		60			150			
I_{CC2}	V_{CC} Supply Current, TTL Standby				2	mA	$\overline{\text{RAS}}, \overline{\text{CAS}}$ at V_{IH} , other inputs $\geq V_{SS}$	
I_{CC3}	V_{CC} Supply Current, RAS-Only Refresh	40			180	mA	$t_{RC} = t_{RC}(\text{min.})$	2
		45			170			
		50			160			
		60			150			
I_{CC4}	V_{CC} Supply Current, Fast Page Mode Operation	40			170	mA	Minimum Cycle	1, 2
		45			160			
		50			150			
		60			140			
I_{CC5}	V_{CC} Supply Current, Standby, Output Enabled				2	mA	$\overline{\text{RAS}} = V_{IH}$, $\overline{\text{CAS}} = V_{IL}$, other inputs $\geq V_{SS}$	1
I_{CC6}	V_{CC} Supply Current, CMOS Standby				1	mA	$\overline{\text{RAS}} \geq V_{CC} - 0.2\text{ V}$, $\overline{\text{CAS}} \geq V_{CC} - 0.2\text{ V}$, All other inputs $\geq V_{SS}$	
V_{CC}	Supply Voltage		4.5	5.0	5.5	V		
V_{IL}	Input Low Voltage		-1		0.8	V		3
V_{IH}	Input High Voltage		2.4		$V_{CC} + 1$	V		3
V_{OL}	Output Low Voltage				0.4	V	$I_{OL} = 4.2\text{ mA}$	
V_{OH}	Output High Voltage		2.4		2.4	V	$I_{OH} = -5\text{ mA}$	

AC Characteristics

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{V}$ unless otherwise noted
 AC Test conditions, input pulse levels 0 to 3V

#	Symbol	Parameter	40		45		50		60		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RAS}	\overline{RAS} Pulse Width	40	75K	45	75K	50	75K	60	75K	ns	
2	t_{RC}	Read or Write Cycle Time	75		80		90		110		ns	
3	t_{RP}	\overline{RAS} Precharge Time	25		25		30		40		ns	
4	t_{CSH}	\overline{CAS} Hold Time	40		45		50		60		ns	
5	t_{CAS}	\overline{CAS} Pulse Width	7		8		9		15		ns	
6	t_{RCD}	\overline{RAS} to \overline{CAS} Delay	17	28	18	32	19	36	20	45	ns	
7	t_{RCS}	Read Command Setup Time	0		0		0		0		ns	4
8	t_{ASR}	Row Address Setup Time	0		0		0		0		ns	
9	t_{RAH}	Row Address Hold Time	7		8		9		10		ns	
10	t_{ASC}	Column Address Setup Time	0		0		0		0		ns	
11	t_{CAH}	Column Address Hold Time	5		6		7		10		ns	
12	$t_{RSH (R)}$	\overline{RAS} Hold Time (Read Cycle)	10		10		10		15		ns	
13	t_{CRP}	\overline{CAS} to \overline{RAS} Precharge Time	5		5		5		5		ns	
14	t_{RCH}	Read Command Hold Time Referenced to \overline{CAS}	0		0		0		0		ns	5
15	t_{RRH}	Read Command Hold Time Referenced to \overline{RAS}	0		0		0		0		ns	5
16	t_{ROH}	\overline{RAS} Hold Time Referenced to \overline{OE}	8		9		10		10		ns	
17	t_{OAC}	Access Time from \overline{OE}		12		13		14		14	ns	12
18	t_{CAC}	Access Time from \overline{CAS}		12		13		14		14	ns	6,7,14
19	t_{RAC}	Access Time from \overline{RAS}		40		45		50		50	ns	6, 8, 9
20	t_{CAA}	Access Time from Column Address		20		22		24		24	ns	6,7,10
21	t_{LZ}	\overline{OE} or \overline{CAS} to Low-Z Output	0		0		0		0		ns	16
22	t_{HZ}	\overline{OE} or \overline{CAS} to High-Z Output	0	6	0	7	0	8	0	8	ns	16
23	t_{AR}	Column Address Hold Time from \overline{RAS}	30		35		40		50		ns	
24	t_{RAD}	\overline{RAS} to Column Address Delay Time	12	20	13	23	14	26	15	30	ns	11
25	$t_{RSH (W)}$	\overline{RAS} or \overline{CAS} Hold Time in Write Cycle	10		10		10		15		ns	
26	t_{CWL}	Write Command to \overline{CAS} Lead Time	12		13		14		15		ns	
27	t_{WCS}	Write Command Setup Time	0		0		0		0		ns	12, 13
28	t_{WCH}	Write Command Hold Time	5		6		7		10		ns	
29	t_{WP}	Write Pulse Width	5		6		7		10		ns	
30	t_{WCR}	Write Command Hold Time from \overline{RAS}	30		35		40		50		ns	
31	t_{RWL}	Write Command to \overline{RAS} Lead Time	12		13		14		15		ns	

AC Characteristics (Cont'd)

#	Symbol	Parameter	40		45		50		60		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
32	t _{DS}	Data in Setup Time	0		0		0		0		ns	14
33	t _{DH}	Data in Hold Time	5		6		7		10		ns	14
34	t _{WOH}	Write to \overline{OE} Hold Time	6		7		8		10		ns	14
35	t _{OED}	\overline{OE} to Data Delay Time	6		7		8		10		ns	14
36	t _{RWC}	Read-Modify-Write Cycle Time	110		115		130		170		ns	
37	t _{RRW}	Read-Modify-Write Cycle \overline{RAS} Pulse Width	75		80		87		105		ns	
38	t _{CWD}	\overline{CAS} to \overline{WE} Delay	30		32		34		40		ns	12
39	t _{RWD}	\overline{RAS} to \overline{WE} Delay in Read-Modify-Write Cycle	58		62		68		85		ns	12
40	t _{CRW}	\overline{CAS} Pulse Width (RMW)	48		50		52		65		ns	
41	t _{AWD}	Col. Address to \overline{WE} Delay	38		41		42		58		ns	12
42	t _{PC}	EDO Fast Page Mode Read or Write Cycle Time	15		17		19		27		ns	
43	t _{CP}	\overline{CAS} Precharge Time	5		6		7		10		ns	
44	t _{CAR}	Column Address to \overline{RAS} Setup Time	20		22		24		30		ns	
45	t _{CAP}	Access Time from Column Precharge		23		25		27		34	ns	7
46	t _{DHR}	Data in Hold Time Referenced to \overline{RAS}	30		35		40		50		ns	
47	t _{CSR}	\overline{CAS} Setup Time \overline{CAS} -before- \overline{RAS} Refresh	10		10		10		10		ns	
48	t _{RPC}	\overline{RAS} to \overline{CAS} Precharge Time	0		0		0		0		ns	
49	t _{CHR}	\overline{CAS} Hold Time \overline{CAS} -before- \overline{RAS} Refresh	8		10		12		15		ns	
50	t _{PCM}	EDO Page Mode Read-Modify-Write Cycle Time	60		65		70		85		ns	
51	t _{COH}	Output Hold After \overline{CAS} Low	5		5		5		5		ns	
52	t _{OES}	\overline{OE} Low to \overline{CAS} HIGH Setup Time	5		5		5		5		ns	
53	t _{OEH}	\overline{OE} Hold Time from \overline{WE} during Read-Modify-Write Cycle	10		10		10		10		ns	
54	t _{OEP}	\overline{OE} High Pulse Width	10		10		10		10		ns	
55	t _T	Transition Time (Rise and Fall)	1.5	50	1.5	50	1.5	50	1.5	50	ns	15
56	t _{REF}	Refresh Interval (512 Cycles)		8		8		8		8	ms	17

Notes:

1. I_{CC} is dependent on output loading when the device output is selected. Specified I_{CC} (max.) is measured with the output open.
2. I_{CC} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in EDO Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to -1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) $\geq V_{SS}$ and V_{IH} (max.) $\leq V_{DD}$.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC} .
5. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle to occur.
6. Measured with a load equivalent to one TTL inputs and 100 pF.
7. Access time is determined by the longest of t_{CAA} , t_{CAC} and t_{CAP} .
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC} .
12. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of \overline{CAS} or \overline{WE} .
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume $t_T = 3$ ns.
16. Assumes a three-state test load (5 pF and a 380 Ohm Thevenin equivalent).
17. An initial 200 μ s pause and 8 \overline{RAS} -containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

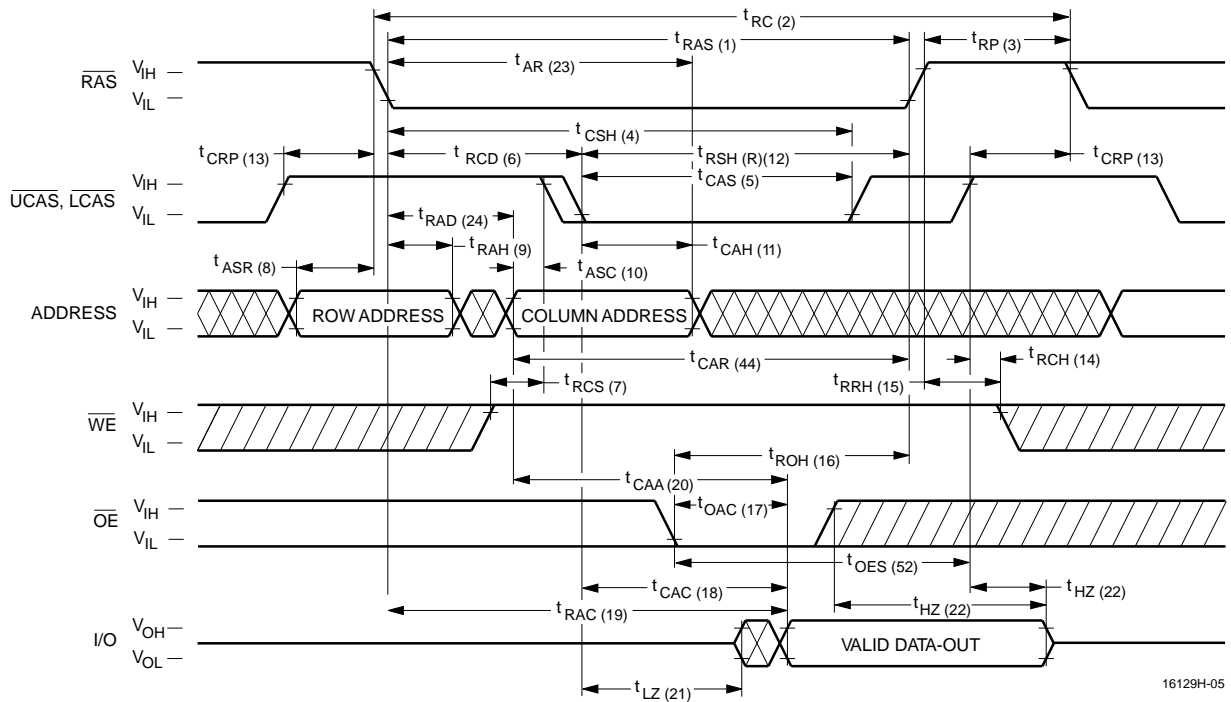
Truth Table

Function	RAS	LCAS	UCAS	WE	OE	ADDRESS	I/O	Notes
Standby	H	H	H	X	X	X	High-Z	
Read: Word	L	L	L	H	L	ROW/COL	Data Out	
Read: Lower Byte	L	L	H	H	L	ROW/COL	Lower Byte, Data-Out Upper Byte, High-Z	
Read: Upper Byte	L	H	L	H	L	ROW/COL	Lower Byte, High-Z Upper Byte, Data-Out	
Write: Word (Early-Write)	L	L	L	L	X	ROW/COL	Data-In	
Write: Lower Byte (Early)	L	L	H	L	X	ROW/COL	Lower Byte, Data-In Upper Byte, High-Z	
Read: Upper Byte (Early)	L	H	L	L	X	ROW/COL	Lower Byte, High-Z Upper Byte, Data-In	
Read-Write	L	L	L	H→L	L→H	ROW/COL	Data-Out, Data-In	1, 2
Page-Mode Read	L	H→L	H→L	H	L	COL	Data-Out	2
Page-Mode Write	L	H→L	H→L	L	X	COL	Data-In	2
Page-Mode Read-Write	L	H→L	H→L	H→L	L→H	COL	Data-Out, Data-In	1, 2
Hidden Refresh Read	L→H→L	L	L	H	L	ROW/COL	Data-Out	2
RAS-Only Refresh	L	H	H	X	X	ROW	High-Z	
CBR Refresh	H→L	L	L	X	X	X	High-Z	3

Notes:

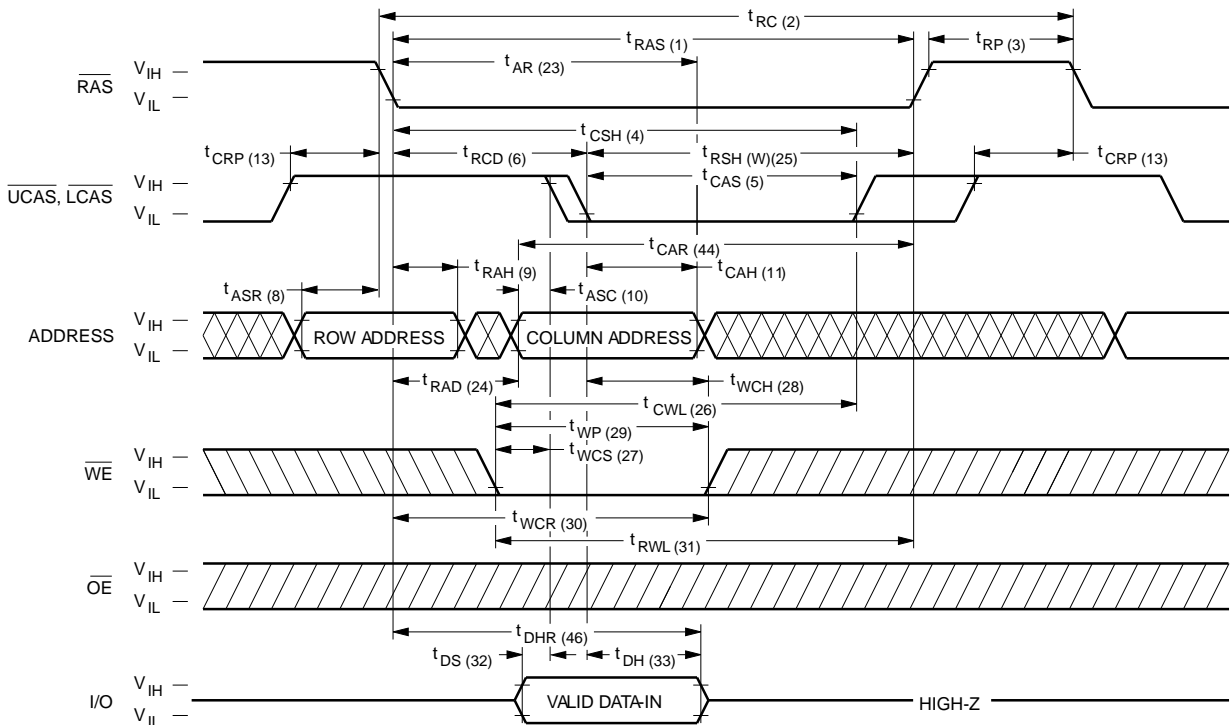
1. Byte Write cycles \overline{LCAS} or \overline{UCAS} active.
2. Byte Read cycles \overline{LCAS} or \overline{UCAS} active.
3. Only one of the two \overline{CAS} must be active (\overline{LCAS} or \overline{UCAS}).

Waveforms of Read Cycle



16129H-05

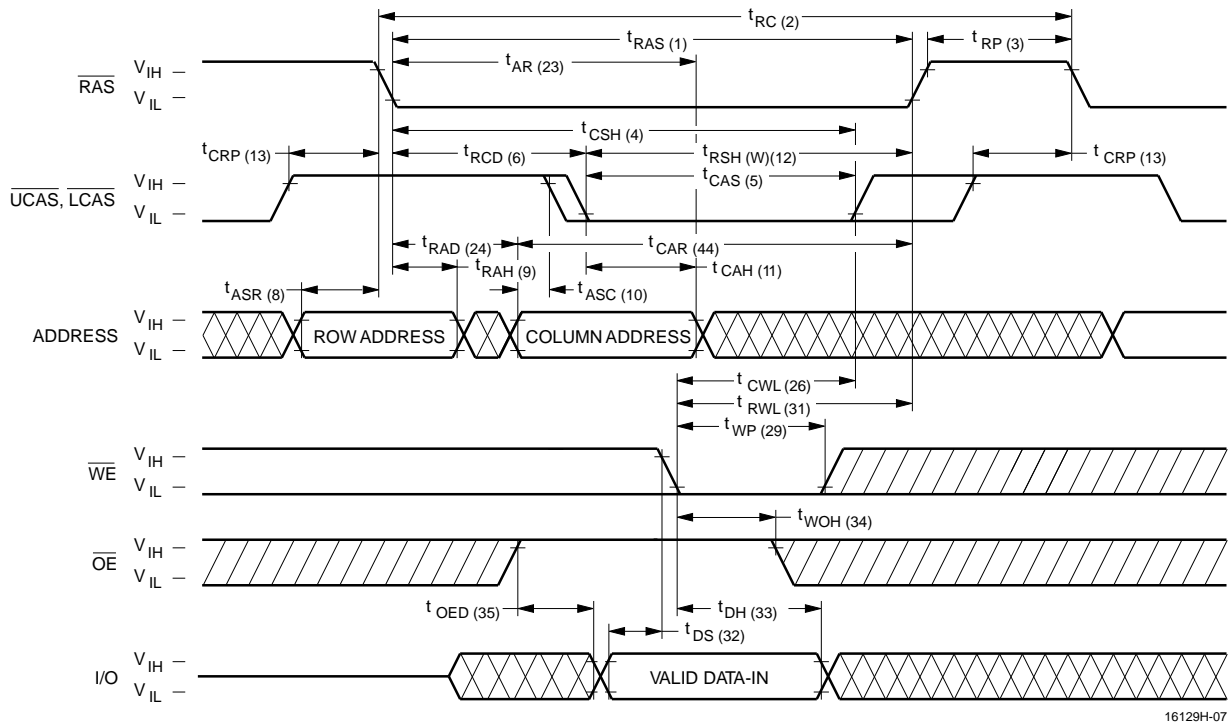
Waveforms of Early Write Cycle



16129H-06

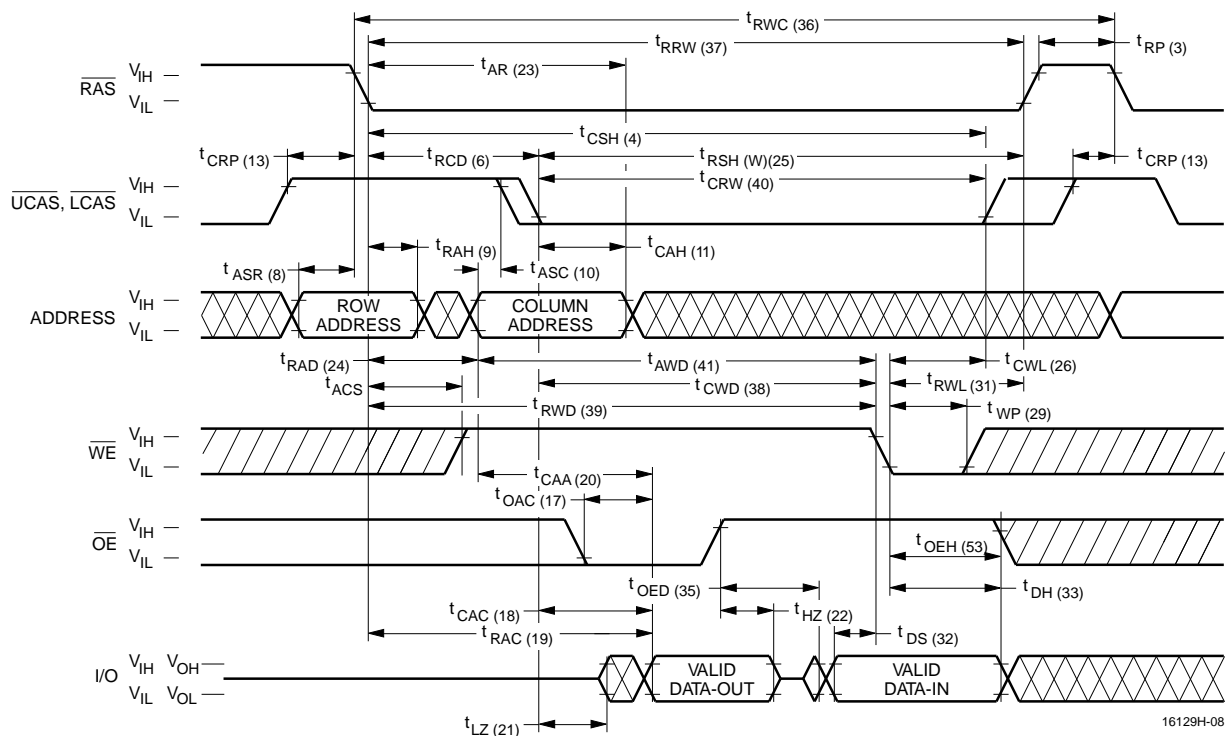
Don't Care Undefined

Waveforms of OE-Controlled Write Cycle

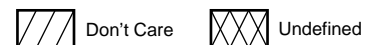


16129H-07

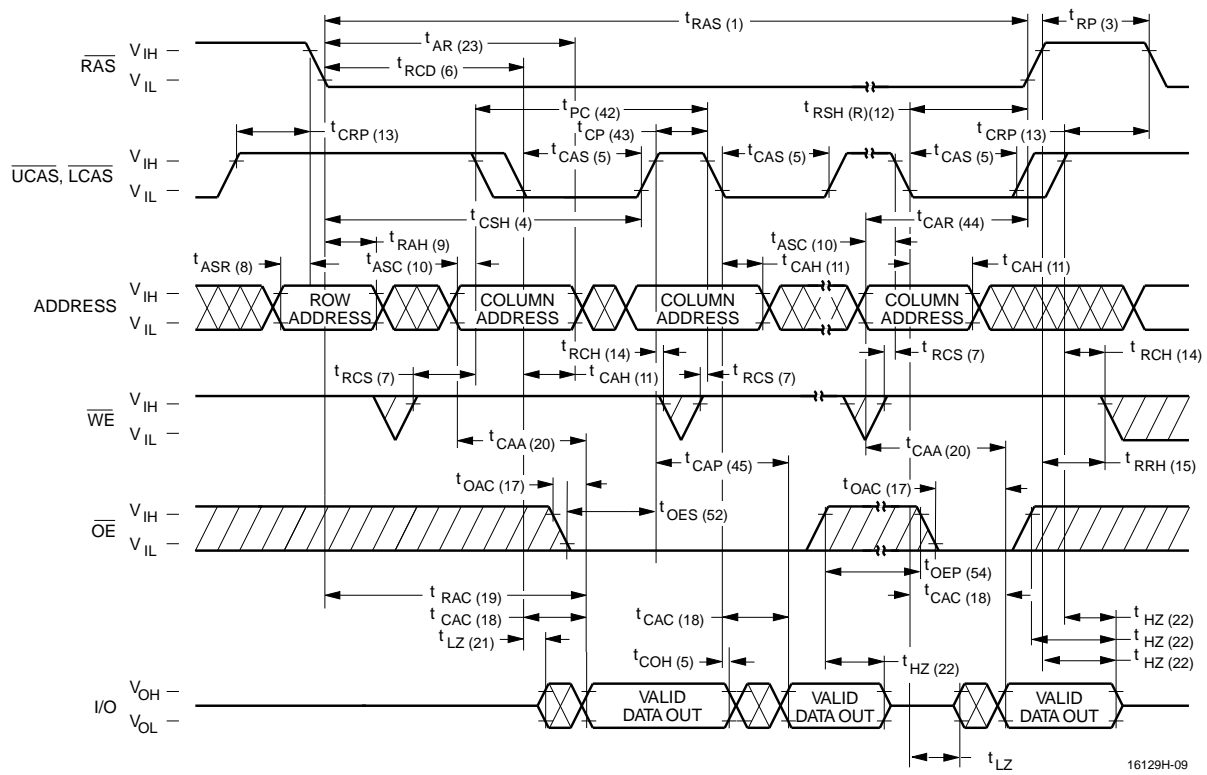
Waveforms of Read-Modify-Write Cycle



16129H-08

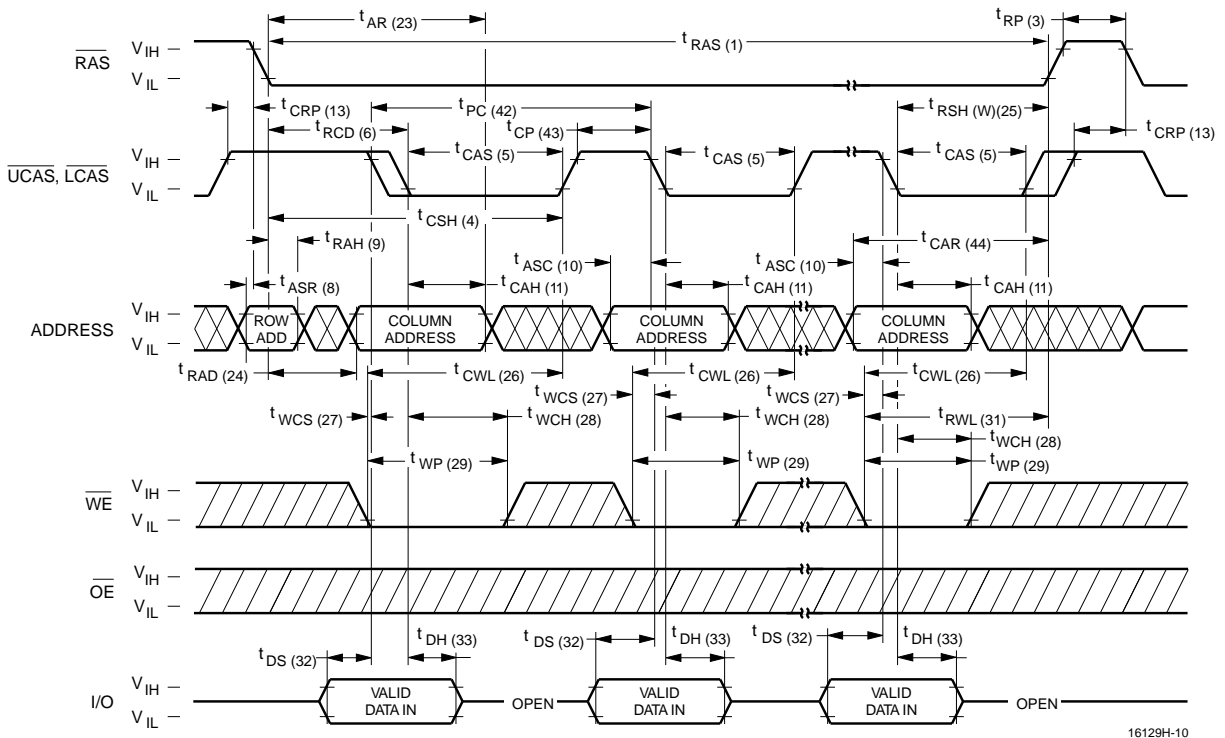


Waveforms of EDO Page Mode Read Cycle



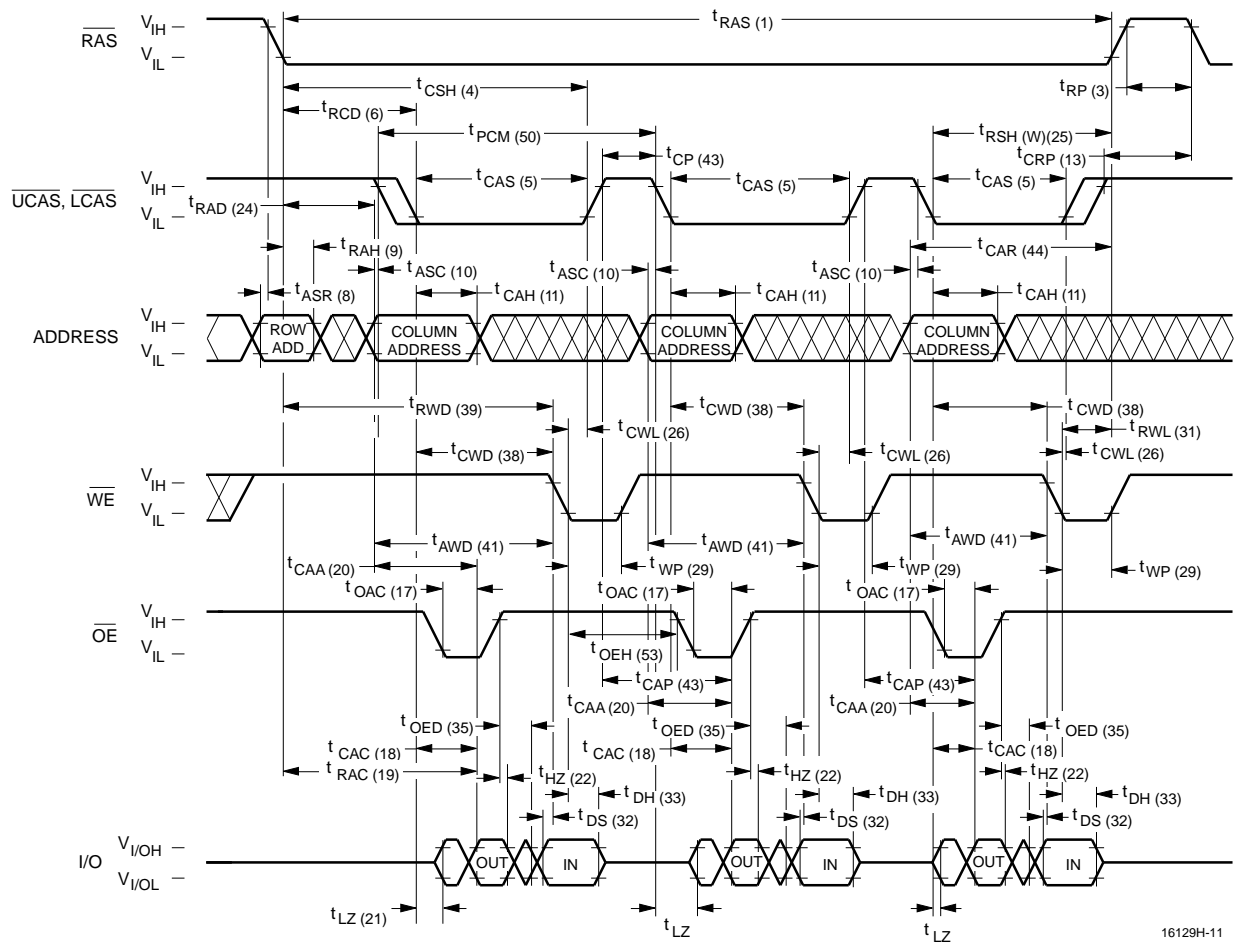
16129H-09

Waveforms of EDO Page Mode Write Cycle



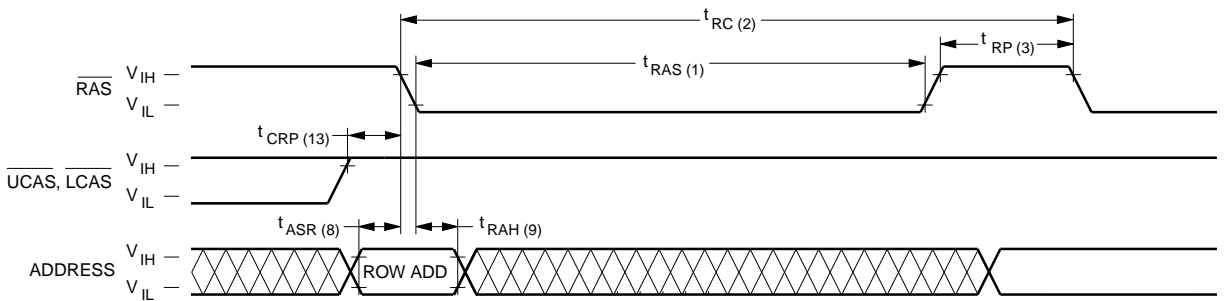
16129H-10

Waveforms of EDO Page Mode Read-Write Cycle



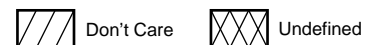
16129H-11

Waveforms of RAS-Only Refresh Cycle

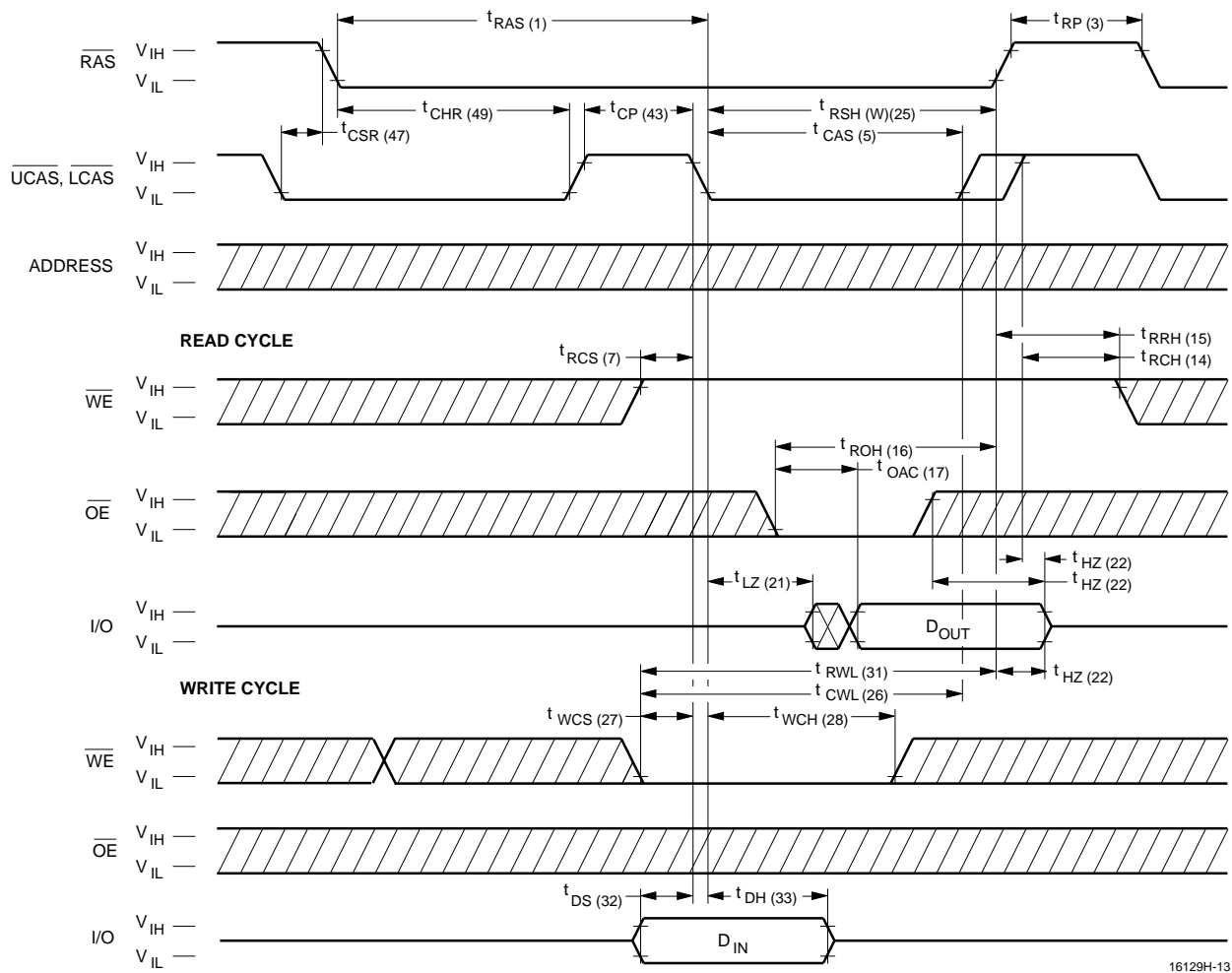


NOTE: \overline{WE} , \overline{OE} = Don't care

16129H-12

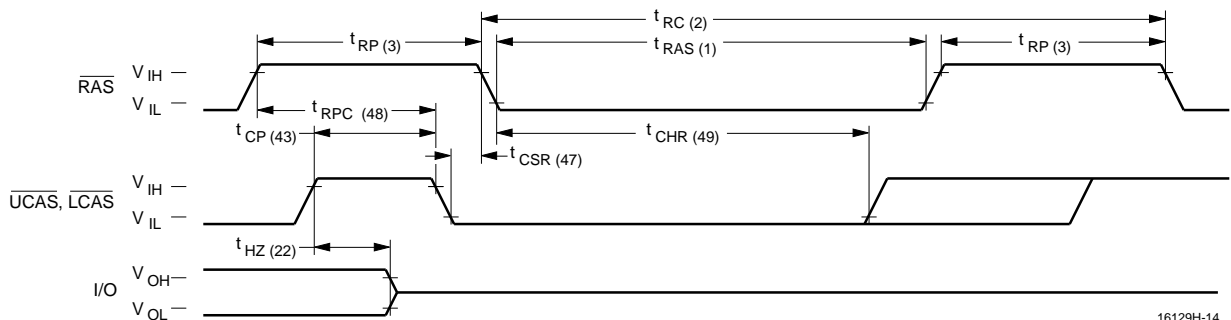


Waveforms of $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Counter Test Cycle



16129H-13

Waveforms of $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle

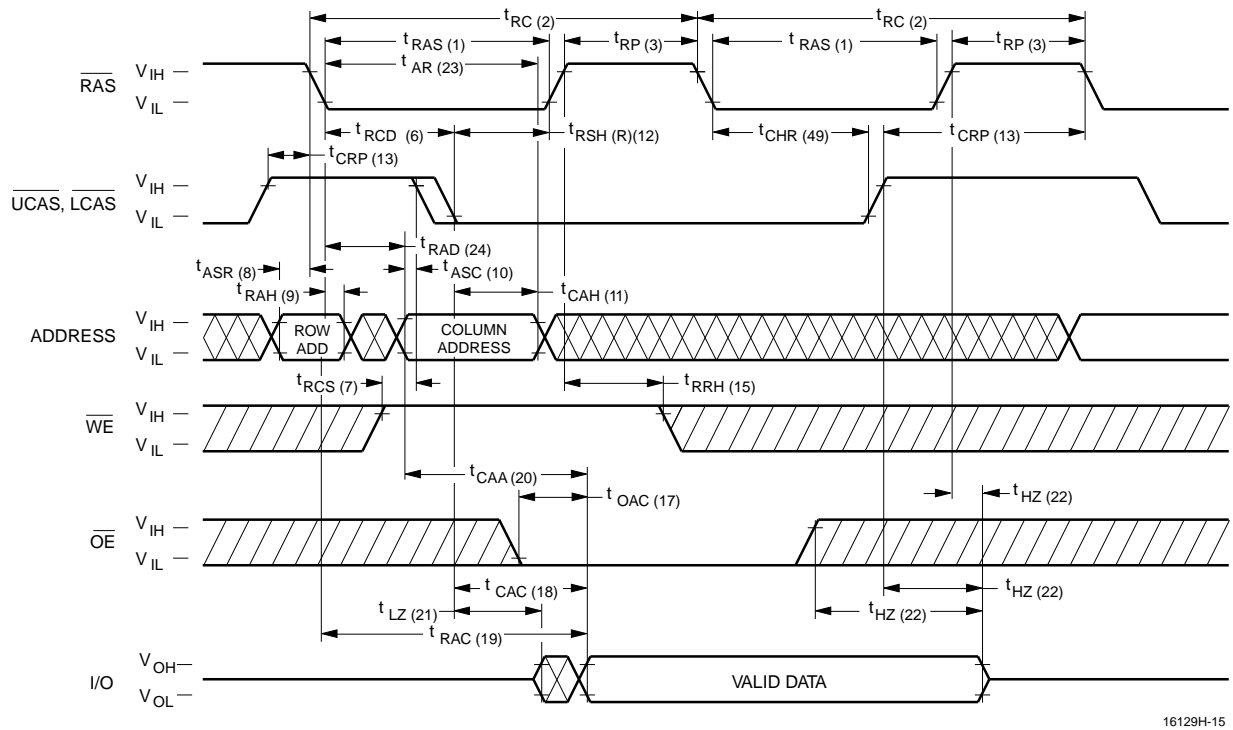


16129H-14

NOTE: $\overline{\text{WE}}$, $\overline{\text{OE}}$, A_0 - A_8 = Don't care

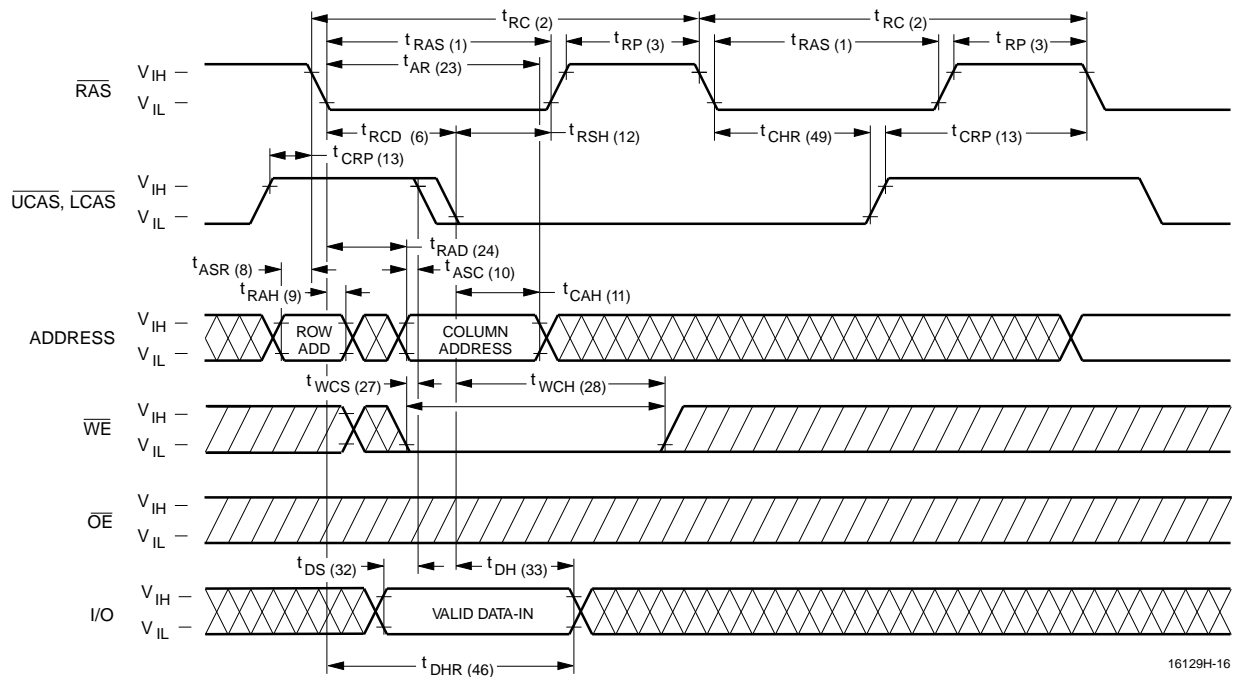
Don't Care Undefined

Waveforms of Hidden Refresh Cycle (Read)



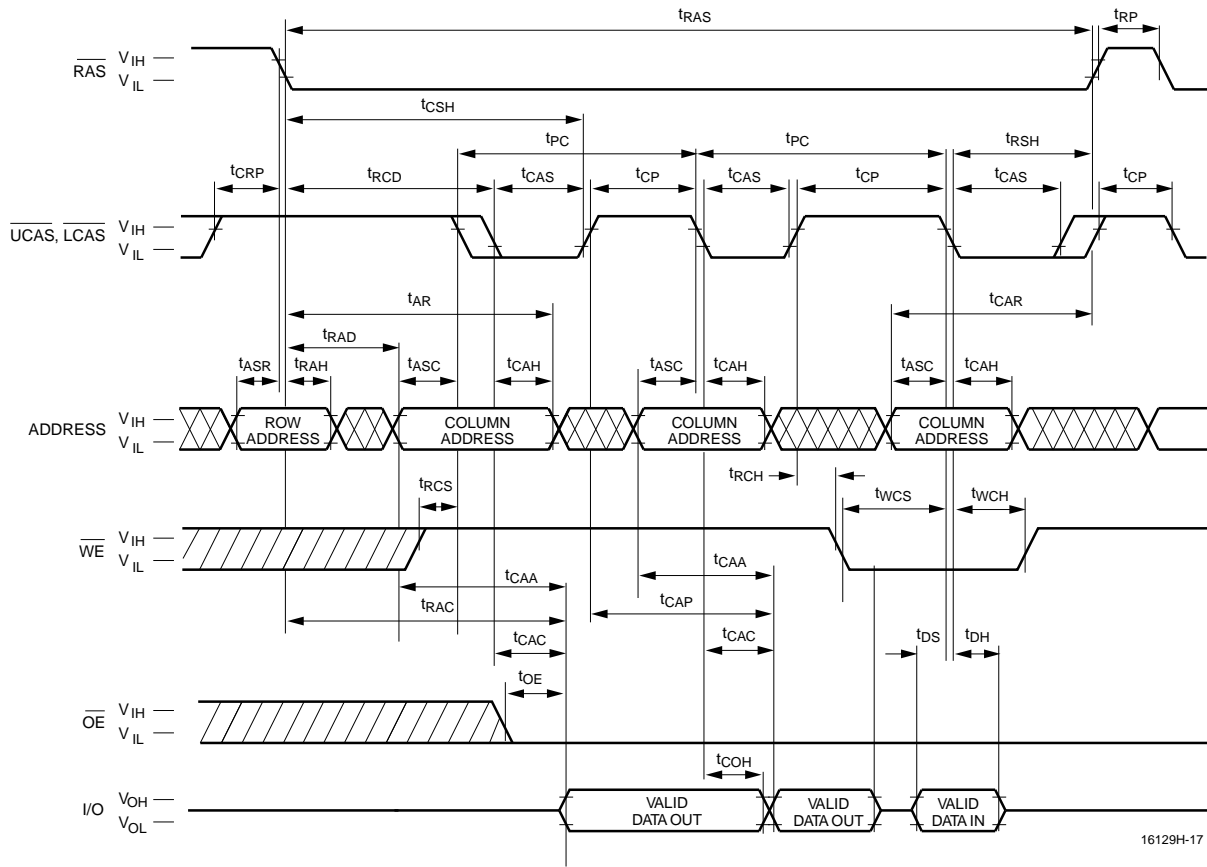
16129H-15

Waveforms of Hidden Refresh Cycle (Write)



16129H-16

Waveforms of EDO Page Mode Read-Early-Write Cycle (Pseudo Read-Modify-Write)



16129H-17

Functional Description

The V53C16129H is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C16129H reads and writes data by multiplexing an 17-bit address into a 8-bit row and an 9-bit column address. The row address is latched by the Row Address Strobe (\overline{RAS}). The column address “flows through” an internal address buffer and is latched by the Column Address Strobe (\overline{CAS}). Because access time is primarily dependent on a valid column address rather than the precise time that the \overline{CAS} edge occurs, the delay time from \overline{RAS} to \overline{CAS} has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing \overline{RAS} low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable (\overline{WE}) signal High during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum specified by t_{AR} . Data Out becomes valid only when t_{OAC} , t_{RAC} , t_{CAA} and t_{CAC} are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by t_{CAA} when t_{RAC} , t_{CAC} and t_{OAC} are all satisfied.

Write Cycle

A Write Cycle is performed by taking \overline{WE} and \overline{CAS} low during a \overline{RAS} operation. The column address is latched by \overline{CAS} . The Write Cycle can be \overline{WE} controlled or \overline{CAS} controlled depending on whether \overline{WE} or \overline{CAS} falls later. Consequently, the input data must be valid at or before the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. In the \overline{CAS} -controlled Write Cycle, when the leading edge of \overline{WE} occurs prior to the \overline{CAS} low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function. Ending the Write with \overline{RAS} or \overline{CAS} will maintain the output in the High-Z state.

In the \overline{WE} controlled Write Cycle, \overline{OE} must be in the high state and t_{OED} must be satisfied.

Refresh Cycle

To retain data, 512 Refresh Cycles are required in each 8 ms period. There are two ways to refresh the memory:

1. By clocking each of the 512 row addresses (A_0 through A_8) with \overline{RAS} at least once every 8 ms. Any Read, Write, Read-Modify-Write or \overline{RAS} -only cycle refreshes the addressed row.
2. Using a \overline{CAS} -before- \overline{RAS} Refresh Cycle. If \overline{CAS} makes a transition from low to high to low after the previous cycle and before \overline{RAS} falls, \overline{CAS} -before- \overline{RAS} refresh is activated. The V53C16129H uses the output of an internal 9-bit counter as the source of row addresses and ignore external address inputs.

\overline{CAS} -before- \overline{RAS} is a “refresh-only” mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle. A \overline{CAS} -before- \overline{RAS} counter test mode is provided to ensure reliable operation of the internal refresh counter.

Extended Data Output Page Mode

EDO Page operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining \overline{RAS} low while performing successive \overline{CAS} cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while \overline{CAS} is high. Thus, access begins from the occurrence of a valid column address rather than from the falling edge of \overline{CAS} , eliminating t_{ASC} and t_T from the critical timing path. \overline{CAS} latches the address into the column address buffer. During EDO operation, Read, Write, Read-Modify-Write or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Hyper Page Mode, access is t_{CAA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of \overline{CAS} , the access time is referenced to the \overline{CAS} rising edge and is specified by t_{CAP} . If the column address is valid after the rising \overline{CAS} edge, access is timed from the occurrence of a valid address and is specified by t_{CAA} . In both cases, the falling edge of \overline{CAS} latches the address and enables the output.

EDO provides a sustained data rate of 83 MHz for applications that require high data rates such as bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{512}{t_{RC} + 511 \times t_{PC}}$$

Data Output Operation

The V53C16129H Input/Output is controlled by OE, CAS, WE and RAS. A RAS low transition enables the transfer of data to and from the selected row address in the Memory Array. A RAS high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a RAS low transition, a CAS low transition or CAS low level enables the internal I/O path. A CAS high transition or a CAS high level disables the I/O path and the output driver if it is enabled. A CAS low transition while RAS is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding OE high. The OE signal has no effect on any data stored in the output latches. A WE low level can also disable the output drivers when CAS is low. During a Write cycle, if WE goes low at a time in relationship to CAS that would normally cause the outputs to be active, it is necessary to use OE to disable the output drivers prior to the WE low transition to allow Data In Setup Time (t_{DS}) to be satisfied.

Power-On

After application of the V_{CC} supply, an initial pause of 200 μs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a RAS clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

During Power-On, the V_{CC} current requirement of the V53C16129H is dependent on the input levels of RAS and CAS. If RAS is low during Power-On, the device will go into an active cycle and I_{CC} will exhibit current transients. It is recommended that RAS and CAS track with V_{CC} or be held at a valid V_{IH} during Power-On to avoid current surges.

Table 1. V53C16129H Data Output Operation for Various Cycle Types

Cycle Type	I/O State
Read Cycles	Data from Addressed Memory Cell
CAS-Controlled Write Cycle (Early Write)	High-Z
WE-Controlled Write Cycle (Late Write)	OE Controlled. High OE = High-Z I/Os
Read-Modify-Write Cycles	Data from Addressed Memory Cell
EDO Page Mode Read	Data from Addressed Memory Cell
EDO Page Mode Write Cycle (Early Write)	High-Z
EDO Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
RAS-only Refresh	High-Z
CAS-before-RAS Refresh Cycle	Data remains as in previous cycle
CAS-only Cycles	High-Z

U.S.A.

3910 NORTH FIRST STREET
SAN JOSE, CA 95134
PHONE: 408-433-6000
FAX: 408-433-0185

TAIWAN

7F, NO. 102
MIN-CHUAN E. ROAD, SEC. 3
TAIPEI
PHONE: 011-886-2-545-1213
FAX: 011-886-2-545-1209

JAPAN

RM.302 ANNEX-G
HIGASHI-NAKANO
NAKANO-KU, TOKYO 164
PHONE: 011-81-03-3365-2851
FAX: 011-81-03-3365-2836

HONG KONG

19 DAI FU STREET
TAIPO INDUSTRIAL ESTATE
TAIPO, NT, HONG KONG
PHONE: 011-852-665-4883
FAX: 011-852-664-7535

1 CREATION ROAD I
SCIENCE BASED IND. PARK
HSIN CHU, TAIWAN, R.O.C.
PHONE: 011-886-35-783344
FAX: 011-886-35-792838

NORTHWESTERN

3910 NORTH FIRST STREET
SAN JOSE, CA 95134
PHONE: 408-433-6000
FAX: 408-433-0185

SOUTHWESTERN

SUITE 200
5150 E. PACIFIC COAST HWY.
LONG BEACH, CA 90804
PHONE: 310-498-3314
FAX: 310-597-2174

CENTRAL & SOUTHEASTERN

604 FIELDWOOD CIRCLE
RICHARDSON, TX 75081
PHONE: 972-690-1402
FAX: 972-690-0341

NORTHEASTERN

SUITE 436
20 TRAFALGAR SQUARE
NASHUA, NH 03063
PHONE: 603-889-4393
FAX: 603-889-9347

The information in this document is subject to change without notice.

MOSEL VITELIC makes no commitment to update or keep current the information contained in this document. No part of this document may be copied or reproduced in any form or by any means without the prior written consent of MOSEL-VITELIC.

MOSEL VITELIC subjects its products to normal quality control sampling techniques which are intended to provide an assurance of high quality products suitable for usual commercial applications. MOSEL VITELIC does not do testing appropriate to provide 100% product quality assurance and does not assume any liability for consequential or incidental arising from any use of its products. If such products are to be used in applications in which personal injury might occur from failure, purchaser must do its own quality assurance testing appropriate to such applications.