M6MFB/T16S2TP

PRELIMINARY

Notice : This is not a final specification.
Some parametric limits are subject to change.

16777216-BIT (2M x 8-BIT / 1M x 16-BIT) CMOS 3.3V-ONLY FLASH MEMORY &
2097152-BIT (256k x 8-BIT) CMOS STATIC RAM
MCP (Multi Chip Package)

DESCRIPTION

The MITSUBISHI M6MFB/T16S2TP is a Multi Chip Package (MCP) that contents 16-Mbit Flash memory and 2M-bit Static RAM in a 82-pin TSOP(TYPE-II).

16M-bit Flash memory is a 2097152 bytes/1048572 words, 3.3V-only, and high performance non-volatile memory fabricated by CMOS technology for the peripheral circuit and DINOR(DIvided bit-line NOR) architecture for the memory cell.
2M-bit SRAM is a 262144 bytes unsynchronous SRAM fabricated by silicon-gate CMOS technology.

M6MFB/T16S2TP is suitable for the application of the mobile-communication-system to reduce both the mount space and weight .

FEATURES

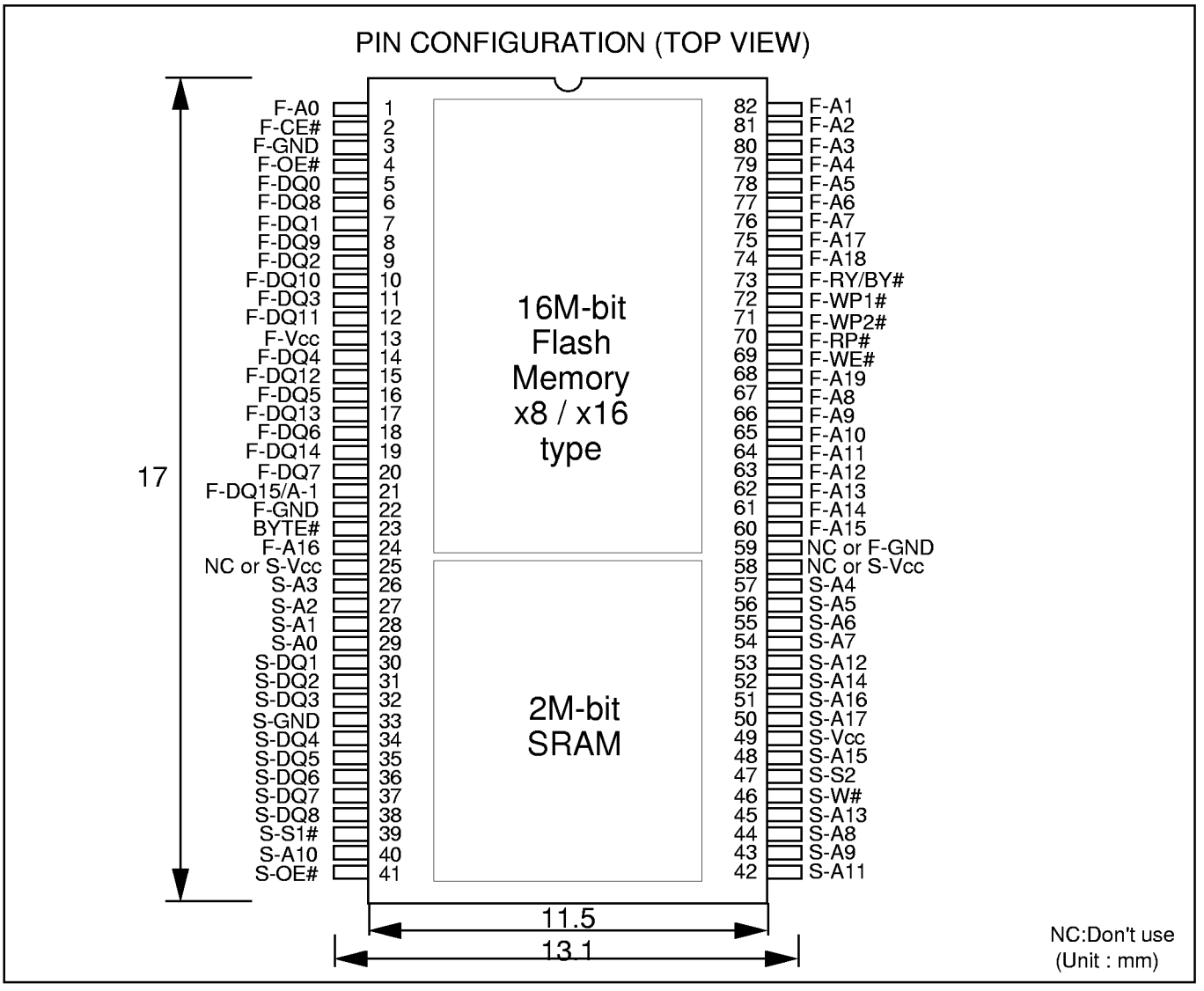
- Flash memory, SRAM Access time ----- 110ns (Max.)
- Supply voltage ---------- Vcc=2.7 ~ 3.6V
- Ambient temperature ---------- Ta=-20 ~ 85°C

- Flash Memory / SRAM : Operates individually
- Package : 82-pin TSOP (Type-II) , 0.4mm lead pitch

APPLICATION

Mobile communication products

PIN CONFIGURATION (TOP VIEW)



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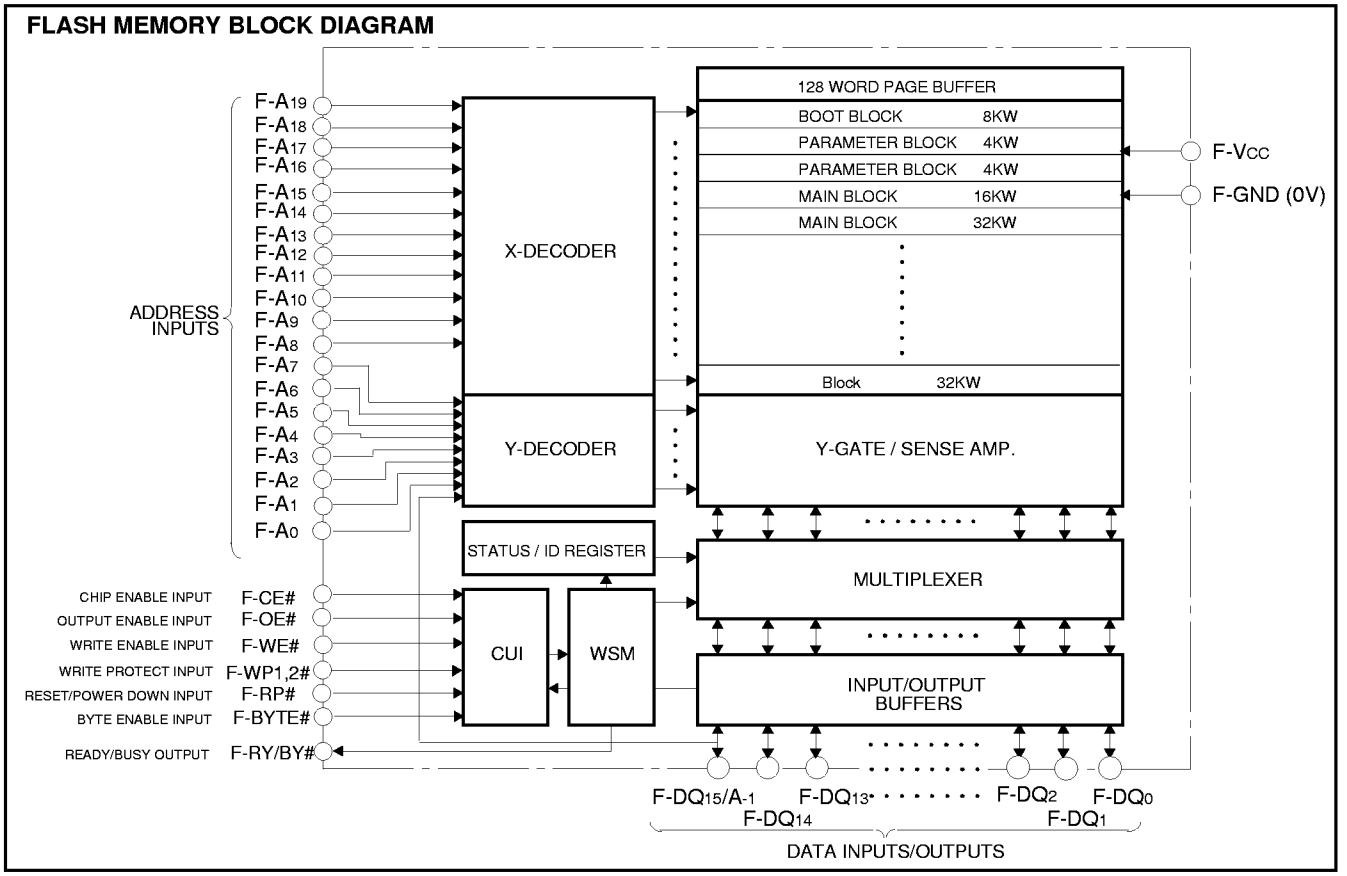
M6MFB/T16S2TP

16777216-BIT (2M x 8-BIT/1M x 16-BIT) CMOS 3.3V-ONLY FLASH MEMORY

FLASH MEMORY BLOCK DIAGRAM



FUNCTION

The flash memory of M6MFT/B16S2TP includes on-chip program/erase control circuitry. The Write State Machine (WSM) controls block erase and page program operations. Operational modes are selected by the commands written to the Command User Interface (CUI). The Status Register indicates the status of the WSM and when the WSM successfully completes the desired program or block erase operation.

A Deep Powerdown mode is enabled when the F-RP# pin is at GND, minimizing power consumption.

Read

The flash memory of M6MFT/B16S2TP has three read modes, which accesses to the memory array, the Device Identifier and the Status Register. The appropriate read command are required to be written to the CUI. Upon initial device powerup or after exit from deep powerdown, the flash memory automatically resets to read array mode. In the read array mode, low level input to F-CE# and F-OE#, high level input to F-WE# and F-RP#, and address signals to the address inputs ($F\text{-}A_{0\text{-}19}$) output the data of the addressed location to the data input/output($F\text{-}DQ_{0\text{-}15}$).

Write

Writes to the CUI enables reading of memory array data, device identifiers and reading and clearing of the Status Register. They also enable block erase and program. The CUI is written by bringing F-WE# to low level, while F-CE# is at low level and F-OE# is at high level. Address and data are latched on the earlier rising edge of F-WE# and F-CE#. Standard micro-processor write timings are used.

Output Disable

When F-OE# is at V_{IH}, output from the devices is disabled. Data input/output are in a high-impedance(High-Z) state.

Standby

When F-CE# is at V_{IH}, the device is in the standby mode and its power consumption is reduced. Data input/output are in a high-impedance(High-Z) state. If the memory is deselected during block erase or program, the internal control circuits remain active and the device consume normal active power until the operation completes.

Automatic Power Saving

When addresses remain stable for about 300ns(T.B.D), the device enters the automatic power saving mode. While in power saving mode, output data is latched and always availavle to the system.

Deep Power-Down

When F-RP# is at V_{IL}, the device is in the deep powerdown mode and its power consumption is substantially low. During read modes, the memory is deselected and the data input/output are in a high-impedance(High-Z) state. After return from powerdown, the CUI is reset to Read Array , and the Status Register is cleared to value 80H.

During block erase or program modes, F-RP# low will abort either operation. Memory array data of the block being altered become invalid.

SOFTWARE COMMAND DEFINITIONS

The device operations are selected by writing specific software command into the Command User Interface.

Read Array Command (FFH)

The device is in Read Array mode on initial device powerup and after exit from deep powerdown, or by writing FFH to the Command User Interface. The device remains in Read Array mode until the other commands are written.

Read Device Identifier Command (90H)

The Device Identifier is read after writing the Read Device Identifier command of 90H to the Command User Interface. Following the command write, the manufacturer code and the device code can be read from address 000000H and 000001H, respectively. Additionally, The Device Identifier is read by rising F-A9 to high voltage for PROM programmers.

Read Status Register Command (70H)

The Status Register is read after writing the Read Status Register command of 70H to the Command User Interface.
The contents of Status Register are latched on the later falling edge of F-OE# or F-CE#. So F-CE# or F-OE# must be toggled every status read.

Clear Status Register Command (50H)

The Erase Status and Program Status bits are set to "1"s by the Write State Machine and can only be reset by the Clear Status Register command of 50H. These bits indicates various failure conditions.

Block Erase / Confirm Command (20H/D0H)

Automated block erase is initiated by writing the Block Erase command of 20H followed by the Confirm command of D0H. An address within the block to be erased is required. The WSM executes iterative erase pulse application and erase verify operation.

Page Program Commands(41H)

Page Program allows fast programming of 128words of data in word-wide mode. Writing of 41H initiates the page program operation. From 2nd cycle to 129th cycle write data must be serially inputted. Address A6-0 have to be incremented from 00H to 7FH. After completion of data loading, the WSM controls the program pulse application and verify operation.

Basically re-program must not be done on a page which has already programmed.

Suspend/Resume Command (B0H/D0H)

Writing the Suspend command of B0H during block erase operation interrupts the block erase operation and allows read out from another block of memory. Writing the Suspend command of B0H during program operation interrupts the program operation and allows read out from another block of memory. The device continues to output Status Register data when read, after the Suspend command is written to it. Polling the WSM Status and Suspend Status bits will determine when the erase operation or program operation has been suspended. At this point, writing of the Read Array command to the CUI enables reading data from blocks other than that which is suspended. When the Resume command of D0H is written to the CUI, the WSM will continue with the erase or program processes.

DATA PROTECTION

The flash memory of M6MFB/T16S2TP provides hardware-locking of boot block, when F-WP1# is fixed to GND, boot block and all main blocks, when F-WP2# is fixed to GND, all blocks, when F-WP1# and F-WP2# are fixed to GND, and selectable block locking of parameter/main blocks by the lock-bit state.
Hardware-locking is pevented from any modifications

Power Supply Voltage

When the power supply voltage (Vcc) is less than 2.2V, the device is set to the Read-only mode.
A delay time of 2 us is required before any device operation is initiated. The delay time is measured from the time Vcc reaches Vccmin.
During power up, F-RP#=GND is recommended. Falling in Busy status is not recommended for possibility of damaging the device.

PRELIMINARY

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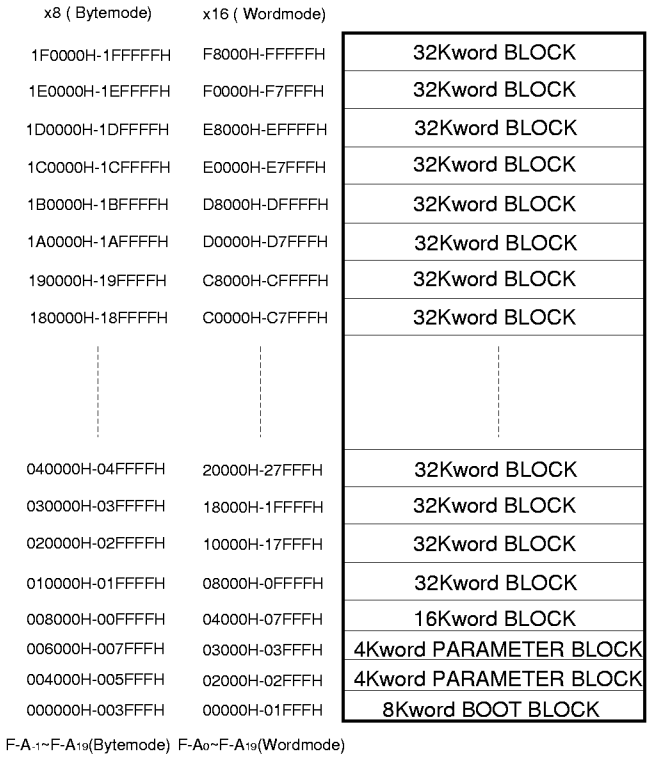
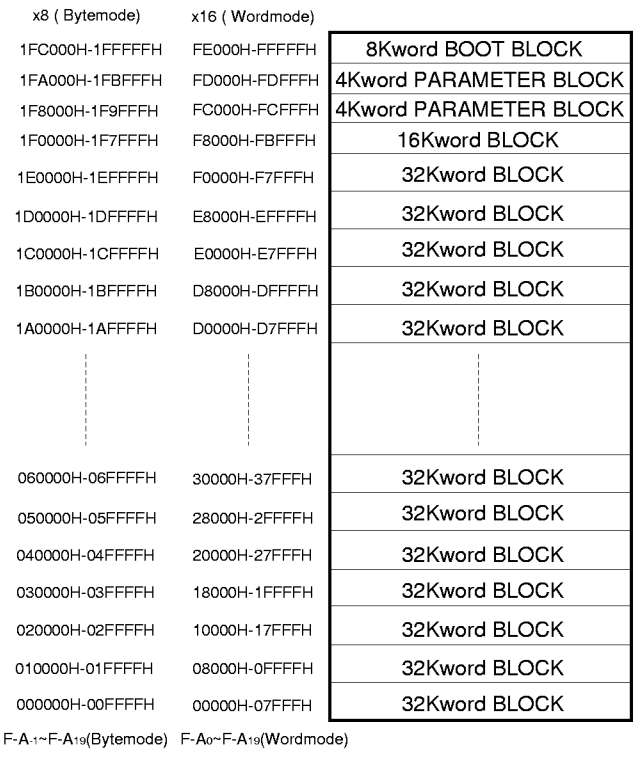


M6MFB16S2TP Flash Memory Map



M6MFT16S2TP Flash Memory Map

BUS OPERATIONS

Bus Operations for Word-Wide Mode (F-BYTE#=V_{IH})

Mode \ Pins		F-CE#	F-OE#	F-WE#	F-RP#	F-DQ0-15	F-RY/BY#
Read	Array	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Data out	V_{OH} (Hi-Z)
	Status Register	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Status Register Data	X [1]
	Lock Bit Status	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Lock Bit Data (DQ6)	X
	Identifier Code	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Identifier Code	V_{OH} (Hi-Z)
Output disable		V_{IL}	V_{IH}	V_{IH}	V_{IH}	Hi-Z	X
Stand by		V_{IH}	X [2]	X	V_{IH}	Hi-Z	X
Write	Program	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Command/Data in	X
	Erase	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Command	X
	Others	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Command	X
Deep Power Down		X	X	X	V_{IL}	Hi-Z	V_{OH} (Hi-Z)

Bus Operations for Byte-Wide Mode (F-BYTE#=V_{IL})

Mode \ Pins		F-CE#	F-OE#	F-WE#	F-RP#	F-DQ0-7	F-RY/BY#
Read	Array	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Data out	V_{OH} (Hi-Z)
	Status Register	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Status Register Data	X [1]
	Lock Bit Status	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Lock Bit Data (DQ6)	X
	Identifier Code	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Identifier Code	V_{OH} (Hi-Z)
Output disable		V_{IL}	V_{IH}	V_{IH}	V_{IH}	Hi-Z	X
Stand by		V_{IH}	X [2]	X	V_{IH}	Hi-Z	X
Write	Program	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Command/Data in	X
	Erase	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Command	X
	Others	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Command	X
Deep Power Down		X	X	X	V_{IL}	Hi-Z	V_{OH} (Hi-Z)

1) X at F-RY/BY# is V_{OL} or V_{OH}(Hi-Z).
*The F-RY/BY# is an open drain output pin and indicates status of the internal WSM. When low,it indicates that the WSM is Busy performing an operation.
A pull-up resistor of 10K-100K Ohms is required to allow the F-RY/BY# signal to transition high indicating a Ready WSM condition.
2) X can be V_{IH} or V_{IL} for control pins.

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SOFTWARE COMMAND DEFINITION
Command List

Command	1st bus cycle			2nd bus cycle			3rd bus cycle		
	Mode	Address	Data (F-DQ7-0)	Mode	Address	Data (F-DQ7-0)	Mode	Address	Data (F-DQ7-0)
Read Array	Write	X	FFH						
Device Identifier	Write	X	90H	Read	IA 2)	ID 2)			
Read Status Register	Write	X	70H	Read	X	SRD 3)			
Clear Status Register	Write	X	50H						
Page Program 4)	Write	X	41H	Write	WA0 4)	WD0 4)	Write	WA1	WD1
Block Erase / Confirm	Write	X	20H	Write	BA 5)	D0H			
Suspend	Write	X	B0H						
Resume	Write	X	D0H						
Read Lock Bit Status	Write	X	71H	Read	BA	DQ6 6)			
Lock Bit Program / Confirm 7)	Write	X	77H	Write	BA	D0H			
Erase All Unlocked Blocks	Write	X	A7H	Write	X	D0H			
Sleep 8)	Write	X	F0H						

1) In the word-wide mode, upper byte data (F-DQ8~F-DQ15) is ignored.
2) IA=ID Code Address : F-A0=VIL (Manufacturer's Code) : F-A0=VIH (Device Code), ID=ID Code,
F-BYTE# =VIL : F-A-1, F-A1~F-A18 = VIL, F-BYTE# =VIH : F-A1~F-A18 = VIL
3) SRD = Status Register Data
4) WA=Write Address, WD=Write Data.
F-BYTE# =VIL : Write Address and Write Data must be provided sequentially from 00H to FFH for F-A-1~A6.
Page size is 256Byte (256byte x 8bit), F-BYTE# =VIH : Write Address and Write Data must be provided
sequentially from 00H to 7FH for F-A0~F-A6. Page size is 128word (128word x 16bit).
5) BA = Block Address
6) DQ6 provides Block Lock Status, DQ6 = 1 : Block Unlock, DQ6 = 0 : Block Locked.
7) Must be set F-RP# to VHH and F-WP# to VIH.
8) Sleep command (F0H) put the device into the sleep mode after completing the current operation. The active current is reduced to deep power -down levels.
The Read Array command (FFH) must be written to get the device out of sleep mode.

BLOCK LOCKING

F-RP#	F-WP1#	F-WP2#	Boot Block	Parameter Block	Main Block	Lock Bit	Write Protection Provided
VHH	x	x	Unlock	Unlock	Unlock	Unlock	All Blocks/LockBits Unlocked (Erase/Program enable)
VIH	VIH	VIH	Unlock	Unlock	Unlock	Unlock	All Blocks/LockBits Unlocked (Erase/Program enable)
VIH	VIH	VIL	Lock	Depend on Lock Bit data1)	Lock	Lock	Boot block and Main block block (hard)locked, and Parameter block locked by Lock Bit.
VIH	VIL	VIH	Lock	Depend on Lock Bit data 1)	Depend on Lock Bit data 1)	Lock	Boot block (hard)locked, and other blocks locked by Lock Bit.
VIH	VIL	VIL	Lock	Lock	Lock	Lock	All Blocks/LockBits (hard)locked
VIL	x	x	Lock	Lock	Lock	Lock	All Blocks/LockBits locked (Deep Power Down Mode)

1) When the Lock bit is "0", its block cannot be programed and erased.
Lock bit is set to "0" by LOCK BIT PROGRAM.
Locked bit("0") is cleared to "1" with block memory by BLOCK ERASE on setting unlock mode.
2) F-DQ6 provides Lock Status of each block after writing the Read Lock Status command(71H).
3) F-WP#(1,2) pin must not be switched during performing Read/Write operations or WSM Busy (WSMS=0).

STATUS REGISTER

Symbol	Status	Definition	
		"1"	"0"
SR.7 (DQ7)	Write State Machine Status	Ready	Busy
SR.6 (DQ6)	Suspend Status	Suspended	Operation in Progress / Completed
SR.5 (DQ5)	Erase Status	Error	Successful
SR.4 (DQ4)	Program Status	Error	Successful
SR.3 (DQ3)	Block Status after Program	Error	Successful
SR.2 (DQ2)	*Reserved*	-	-
SR.1 (DQ1)	*Reserved*	-	-
SR.0 (DQ0)	Device Sleep Status	Device in Sleep	Device Not in Sleep

*The F-RY/BY# is an open drain output pin and indicates status of the internal WSM. When low,it indicates that the WSM is Busy performing an operation.
A pull-up resistor of 10K-100K Ohms is required to allow the F-RY/BY# signal to transition high indicating a Ready WSM condition.

*F-DQ3 indicates the block status after the page programming. When F-DQ3 is "1", the page has the over-programed cell . If over-program occures, the device is block fail. However if F-DQ3 is "1", please try the block erase to the block. The block may revive.

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M6MFB/T16S2TP

16777216-BIT (2M x 8-BIT/1M x 16-BIT)
CMOS 3.3V-ONLY FLASH MEMORY

DEVICE IDENTIFIER CODE

Code \ Pins	F-A0	F-DQ7	F-DQ6	F-DQ5	F-DQ4	F-DQ3	F-DQ2	F-DQ1	F-DQ0	Hex. Data
Manufacturer Code	VIL	0	0	0	1	1	1	0	0	1CH
Device Code (-T)	VIH	0	1	1	0	0	0	1	0	62H
Device Code (-B)	VIH	0	1	1	0	0	1	0	0	64H

In the word-wide mode, F-DQ15-8 = 00H.
F-A9 = VHH Mode : F-A9 = 11.4V~12.6V Set F-A9 to VHH min.200ns before falling edge of F-CE in ready status. Min.200ns after return to VIH ,device can't be accessed.
F-A1~F-A8, F-A10~F-A18, F-CE#,F-OE# = VIL, F-WE# = VIH
F-DQ15/A-1 = VIL (F-BYTE# = L)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Max	Unit
F-Vcc	Vcc voltage (Flash Memory)	With respect to Ground	-0.2	4.6	V
VI1	All input or output voltage except Vcc,A9,RP# 1)		-0.6	4.6	V
VI2	A9,RP# supply voltage		-0.6	14.0	V
Ta	Ambient temperature		-20	85	°C
Tbs	Temperature under bias		-30	95	°C
Tstg	Storage temperature		-65	125	°C
I OUT	Output short circuit current			100	mA

1) Minimum DC voltage is -0.5V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is Vcc+0.5V which, during transitions, may overshoot to Vcc+1.5V for periods <20ns.

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
CIN	Input capacitance (Address, Control Pins)	Ta = 25°C, f = 1MHz, Vin = Vout = 0V			8	pF
COUT	Output capacitance				12	pF

DC ELECTRICAL CHARACTERISTICS (Ta = -20 ~ 85°C, Vcc = 2.7V ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ1)	Max	
ILI	Input leakage current	0V ≤ VIN ≤ F-VCC			±1.0	µA
ILO	Output leakage current	0V ≤ VOUT ≤ F-VCC			±10	µA
ISB1	Vcc standby current	F-Vcc=3.6V, VIN=VIL/VIH, F-CE#=F-RP#=F-WP1,2#=VIH		50	200	µA
ISB2		F-Vcc=3.6V,VIN=F-GNDorF-Vcc,F-CE#=F-RP#=F-WP1,2#=F-Vcc±0.3V		0.1	5	µA
ISB3	Vcc deep powerdown current	F-VCC = 3.6V, VIN=VIL/VIH, F-RP# = VIL		5	15	µA
ISB4		F-Vcc = 3.6V, VIN=F-GND or F-Vcc, F-RP# =F-GND±0.3V		0.1	5	µA
ICC1	Vcc read current for Word or Byte	F-VCC = 3.6V, VIN=VIL/VIH, F-CE# = VIL, F-RP# = F-OE# = VIH, f = 5MHz, IOUT = 0mA		7	25	mA
ICC2	Vcc Write current for Word or Byte	F-Vcc=3.6V, VIN=VIL/VIH, F-CE#=F-WE#=VIL, F-RP#=F-OE#=VIH			25	mA
ICC3	Vcc program current	F-Vcc = 3.6V, VIN=VIL/VIH, F-CE# = F-RP# =F-WP1,2# = VIH			30	mA
ICC4	Vcc erase current	F-Vcc = 3.6V, VIN=VIL/VIH, F-CE# = F-RP# =F-WP1,2# = VIH			40	mA
ICC5	Vcc suspend current	F-Vcc = 3.6V, VIN=VIL/VIH, F-CE# = F-RP# =F-WP1,2# = VIH			200	µA
ICC6	Automatic power saving	F-Vcc = 3.6V, VIN=F-GND or F-Vcc		0.1	5	µA
IRP	F-RP# block unlock current	F-RP# = VIHH max			100	µA
IID	F-A9 intelligent identifier current	F-A9 = VID max			100	µA
VIHH	F-RP# block unlock voltage		11.4	12.0	12.6	V
VID	F-A9 intelligent identifier voltage		11.4	12.0	12.6	V
VIL	Input low voltage		– 0.5		0.8	V
VIH	Input high voltage		2.0		Vcc+0.5	V
VOL	Output low voltage	IOL = 5.8mA			0.45	V
VOH1	Output high voltage	IOH = –2.5mA	0.85Vcc			V
VOH2		IOH = –100µA	Vcc–0.4			V
VLKO	Low Vcc Lock-Out voltage 2)		1.5		2.5	V

All currents are in RMS unless otherwise noted.
1) Typical values at Vcc=3.3V, Ta=25°C
2) To protect against initiation of write cycle during Vcc power-up/ down, a write cycle is locked out for Vcc less than VLKO.
If Vcc is less than VLKO, Write State Machine is reset to read mode. When the Write State Machine is in Busy state, if Vcc is less than VLKO, the alteration of memory contents may occur.

AC ELECTRICAL CHARACTERISTICS (Ta = -20 ~ 85°C, Vcc = 2.7V ~ 3.6V, unless otherwise noted)

Read-Only Mode

Symbol		Parameter	Limits			Unit
			Min	Typ	Max	
t_{RC}	t_{AVAV}	Read cycle time	110			ns
$t_{a(AD)}$	t_{AVQV}	Address access time			110	ns
$t_{a(CE)}$	t_{ELQV}	Chip enable access time			110	ns
$t_{a(OE)}$	t_{GLQV}	Output enable access time			55	ns
t_{CLZ}	t_{ELQX}	Chip enable to output in low-Z	0			ns
$t_{DF(CE)}$	t_{EHQZ}	Chip enable high to output in high Z			30	ns
t_{OLZ}	t_{GLQX}	Output enable to output in low-Z	0			ns
$t_{DF(OE)}$	t_{GHQZ}	Output enable high to output in high Z			30	ns
t_{PHZ}	t_{PLQZ}	F-RP# low to output high-Z			300	ns
$t_{a(BYTE)}$	$t_{FL/HQV}$	F-BYTE# access time			110	ns
t_{BHZ}	t_{FLQZ}	F-BYTE# low to output high-Z			30	ns
t_{OH}	t_{OH}	Output hold from F-CE#, F-OE#, addresses	0			ns
t_{BCD}	$t_{ELFL/H}$	F-CE# low to F-BYTE# high or low			5	ns
t_{BAD}	$t_{AVFL/H}$	Address to F-BYTE# high or low			5	ns
t_{OEH}	t_{WHGL}	F-OE# hold from F-WE# high	110			ns
t_{PWH}	t_{PHEL}	F-RP# high recovery to F-CE# low	500			ns

Timing measurements are made under AC waveforms for read operations.

AC ELECTRICAL CHARACTERISTICS (Ta = -20 ~ 85°C, Vcc = 2.7V ~ 3.6V, unless otherwise noted)

Write Mode (WE control)

Symbol		Parameter	Limits			Unit
			Min	Typ	Max	
t_{WC}	t_{AVAV}	Write cycle time	110			ns
t_{AS}	t_{AVWH}	Address set-up time	50			ns
t_{AH}	t_{WHAX}	Address hold time	10			ns
t_{DS}	t_{DVWH}	Data set-up time	50			ns
t_{DH}	t_{WHDX}	Data hold time	10			ns
t_{CS}	t_{ELWL}	Chip enable set-up time	0			ns
t_{CH}	t_{WHEH}	Chip enable hold time	0			ns
t_{WP}	t_{WLWH}	Write pulse width	60			ns
t_{WPH}	t_{WHWL}	Write pulse width high	20			ns
t_{BS}	$t_{FL/HWH}$	Byte enable high or low set-up time	50			ns
t_{BH}	$t_{WHFL/H}$	Byte enable high or low hold time	110			ns
t_{BLS} / t_{WPS}	t_{PHHWH}	Block Lock set-up to write enable high	110			ns
t_{BLH} / t_{WPH}	t_{QVPH}	Block Lockhold from valid SRD	0			ns
t_{DAP}	t_{WHRH1}	Duration of auto-program operation		4	80	ms
t_{DAE}	t_{WHRH2}	Duration of auto-block erase operation		40	600	ms
t_{WHRL}	t_{WHRL}	Write enable high to F-RY/BY# low			110	ns
t_{PS}	t_{PHWL}	F-RP# high recovery to write enable low	500			ns

Read timing parameters during command write operations mode are the same as during read-only operations mode.
Typical values at F-Vcc=3.3V, Ta=25°C

AC ELECTRICAL CHARACTERISTICS (Ta = -20 ~ 85°C, Vcc = 2.7V ~ 3.6V, unless otherwise noted)

Write Mode (CE control)

Symbol		Parameter	Limits			Unit
			Min	Typ	Max	
t_{WC}	t_{AVAV}	Write cycle time	110			ns
t_{AS}	t_{AVEH}	Address set-up time	50			ns
t_{AH}	t_{EHAX}	Address hold time	10			ns
t_{DS}	t_{DVEH}	Data set-up time	50			ns
t_{DH}	t_{EHDX}	Data hold time	10			ns
t_{WS}	t_{WLEL}	Write enable set-up time	0			ns
t_{WH}	t_{EHWH}	Write enable hold time	0			ns
t_{CEP}	t_{ELEH}	F-CE# pulse width	60			ns
t_{CEPH}	t_{EHEL}	F-CE# pulse width high	20			ns
t_{BS}	$t_{FL/HEH}$	Byte enable high or low set-up time	50			ns
t_{BH}	$t_{EHFL/H}$	Byte enable high or low hold time	110			ns
t_{BLS} / t_{WPS}	t_{PHHEH}	Block Lock set-up to write enable high	110			ns
t_{BLH} / t_{WPH}	t_{QVPH}	Block Lockhold from valid SRD	0			ns
t_{DAP}	t_{EHRH1}	Duration of auto-program operation		4	80	ms
t_{DAE}	t_{EHRH2}	Duration of auto-block erase operation		40	600	ms
t_{EHRL}	t_{EHRL}	F-CE# enable high to F-RY/BY# low			110	ns
t_{PS}	t_{PHEL}	F-RP# high recovery to write enable low	500			ns

Read timing parameters during command write operations mode are the same as during read-only operations mode.
Typical values at Vcc=3.3V, Ta=25°C

Erase and Program Performance

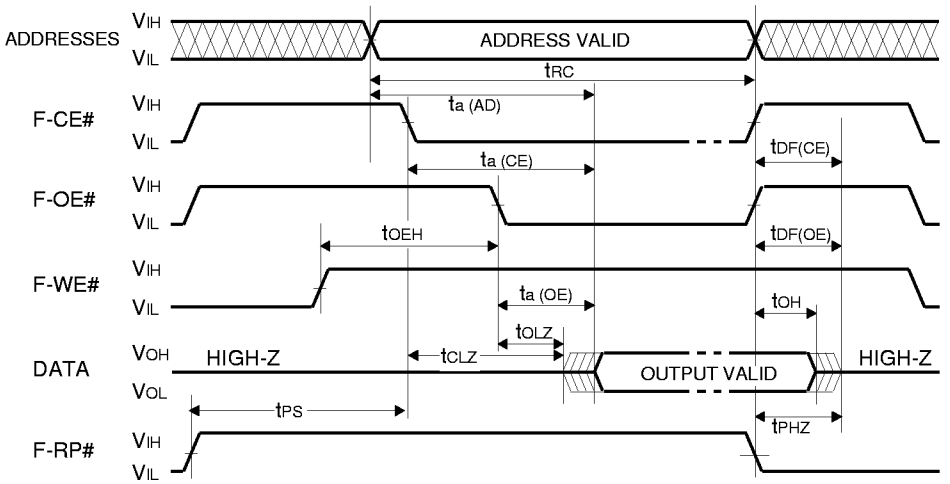
Parameter	Min	Typ	Max	Unit
Block Erase Time		40	600	ms
Main Block Write Time (Page Mode)		1.3	5	sec
Page Write Time		4	80	ms

Vcc Power Up / Down Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{VCS}	F-RP =V_{IH} set-up time from Vccmin	2			µs

During power up/down, by the noise pulses on control pins, the device has possibility of accidental erasure or programming.
The device must be protected against initiation of write cycle for memory contens during power up/down.
The delay time of min.2usec is always required before read operation or write operation is initiated from the time Vcc reaches Vccmin during power up/down. By holding RP# V_{IL}, the contens of memory is protected during Vcc power up/down.
During power up, RP# must be held V_{IL} for min.2us from the time Vcc reaches Vccmin.
During power down, RP# must be held V_{IL} until Vcc reaches GND.
RP# doesn't have latch mode ,so RP# must be held V_{IH} during read operation or erase/program operation.

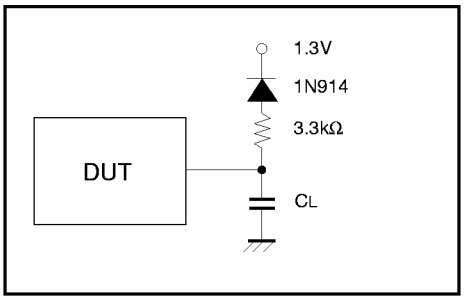
AC WAVEFORMS FOR READ OPERATION AND TEST CONDITIONS



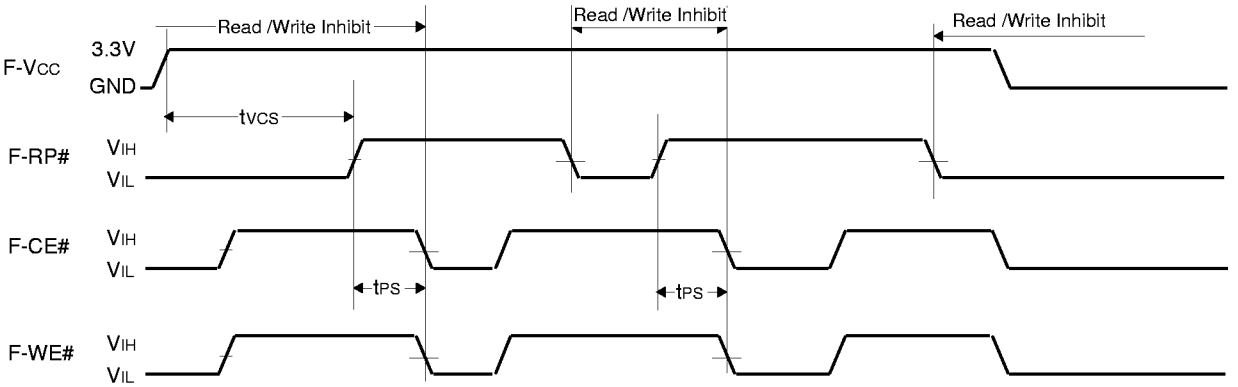
TEST CONDITIONS FOR AC CHARACTERISTICS

Test Configuration		F-Vcc=2.7V ~ 3.6V
Input voltage	V_{IL}	0V
	V_{IH}	3.0V
Input rise and fall times (10%-90%)		5ns
Reference voltage at timing measurement		1.5V
Capacitance Load value	CL	100pF

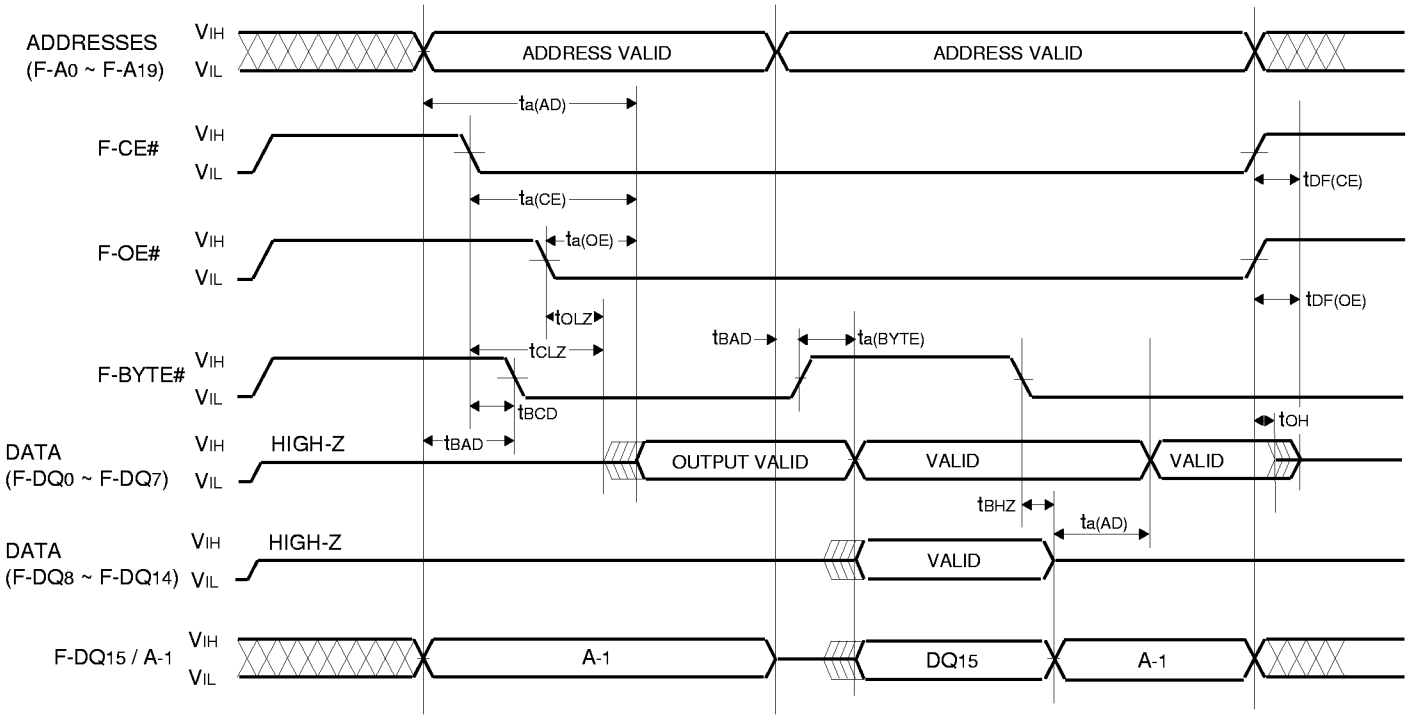
Output load : 1TTL gate + CL
or



Vcc POWER UP / DOWN TIMING



BYTE# AC WAVEFORMS FOR READ OPERATION

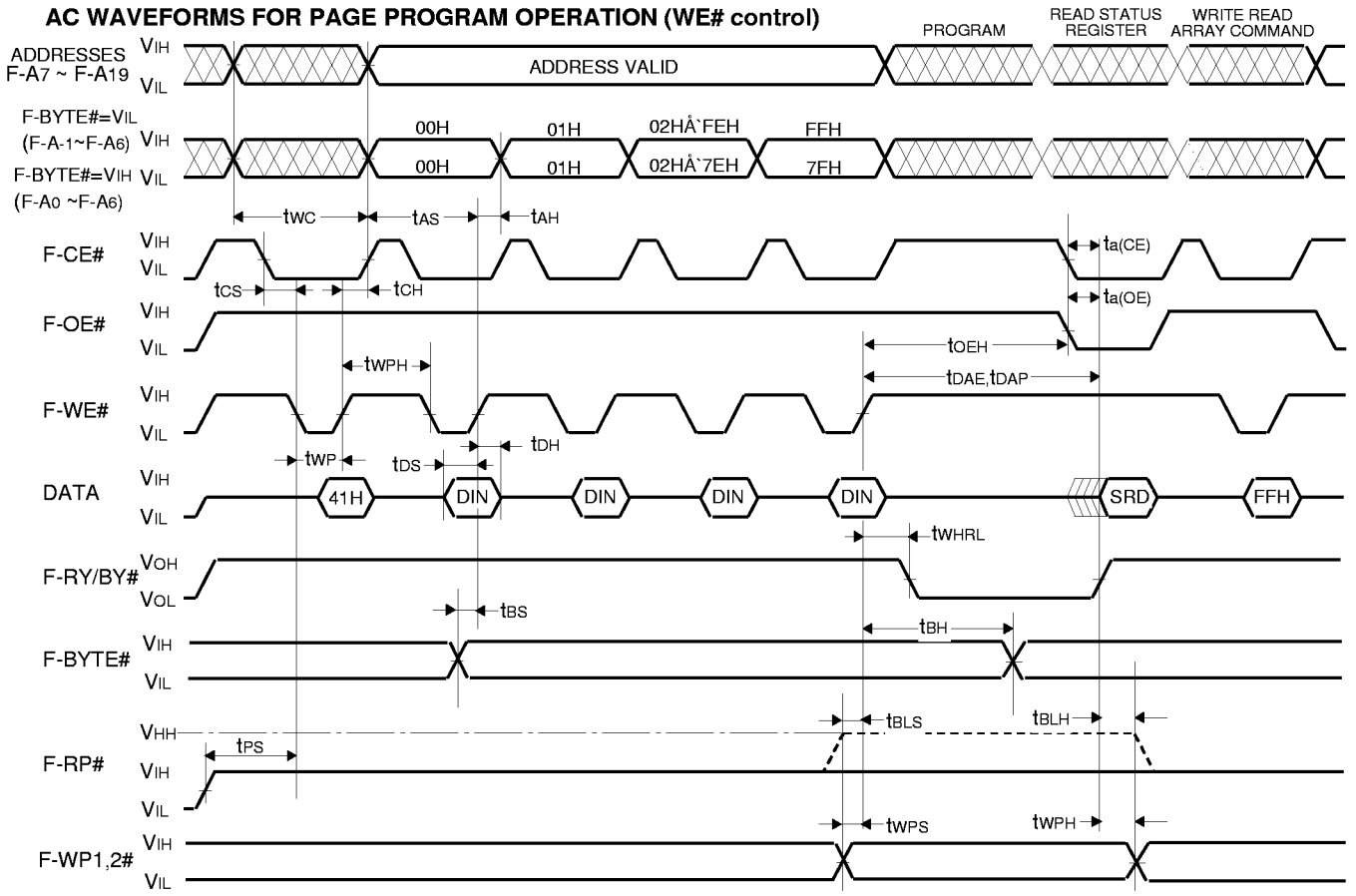


When F-BYTE#=V_{IH}, F-CE#=F-OE#=V_{IL} , DQ_{15}/A_{-1} is output status. At this time, input signal must not be applied.

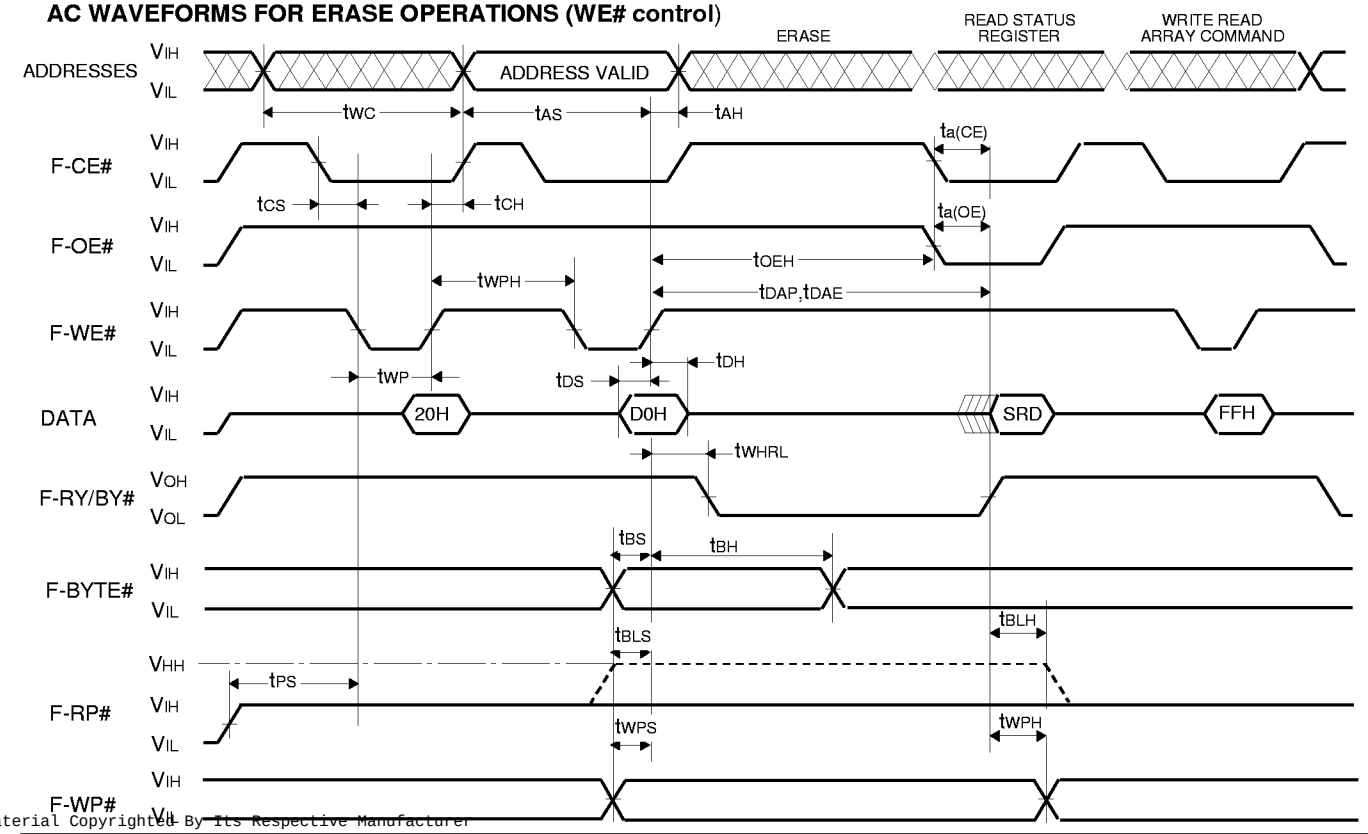
PRELIMINARY

Notice : This is not a final specification.
Some parametric limits are subject to change.

AC WAVEFORMS FOR PAGE PROGRAM OPERATION (WE# control)



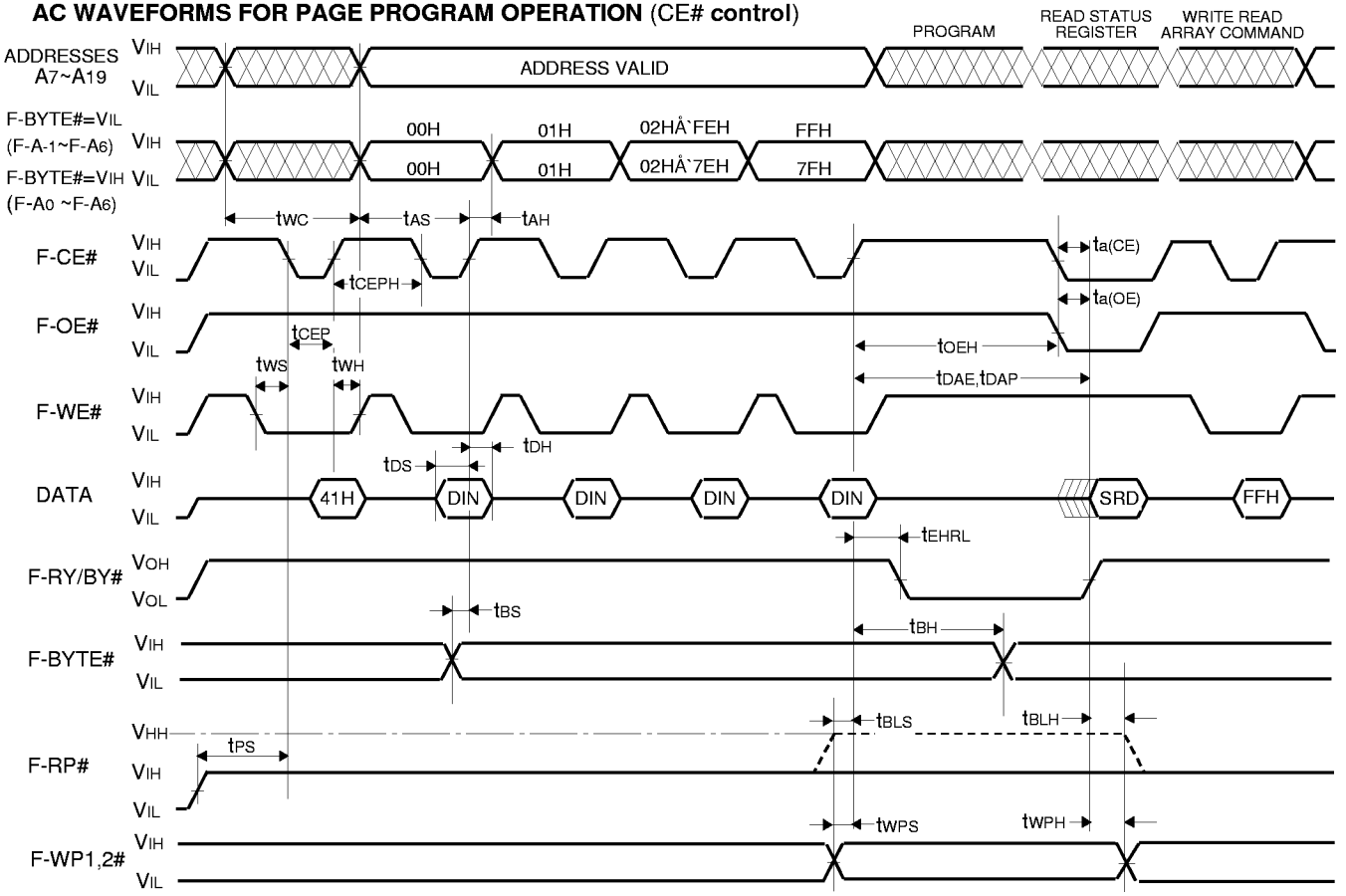
AC WAVEFORMS FOR ERASE OPERATIONS (WE# control)



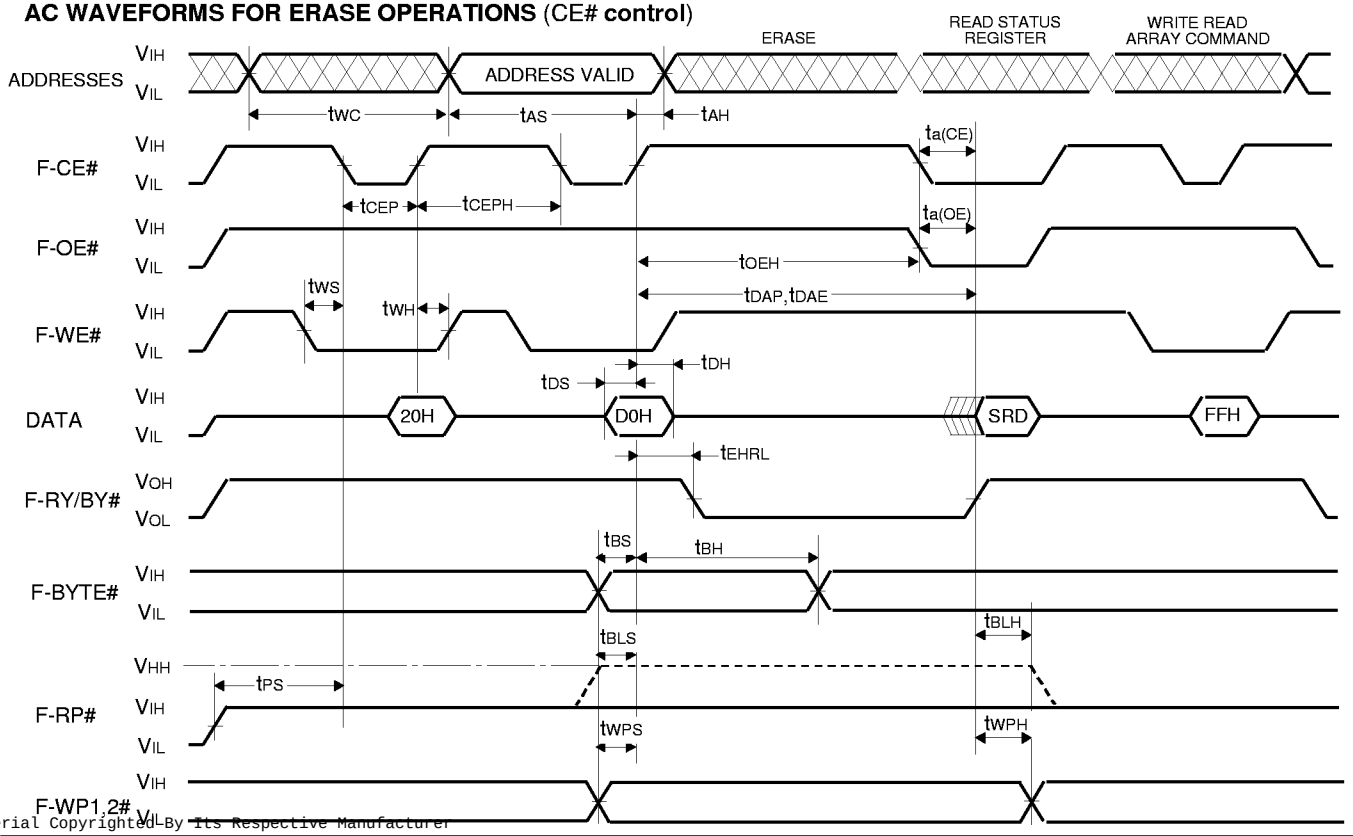
PRELIMINARY

Notice : This is not a final specification.
Some parametric limits are subject to change.

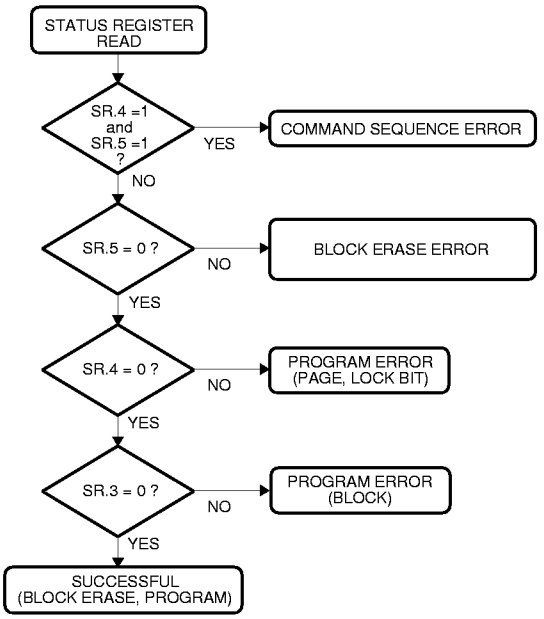
AC WAVEFORMS FOR PAGE PROGRAM OPERATION (CE# control)



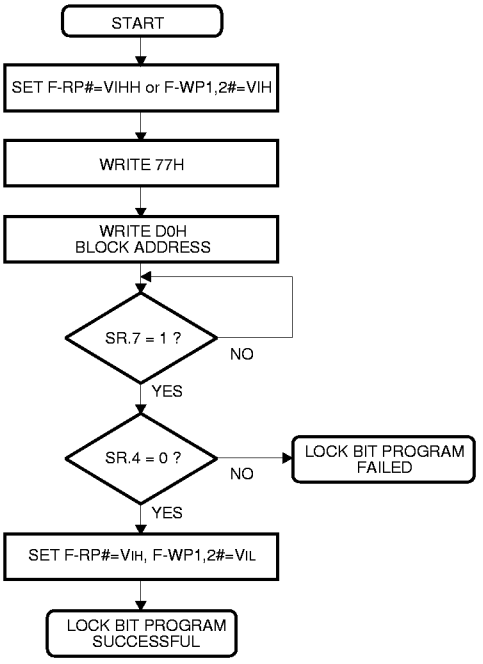
AC WAVEFORMS FOR ERASE OPERATIONS (CE# control)



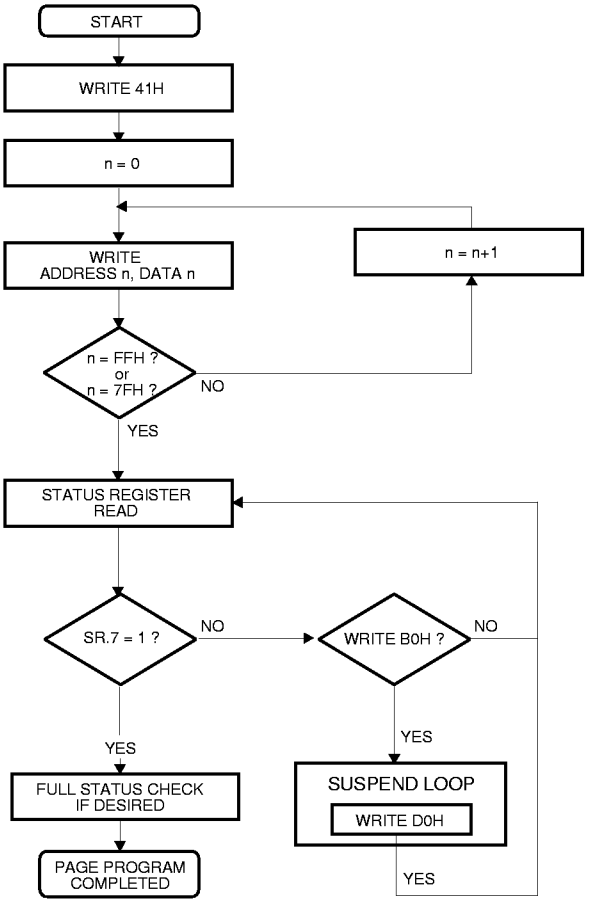
FULL STATUS CHECK PROCEDURE



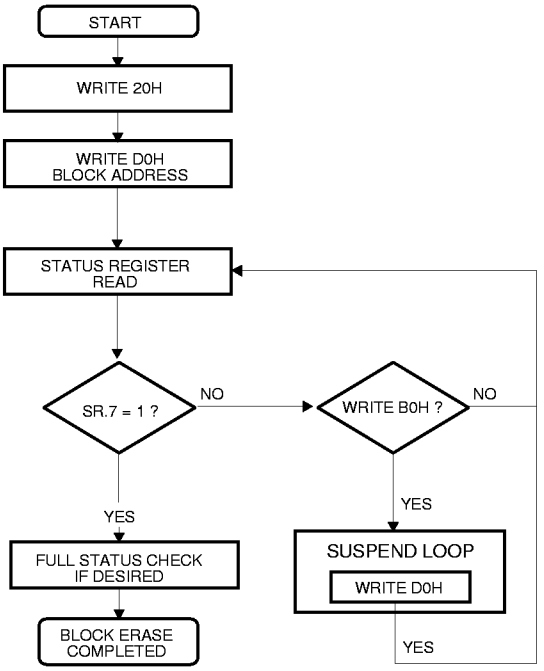
LOCK BIT PROGRAM FLOW CHART



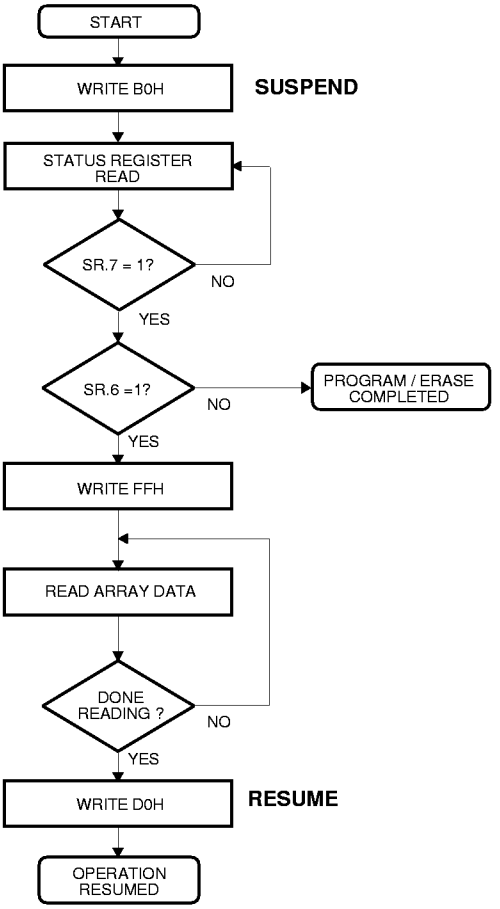
PAGE PROGRAM FLOW CHART



BLOCK ERASE FLOW CHART



SUSPEND / RESUME FLOW CHART



M6MFB/T16S2TP

2097152-BIT (256k x 8-BIT)
CMOS STATIC RAM

PRELIMINARY

Notice : This is not a final specification.
Some parametric limits are subject to change.

FUNCTION

The SRAM of the M6MFT/B16S2TP operation mode is determined by a combination of the device control inputs S-S1#,S-S2,S-W# and S-OE#.

Each mode is summarized in the function table.

A write cycle is executed whenever the low level S-W# overlaps with the low level S-S1# and the high level S-S2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of S-W#,S-S1# or S-S2,whichever occurs first,requiring the set-up and hold time relative to these edge to be maintained. The output enable input S-OE# directly controls the output stage. Setting the S-OE# at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

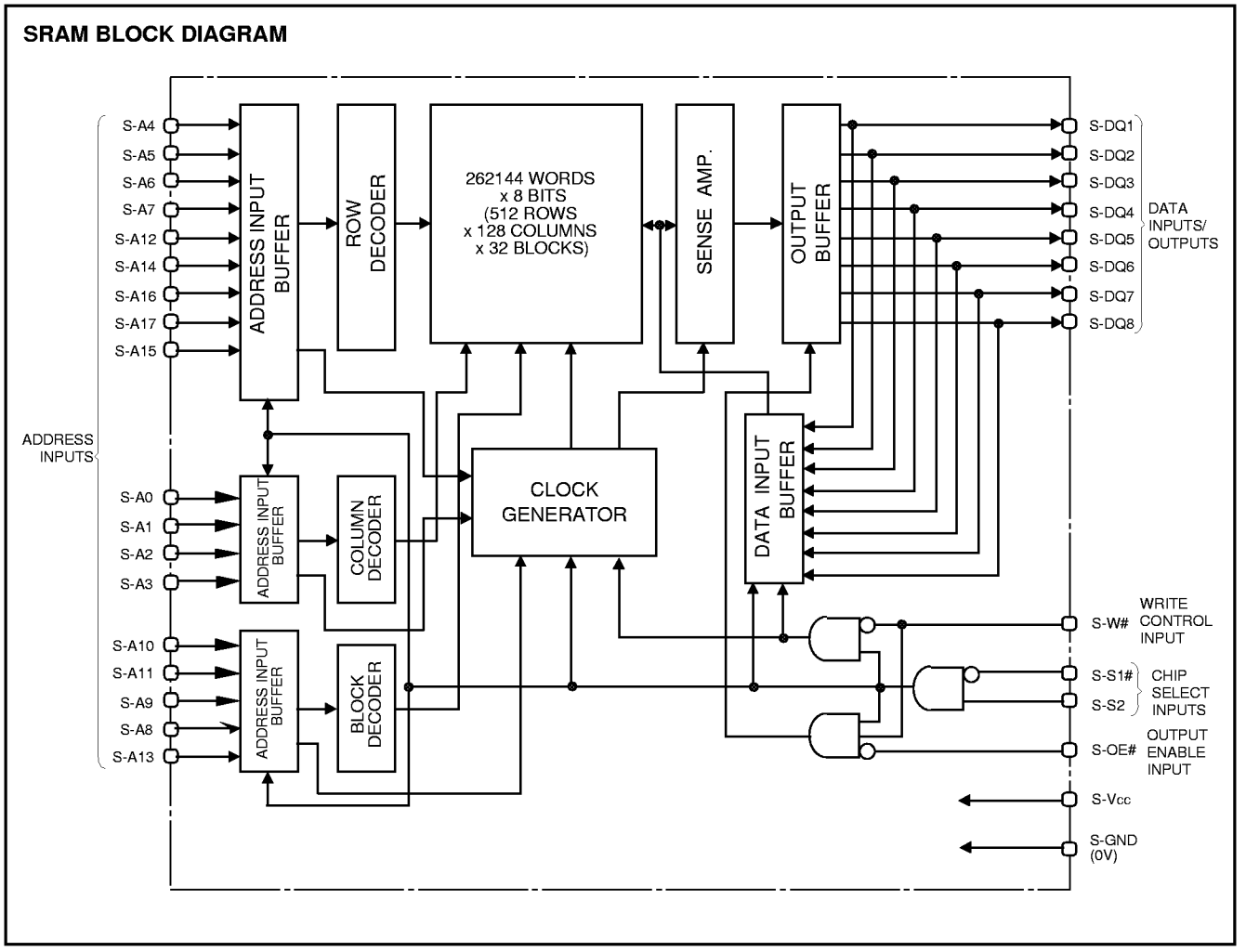
A read cycle is executed by setting S-W# at a high level and S-OE# at a low level while S-S1# and S-S2 are in an active state(S-S1#=L,S-S2=H).

When setting S-S1# at a high level or S-S2 at a low level, the chip are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high- impedance state, allowing OR-tie with other chips and memory expansion by S-S1# and S-S2. The power supply current is reduced as low as the stand-by current which is specified as ICC3 or ICC4, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

S-S1#	S-S2	S-W#	S-OE#	Mode	DQ	Icc
X	L	X	X	Non selection	High-impedance	Stand-by
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active

SRAM BLOCK DIAGRAM



ABSOLUTE MAXIMUM RAPINGS

Symbol	Parameter	Conditions	Ratings	Unit
S-Vcc	Supply voltage (SRAM)	With respect to GND	– 0.3* ~ 4.6	V
V_I	Input voltage		– 0.3* ~ Vcc + 0.5 (Max 4.6)	V
V_O	Output voltage		0 ~ Vcc	V
P_d	Power dissipation	Ta=25°C	700	mW
T_{opr}	Operating temperature		-20 ~ 85	°C
T_{stg}	Storage temperature		– 65 ~ 150	°C

* –3.0V in case of AC (Pulse width ≤ 30ns)

DC ELECTRICAL CHARACTERISTICS (Ta=-20 ~ 85°C, Vcc=2.7V~3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.0		Vcc +0.3V	V
V_{IL}	Low-level input voltage			–0.3*		0.6	V
V_{OH1}	High-level output voltage 1	I_{OH}= –0.5mA		2.4			V
V_{OH2}	High-level output voltage 2	I_{OH}= –0.05mA		Vcc -0.5V			V
V_{OL}	Low-level output voltage	I_{OL}=2mA				0.4	V
I_I	Input current	V_I=0 ~ Vcc				±1	µA
I_O	Output current in off-state	S-S_1=V_{IH} or S-S_2=V_{IL} or S-OE=V_{IH} $V_{I/O}$=0 ~ S-Vcc				±1	µA
I_{CC1}	Active supply current (MOS level input)	S-S_1 ≤ 0.2V, S-S_2 ≥ Vcc - 0.2V other inputs ≤ 0.2V or ≥S-Vcc - 0.2V Output-open(duty 100%)	10MHz	-	20	25	mA
			5MHz	-	10	13	
			1MHz	-	3	5	
I_{CC2}	Active supply current (TTL level input)	S-S_1=V_{IL},S-S_2=V_{IH}, other inputs=V_{IH} or V_{IL} Output-open(duty 100%)	10MHz	-	22	27	mA
			5MHz	-	12	15	
			1MHz	-	3	5	
I_{CC3}	Stand-by current	1) S-S_2 ≤ 0.2V,other inputs=0 ~ S-Vcc 2) S-S_1 ≥ S-Vcc - 0.2V, S-S_2 ≥ S-Vcc - 0.2V other inputs=0 ~ S-Vcc	-20 ~ +85°C	-	-	40	µA
			-20 ~ +40°C	-	-	5	
			+25°C	-	0.3	2	
I_{CC4}	Stand-by current	S-S_1=V_{IH} or S-S_2=V_{IL},other inputs=0 ~ S-Vcc		-	-	0.33	mA

* –3.0V in case of AC (Pulse width ≤ 30ns)

CAPACITANCE (Ta=-20 ~ 85°C, Vcc=2.7V ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			7	pF
C_O	Output capacitance	V_O=GND,V_O=25mVrms, f=1MHz			9	pF

Note 1: Direction for current flowing into an IC is positive (no mark).
2: Typical value is Vcc = 3V, Ta = 25°C

AC ELECTRICAL CHARACTERISTICS (Ta=-20 ~ 85°C, Vcc=2.7V ~ 3.6V, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

V_{CC} ..... 2.7V ~ 3.6V
Input pulse level ..... V_{IH}=2.2V, V_{IL}=0.4V
Input rise and fall time 5ns
Reference level ..... V_{OH}=V_{OL}=1.5V
Output loads ..... Fig.1, C_L = 30pF
C_L = 5pF (for t_{en},t_{dis})
Transition is measured ±500mV from steady state voltage. (for t_{en},t_{dis})

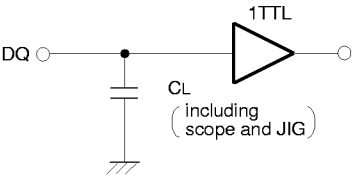


Fig.1 Output load

(2) READ CYCLE

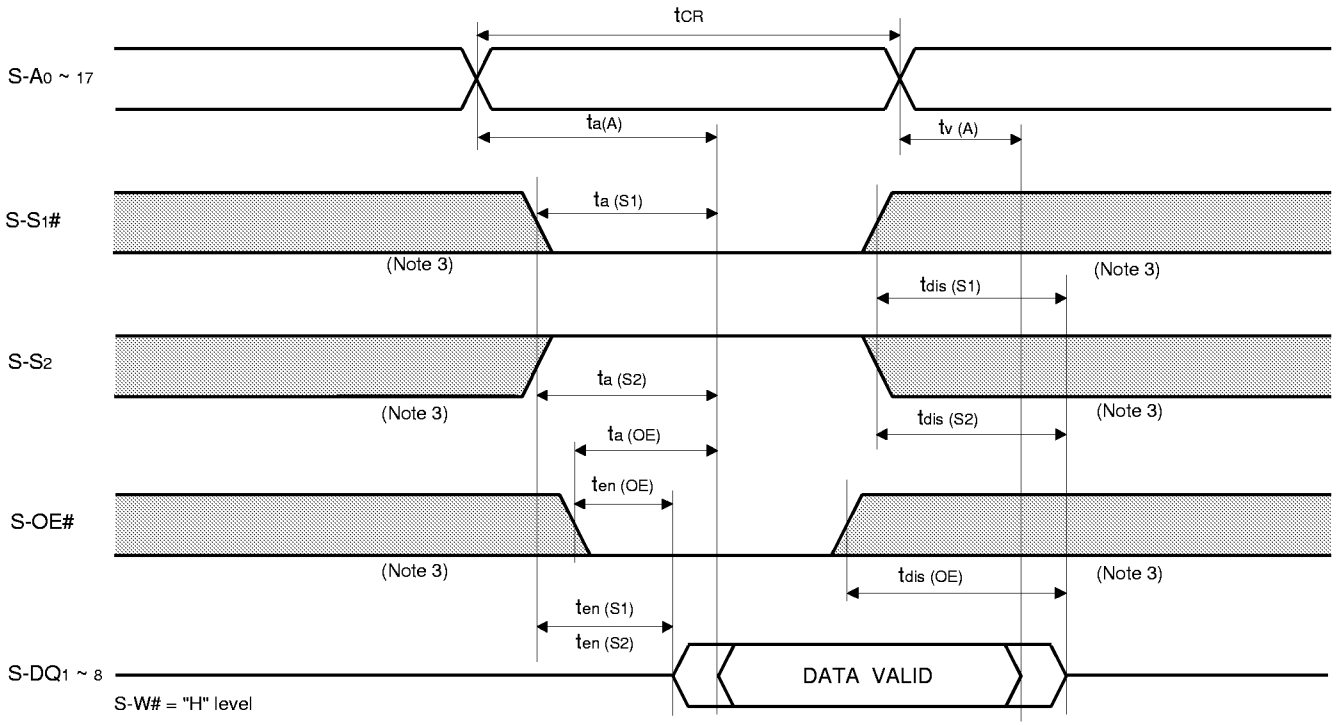
Symbol	Parameter	Limits		Unit
		Min	Max	
t_{CR}	Read cycle time	110		ns
$t_{a(A)}$	Address access time		110	ns
$t_{a(S1)}$	Chip select 1 access time		110	ns
$t_{a(S2)}$	Chip select 2 access time		110	ns
$t_{a(OE)}$	Output enable access time		55	ns
$t_{dis(S1)}$	Output disable time after S-S_1# high		40	ns
$t_{dis(S2)}$	Output disable time after S-S_2 low		40	ns
$t_{dis(OE)}$	Output disable time after S-OE# high		40	ns
$t_{en(S1)}$	Output enable time after S-S_1# low	10		ns
$t_{en(S2)}$	Output enable time after S-S_2 high	10		ns
$t_{en(OE)}$	Output enable time after S-OE# low	5		ns
$t_{V(A)}$	Data valid time after address	10		ns

(3) WRITE CYCLE

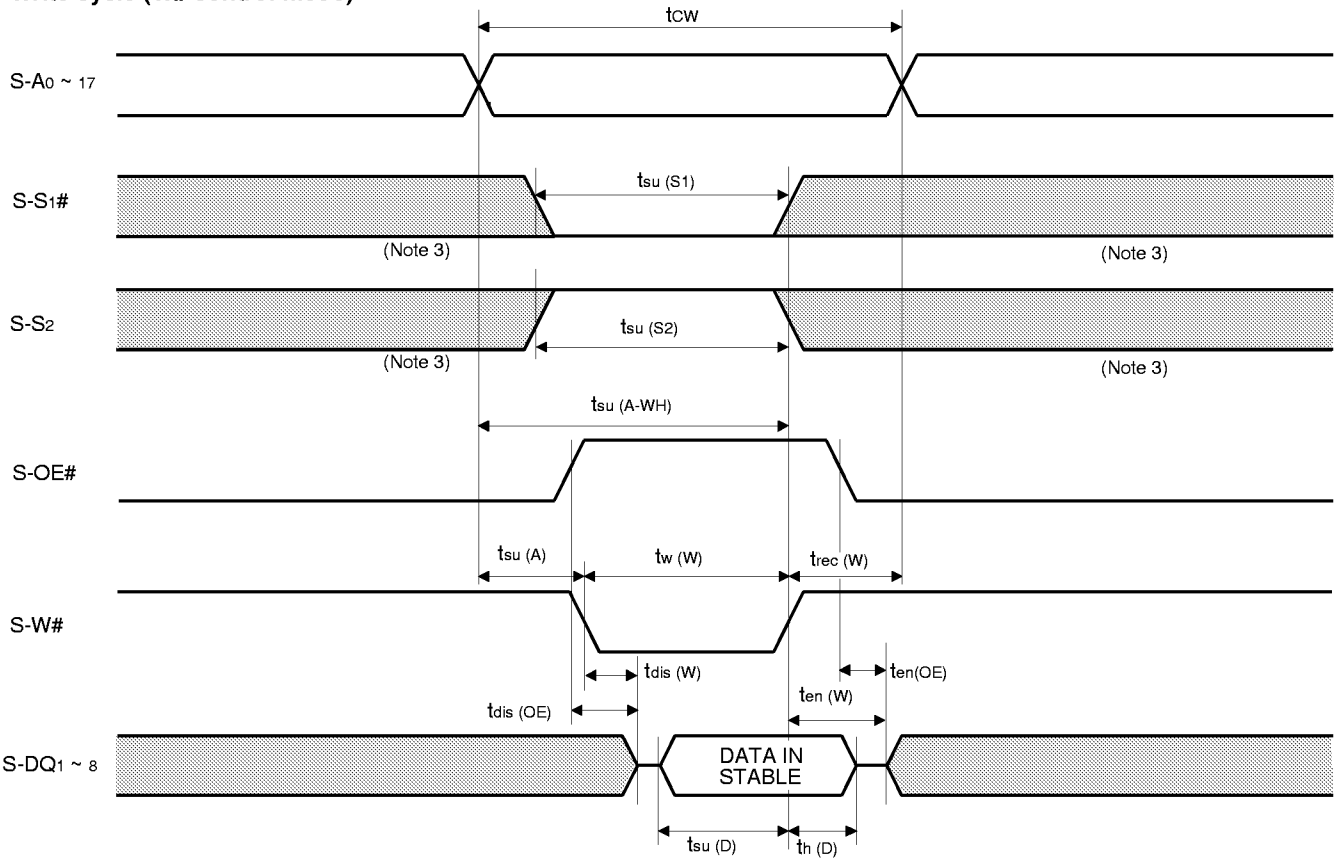
Symbol	Parameter	Limits		Unit
		Min	Max	
t_{CW}	Write cycle time	110		ns
$t_{w(W)}$	Write pulse width	85		ns
$t_{su(A)}$	Address setup time	0		ns
$t_{su(A-WH)}$	Address setup time with respect to S-W#	100		ns
$t_{su(S1)}$	Chip select 1 setup time	100		ns
$t_{su(S2)}$	Chip select 2 setup time	100		ns
$t_{su(D)}$	Data setup time	45		ns
$t_{h(D)}$	Data hold time	0		ns
$t_{rec(W)}$	Write recovery time	0		ns
$t_{dis(W)}$	Output disable time from S-W# low		40	ns
$t_{dis(OE)}$	Output disable time from S-OE# high		40	ns
$t_{en(W)}$	Output enable time from S-W# high	5		ns
$t_{en(OE)}$	Output enable time from S-OE# low	5		ns

(4) TIMING DIAGRAMS

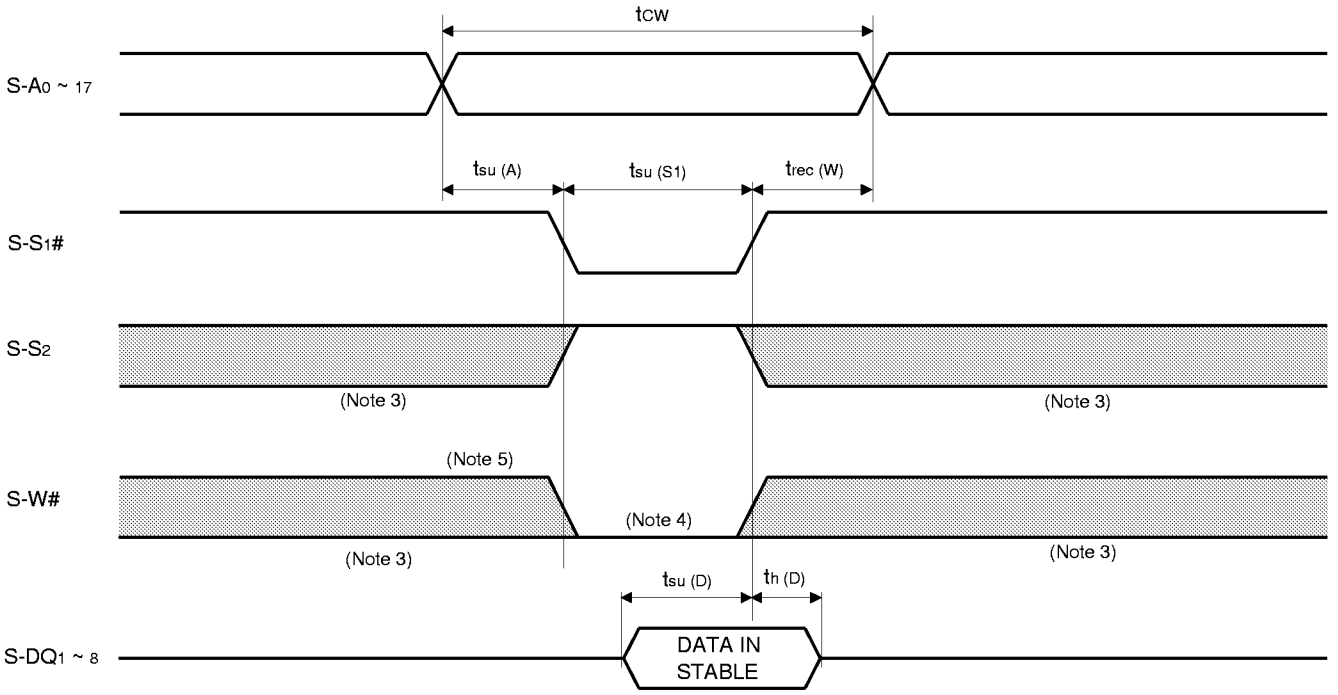
Read cycle



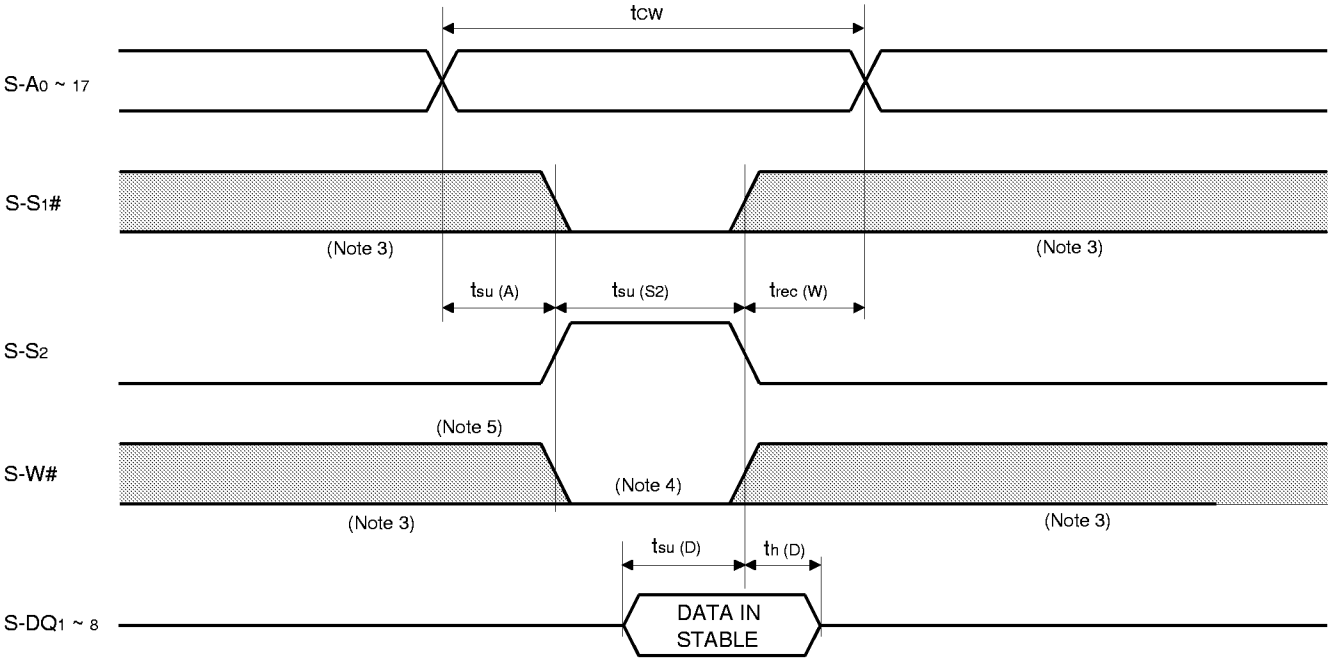
Write cycle (W# control mode)



Write cycle (S_1# control mode)



Write cycle (S_2 control mode)



Note 3: Hatching indicates the state is "don't care".
4: Writing is executed while S-S_2 high overlaps S-S_1# and S-W# low.
5: When the falling edge of S-W# is simultaneously or prior to the falling edge of S-S_1# or rising edge of S-S_2, the outputs are maintained in the high impedance state.
6: Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (Ta = -20 ~ 85°C, unless otherwise noted)

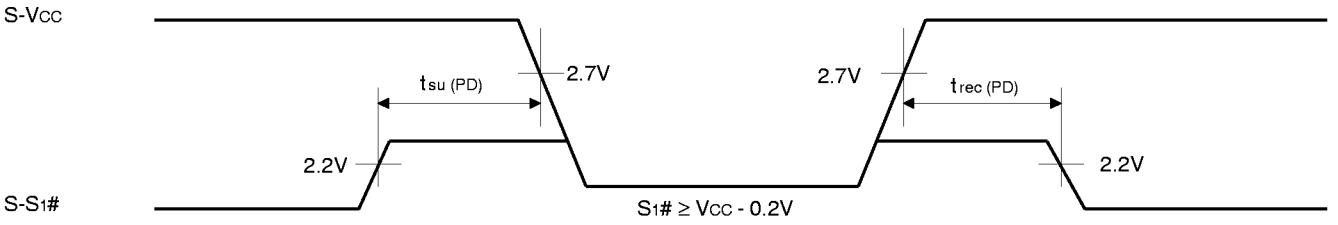
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC\ (PD)}$	Power down supply voltage			2			V
$V_{I\ (S1\#)}$	Chip select input S-$S_{1\#}$			2.0			V
$V_{I\ (S2)}$	Chip select input S-S_2					0.2	V
$I_{CC\ (PD)}$	Power down supply current	S-V_{CC} = 3.0V 1) S-$S_2 \le$ 0.2V, other inputs = 0 ~ S-V_{CC} 2) $S_{1\#} \ge$ S-V_{CC} - 0.2V, $S_2 \ge$ S-V_{CC} - 0.2V other inputs = 0 ~ S-V_{CC}	-20~+85°C			30	µA
			-20~+40°C			3	
			+25°C		0.3	1	

(2) TIMING REQUIREMENTS (Ta = -20 ~ 85°C, unless otherwise noted)

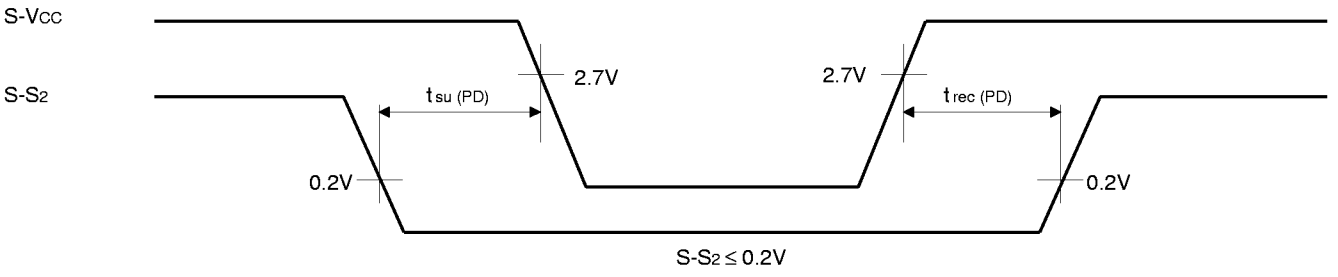
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su\ (PD)}$	Power down set up time		0			ns
$t_{rec\ (PD)}$	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

$S_{1\#}$ control mode



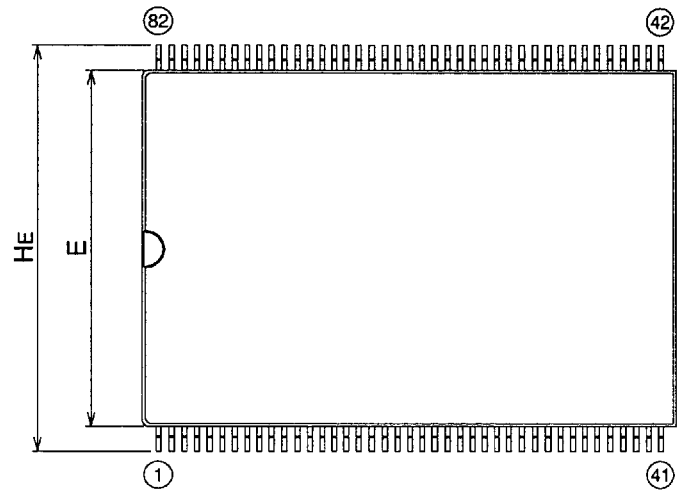
S_2 control mode

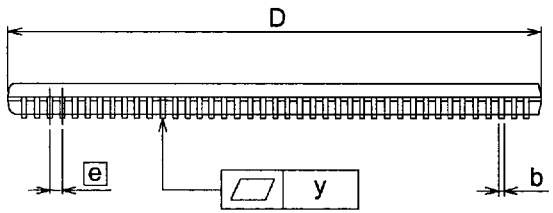


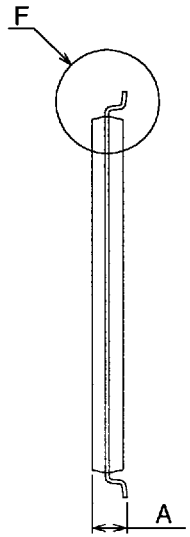
82PTA-B

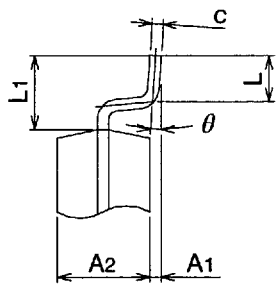
Plastic 82pin 11.5mm TSOP (II)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
–	–	0.47	Alloy 42

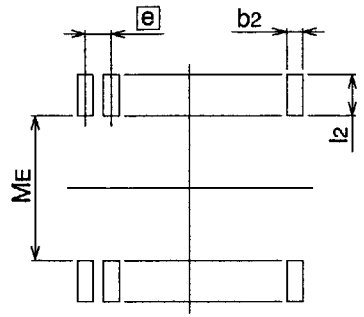








Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.2
A1	0.05	0.125	0.2
A2	–	1.0	–
b	0.11	0.16	0.26
c	0.105	0.125	0.175
D	16.9	17	17.1
E	11.4	11.5	11.6
e	–	0.4	–
HE	12.9	13.1	13.3
L	0.4	0.5	0.6
L1	–	0.8	–
y	–	–	0.08
θ	0°	–	10°
ME	–	11.7	–
l2	0.9	–	–
b2	–		–

Mar.'98