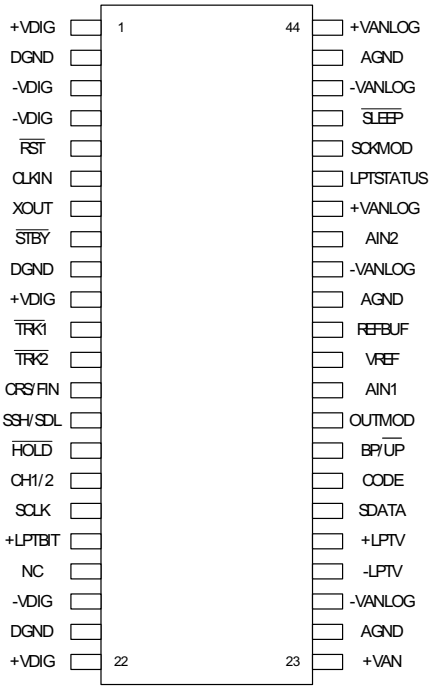
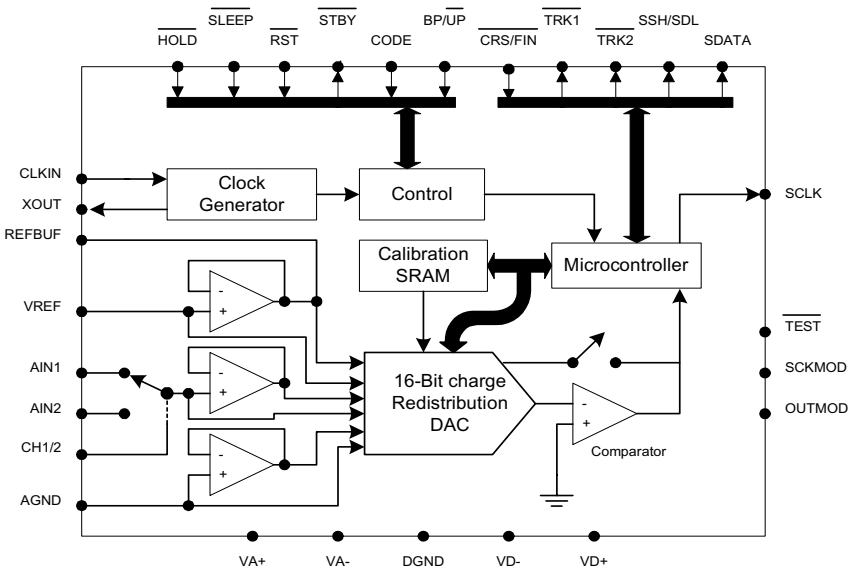
5102ALP

16-Bit, 20 KHz A/D Converter





FEATURES:

- Monolithic CMOS A/D converters
  - Inherent sampling architecture
  - 2-channel input multiplexer
  - Flexible serial output port
- Conversion time
  - 5102A: 40 µs
- Linearity error: ±0.001% FS
  - Guaranteed no missing codes
- Self-calibration maintains accuracy
  - Over time and temperature
- Fully latchup protected

DESCRIPTION:

Maxwell Technologies' 5102ALPRP is a 16-bit monolithic CMOS analog-to-digital converter capable of 20 kHz throughput. On-chip self-calibration achieves nonlinearity of ±0.001% of FS and guarantees 16-bit no missing codes over the entire specified temperature range. Offset and full-scale errors are minimized during the calibration cycle, eliminating the need for external trimming.

The 5102ALP each consist of a 2-channel input multiplexer, DAC, conversion and calibration microcontroller, clock generator, comparator, and serial communications port. The inherent sampling architecture of the device eliminates the need for an external track and hold amplifier.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while improving the TID performance in most space environments. This product is available with screening up to Maxwell Technologies self-defined Class K.

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TABLE 1. 5102ALP ABSOLUTE MAXIMUM RATINGS

(AGND, DGND = 0V, ALL VOLTAGES WITH RESPECT TO GROUND)

PARAMETER	SYMBOL	MIN	MAX	UNIT
DC Power Supplies: [1]				V
Positive Digital	VD+	-0.3	6.0	
Negative Digital	VD-	0.3	-6.0	
Positive Analog	VA+	-0.3	6.0	
Negative Analog	VA-	0.3	-6.0	
Input Current, Any Pin Except Supplies [2]	I_{IN}	--	±10	mA
Analog Input Voltage (AIN and V_{REF} pins)	V_{INA}	(VA-) -0.3	(VA+) 0.3	V
Digital Input Voltage	V_{IND}	-0.3	(VA+) 0.3	V
Ambient Operating Temperature	T_A	-15	55	°C
Storage Temperature	T_{STG}	-65	150	°C

1. In addition, VD+ must not be greater than (VA+) 0.3V.
2. Transient currents of up to 100 mA will not cause SCR latchup.

TABLE 2. 5102ALP RECOMMENDED OPERATING CONDITIONS

(AGND, DGND = 0V, ALL VOLTAGES WITH RESPECT TO GROUND)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
DC Power Supplies:					V
Positive Digital	VD+	4.5	5.0	VA+	
Negative Digital	VD-	-4.5	-5.0	-5.5	
Positive Analog	VA+	4.5	5.0	5.5	
Negative Analog	VA-	-4.5	-5.0	-5.5	
Analog Reference Voltage	VREF	2.5	4.5	(VA+) -0.5	V
Analog Input Voltage [1]	V_{AIN}				V
Unipolar		AGND	--	V_{REF}	
Bipolar		$-V_{REF}$	--	V_{REF}	

1. The 5102ALPRP can accept input voltage up to the analog supplies (VA+ and VA-). They will produce an output of all 1s for inputs above V_{REF} and all 0s for inputs below AGND in unipolar mode and $-V_{REF}$ in bipolar mode, with binary coding (CODE = low).

TABLE 3. ANALOG CHARACTERISTICS

($T_A = T_{MIN}$ TO T_{MAX}; VA+, VD+ = 5V; VA-, VD- = -5V; V_{REF} = 4.5V; FULL-SCALE INPUT SINEWAVE, 200 HZ; CLKIN = 1.6 MHz; f_S = 20 KHZ; BIPOLAR MODE; FRN MODE; AIN1 AND AIN2 TIED TOGETHER, EACH CHANNEL TESTED SEPARATELY; ANALOG SOURCE IMPEDANCE = 50 W WITH 1000 PF TO AGND UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Accuracy					
Resolution [1]	RES	16	--	--	Bits
Full Scale Error [2] Drift [3]	FSE	-- --	±1 ±2	±5 --	LSB DLSB
Unipolar Offset [2] Drift [3]	VOFF	-- --	±1 ±2	±5 --	LSB DLSB
Bipolar Offset [2] Drift [3]	BOFF	-- --	±2 ±2	±5 --	LSB DLSB
Bipolar Negative Full Scale Error [2] Drift [2]	BNFSE	-- --	±2 ±2	±5 --	LSB DLSB
Integral Nonlinearity	INL	--	--	±3	LSB
Differential Nonlinearity	DNL	--	±1	--	LSB
Dynamic Performance (Bipolar Mode)					
Peak Harmonic or Spurious Noise [2, 4]		94	100	--	dB
Total Harmonic Distortion [4]		--	0.002	--	%
Signal-to-Noise Ratio [2, 4] 0 dB Input -60 dB Input		 87 --	 90 30	 -- --	dB
Noise [5] Unipolar Mode Bipolar Mode		 -- --	 35 70	 -- --	µVrms
Analog Input					
Aperture Time		--	30	--	ns
Aperture Jitter		--	100	--	ps
Input Capacitance [6, 4] Unipolar Mode Bipolar Mode		 -- --	 335 215	 -- --	pF
Conversion and Throughput					
Conversion Time [7]	t_c	--	40.625	--	µs
Acquisition Time [8]	t_a	--	9.375	--	µs
Throughput [9, 10]	f_{tp}	--	20	--	kHz
Power Supplies					

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PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Power Supply Current [11]					mA
Positive Analog	I_{A+}	--	8.5	12	
Negative Analog	I_{A-}	--	-7.7	-11	
(SLEEP High) Positive Digital	I_{D+}	--	0.5	1.5	
Negative Digital	I_{D-}	--	-0.5	-1.5	
Power Consumption [11, 12]					mW
(SLEEP High)	P_{do}	--	85	130	
(SLEEP Low)	P_{ds}	--	45	--	
Power Supply Rejection [13]					dB
Positive Supplies	PSR	--	84	--	
Negative Supplies	PSR	--	84	--	

1. Minimum resolution for which no missing codes are guaranteed over the specified temperature range.
2. Applies after calibration at any temperature within the specified temperature range.
3. Total drift over specified temperature range after calibration at power-up at 25°C.
4. Guaranteed by characterization (5102A die).
5. Wideband noise aliased into the baseband. Referred to the input.
6. Applied only in the track mode. When converting or calibrating, input capacitance will not exceed 30 pF.
7. Conversion time scales directly to the master clock speed. The times shown are for synchronous, internal loopback (FRN mode). In PDT, RBT, and SSC modes, asynchronrous delay between the falling edge of HOLD and the start of conversion may add to the apparent conversion time. This delay will not exceed 1 master clock cycle + 140 ns.
8. The 5102ALPRP requires 6 clock cycles of coarse charge, followed by a minimum of 5.625 µs of fine charge. FRN mode allows 9 clock cycles for fine charge which provides for the minimum 5.625 µs with a 1.6 MHz clock; however, in PDT, RBT, or SSC modes, at clock frequencies less than 1.6 MHz, fine charge may be less than 9 clock cycles.
9. Throughput is the sum of the acquisition and conversion times. It will vary in accordance with conditions affecting acquisition and conversion times described above.
10. Typical value (measured).
11. All outputs unloaded. All inputs at VD+ or DGND.
12. Power consumption in the sleep mode applies with no master clock applied (CLKIN held high or low).
13. With 300 mV p-p, 1 kHz ripple applied to each supply separately in the bipolar mode. Rejection improves by 6 dB in the unipolar mode to 90 dB.

TABLE 4. 5102ALP SWITCHING CHARACTERISTICS

($T_A = T_{MIN}$ TO T_{MAX}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; INPUTS: LOGIC 0 = 0V, LOGIC 1 = VD+; C_L = 50 PF)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CLKIN Period [1, 2]	t_{clk}	0.5	--	10	µs
CLKIN Low Time	t_{clkl}	200	--	--	ns
CLKIN High Time	t_{clkh}	200	--	--	ns

TABLE 4. 5102ALP SWITCHING CHARACTERISTICS

($T_A = T_{MIN}$ TO T_{MAX}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; INPUTS: LOGIC 0 = 0V, LOGIC 1 = VD+; C_L = 50 PF)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Crystal Frequency [1, 2]	f_{xtal}	--	1.6	--	MHz
SLEEP Rising to Oscillator Stable [3]		--	20	--	ms
RST Pulse Width [4]	t_{rst}	150	--	--	ns
RST to STBY Falling	t_{drrs}	--	100	--	ns
RST Rising to STBY Rising	t_{cal}	--	2,882,040	--	tclk
CH1/2 Edge to TRK1, TRK2 Rising [5]	t_{drsh1}	--	80	--	ns
CH1/2 Edge to TRK1, TRK2 Falling [5]	t_{dfsh4}	--	--	$68t_{clk}$ + 260	ns
HOLD to SSH Falling [6]	t_{dfsh2}	--	60	--	ns
HOLD to TRK1, TRK2, Falling [6]	t_{dfsh1}	$66t_{clk}$	--	$68t_{clk}$ + 260	ns
HOLD to TRK1, TRK2, SSH Rising [6]	t_{drsh}	--	120	--	ns
HOLD Pulse Width [7]	t_{hold}	$1t_{clk}$ + 20	--	$63t_{clk}$	ns
HOLD to CH1/2 Edge [6]	t_{dhlri}	300	--	$64t_{clk}$	ns
HOLD Falling to CLKIN Falling [7]	t_{hcf}	275	--	$1t_{clk}$ + 10	ns
PDT and RBT Modes					
SCLK Input Pulse Period	t_{sclk}	1000	--	--	ns
SCLK Input Pulse Width Low	t_{sckll}	500	--	--	ns
SCLK Input Pulse Width High	t_{sclkh}	500	--	--	ns
SCLK Input Falling to SDATA Valid	t_{dss}	--	100	150	ns
HOLD Falling to SDATA Valid - PDT Mode	t_{dhs}	--	140	230	ns
TRK1, TRK2 Falling to SDATA Valid [8]	t_{dts}	--	65	125	ns
FRN and SSC Modes					
SCLK Output Pulse Width Low	t_{slkl}	--	$2t_{clk}$	--	t_{clk}
SCLK Output Pulse Width High	t_{slkh}	--	$2t_{clk}$	--	t_{clk}
SDATA Valid Before Rising SCLK	t_{ss}	$2t_{clk}$ - 100	--	--	ns
SDATA Valid After Rising SCLK	t_{sh}	$2t_{clk}$ - 100	--	--	ns
SDL Falling to 1st Rising SCLK	t_{rsclk}	--	$2t_{clk}$	--	ns
Last Rising SCLK to SDL Rising	t_{rsdl}	--	$2t^{clk}$	$2t_{clk}$ + 200	ns
HOLD Falling to 1st Falling SCLK	t_{hfs}	$6t_{clk}$	--	$8t_{clk}$ + 200	ns
CH1/2 Edge to 1st Falling SCLK	t_{chfs}	--	$7t_{clk}$	--	t_{clk}

1. Minimum CLKIN period is 0.625 µs is FRN mode (20 kHz sample rate).
2. External loading capacitors are required to allow the crystal to oscillate. Maximum crystal frequency is 1.6 MHz in FRN mode (20 kHz sample rate).
3. With a 2.0 MHz crystal, two 33 pF loading capacitors and a 10 MW parallel resistor.
4. Guaranteed by initial characterization (5102A die).
5. These times are for FRN mode.
6. These times are for PDT and RBT modes.

7. When $\overline{\text{HOLD}}$ goes low, the analog sample is captured immediately. To start conversion, $\overline{\text{HOLD}}$ must be latched by a falling edge of CLKIN. Conversion will begin on the next rising edge of CLKIN after $\overline{\text{HOLD}}$ is latched.
8. Only valid for $\overline{\text{TRK1}}$, $\overline{\text{TRK2}}$ falling when SCLK is low. If SCLK is high when $\overline{\text{TRK1}}$, $\overline{\text{TRK2}}$ falls, then SDATA is valid t_{dss} time after the next falling SCLK.

TABLE 5. 5102ALP DIGITAL CHARACTERISTICS

($T_A = T_{MIN}$ TO T_{MA}X; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Calibration Memory Retention Power Supply Voltage VA+ & VD+ [1]	V_{MR}	2.0	--	--	V
High-Level Input Voltage	V_{IH}	2.0	--	--	V
Low-Level Input Voltage	V_{IL}	--	--	0.8	V
High-Level Output Voltage [2]	V_{OH}	(VD+) -1.0	--	--	V
Low-Level Output Voltage - I_{OUT} = 1.6 mA	V_{OL}	--	--	0.4	V
Input Leakage Current	I_{IN}	--	--	10	µA
Digital Output Pin Capacitance	C_{OUT}	--	9	--	pF

1. VA- and VD- can be any value from zero to -5V for memory retention. Neither VA- or VD- should be allowed to go positive. AIN1, AIN2 or V_{REF} must not be greater than VA+ or VD+. This parameter is guaranteed by characterization.
2. I_{OUT} = -100 µA. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{OUT} = -40 µA.

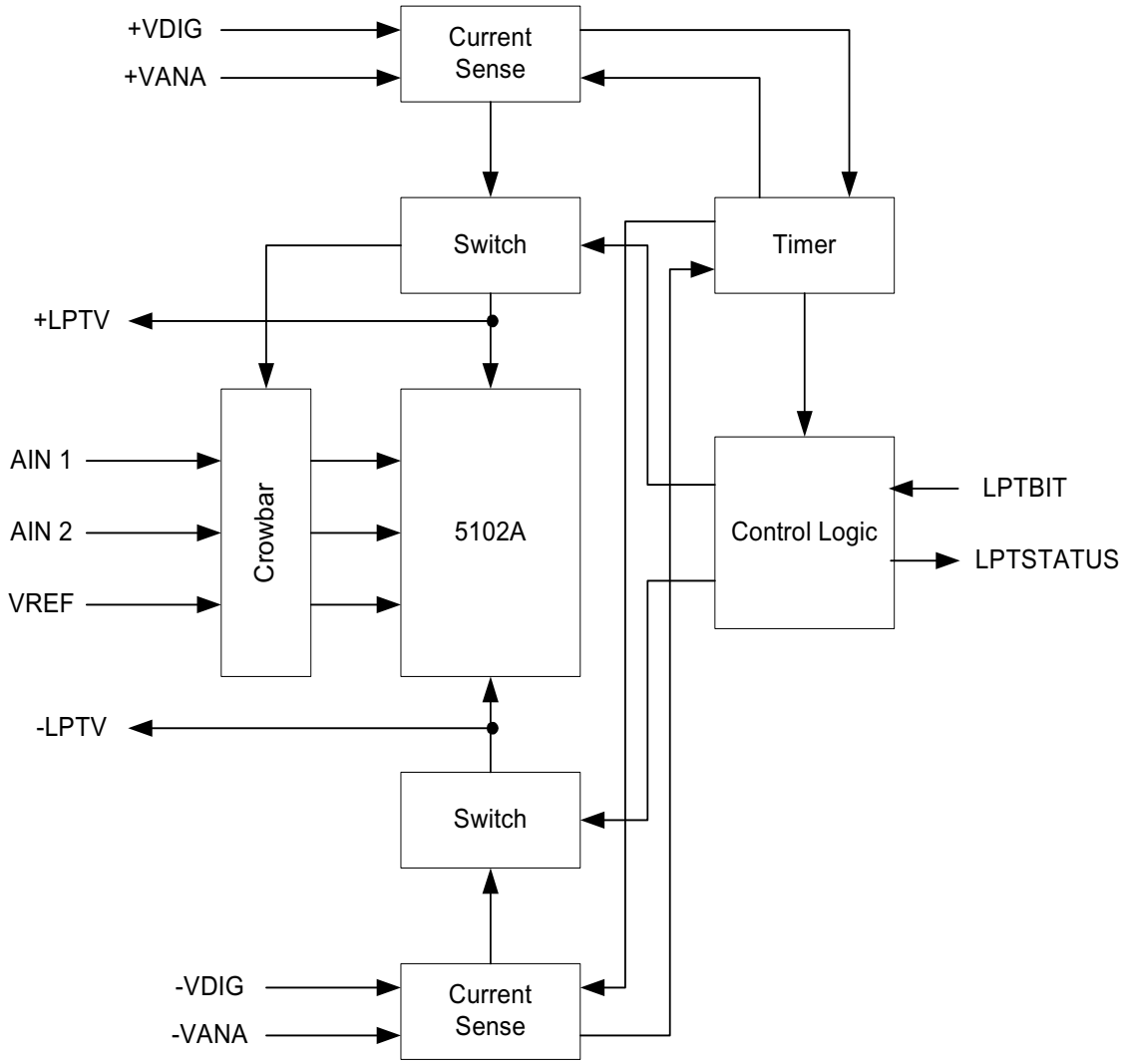
LPT™ OPERATION

Latchup Protection Technology (LPT™) automatically detects an increase in the supply current of the 5102ALP converter due to a single event effect and internally cycle the power to the converter off, then on, which restores the steady state operation of the device.

If data outputs are connected to a bus with other bus driver circuits, all external data bus drivers must be tri-stated and individual pull up resistors to the supply voltage (if used on the data bus) must no be less than 10 K ohm typical to assure proper single event effect recovery.

STATUS can also be used to generate an input to the system data processor indicating that an LPT™ cycle has occurred, and the protected device output accuracy may not be met until after the respective recovery time to the event. The STATUS signal is generated from an advanced CMOS logic gate output. This output may not exhibit a monotonic fall time and may even oscillate briefly while power is being restored to the protected device and the decoupling capacitance is charged. Loading on the STATUS output should be minimized because this signal is used internally by the 5102ALP. It is recommended that load current not exceed 2 mA and load capacitance be kept will below 1000 pF.

5102ALP LPT™ BLOCK DIAGRAM



LATCH-UP PROTECTION CIRCUIT (LPT) PIN DESCRIPTION

PIN	PIN NAME	FUNCTION
18	LPTBIT	The LPT circuit will crowbar the power supplies to the SEI5102ALPRP for as long as a logical high is applied. Used to verify operation of the LPT. Normally a logical low or ground is applied to this input.
26	-LPTV	Negative power supply. VA- and VD- are connected and can be measured on this pin. Normally -5V.
27	+LPTV	Positive power supply. VA+ and VD+ are connected and can be measured on this pin. Normally +5V.

Latch-up Protection Circuit (LPT) Pin Description

Pin	Pin Name	Function
39	LPT-STA-TUS	A 0 to 5V square-wave will output during a latch condition. Normally low.

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Figure 1. Reset and Calibration Timing

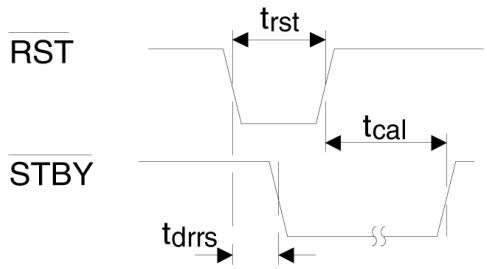
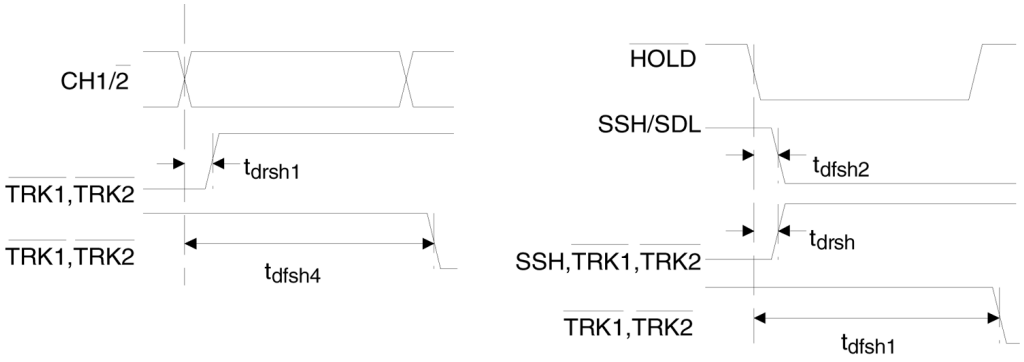


Figure 2. Control Output Timing



a. FRN Mode

b. PDT, RBT Mode

Figure 3. Channel Selection Timing

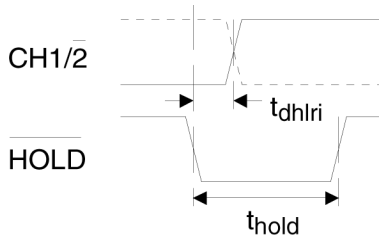


FIGURE 4. START CONVERSION TIMING

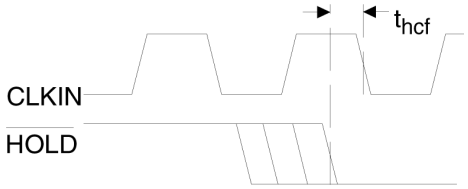
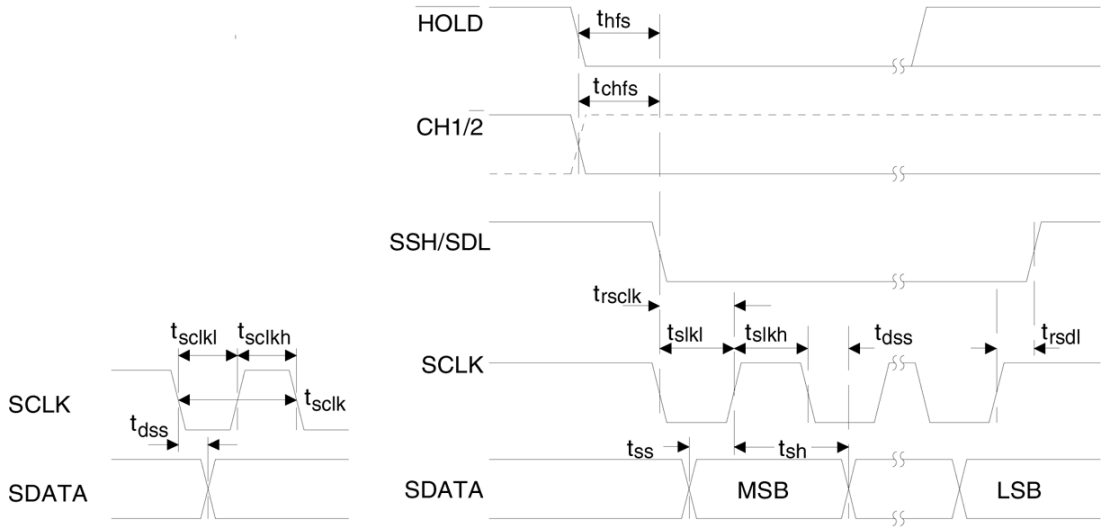


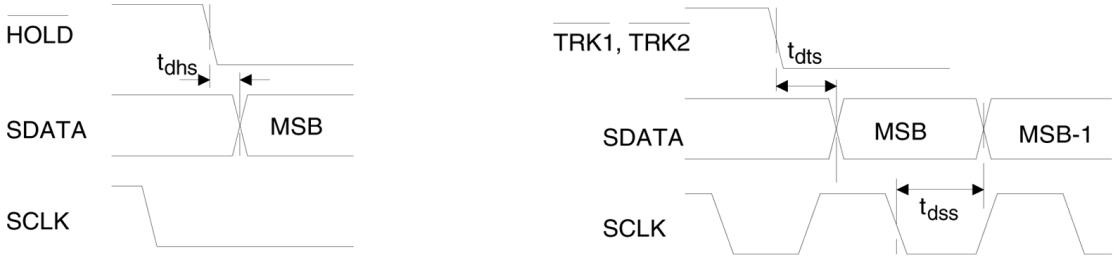
FIGURE 5. SERIAL DATA TIMING



a. SCLK input (RBT and PDT mode)

b. SCLK output (SSC and FRN modes)

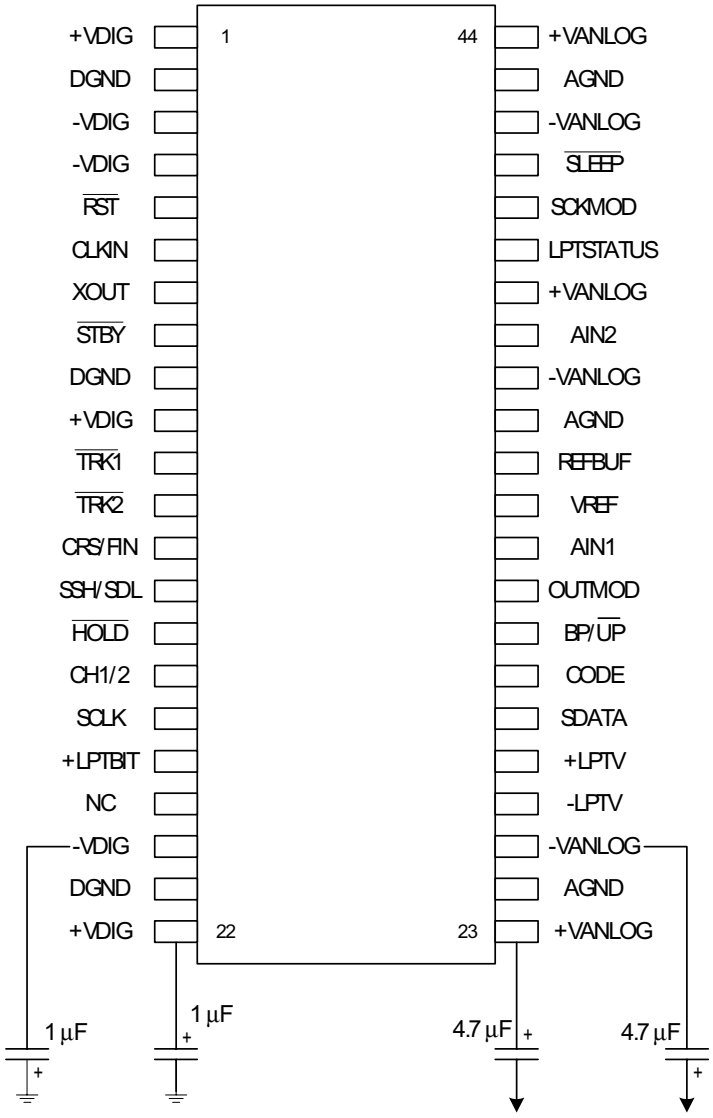
FIGURE 6. DATA TRANSMISSION TIMING



a. Pipelined Data Transmission (PDT)

b. Register Burst Transmission (RBT) Mode

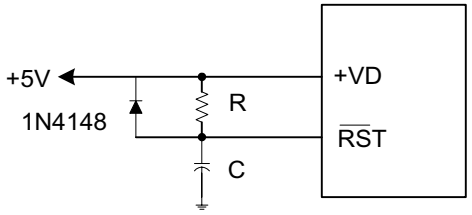
FIGURE 7. BYPASS CIRCUIT

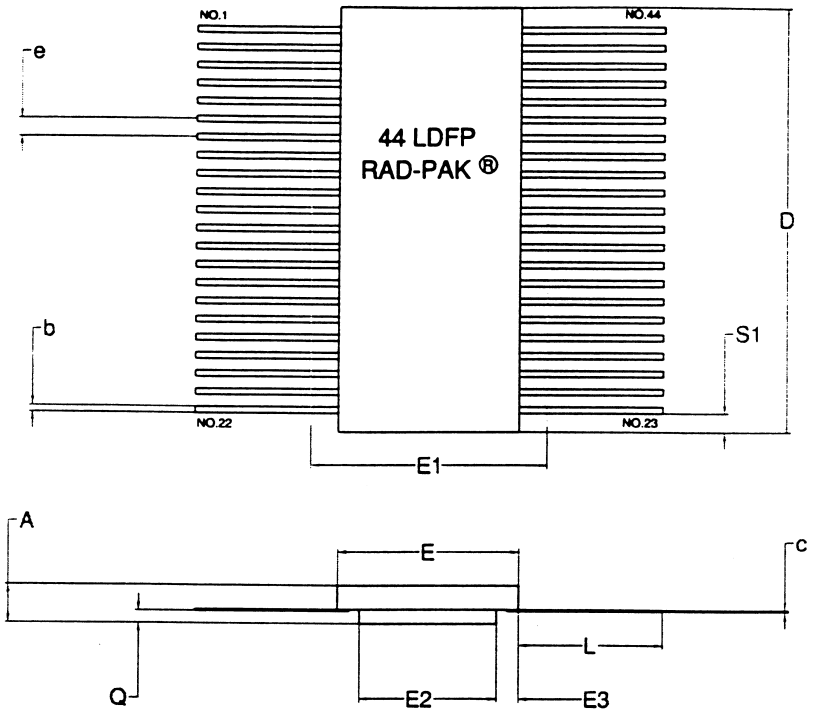


Note:

1. Cap must be connected to the device for proper operation. 4.7 µF analog side. 1 µF digital side.
2. Unused logic inputs should be tied to +VD or DGND.

FIGURE 8. POWER-UP RESET CIRCUIT





44 PIN FRP

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.256	0.282	0.308
b	0.014	0.017	0.020
c	0.009	0.010	0.012
D	1.089	1.100	1.111
E	0.564	0.570	0.576
E1	--	--	0.600
E2	0.410	0.430	0.450
E3	0.044	0.070	--
e	0.050 BSC		
L	0.455	0.465	0.475
Q	0.022	0.027	0.032
S1	0.005	--	--
N	44		

F44
Note: All dimensions in inches

Important Notice:

These data sheets are created using the chip manufacturers published specifications. MAxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Maxwell Technologies assumes no responsibility for the use of this information.

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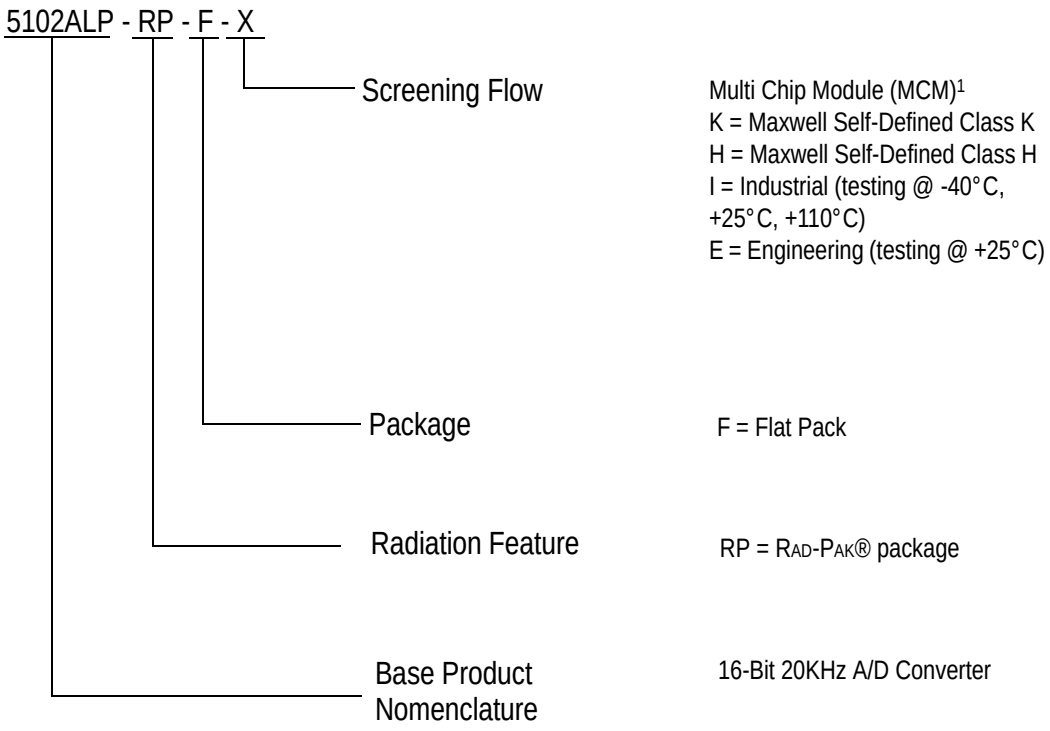
Product Ordering Options

Model Number



1) Products are manufactured and screened to Maxwell Technologies self-defined Class H and Class K flows.