## CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer


#### Abstract

General Description The MAX2310/MAX2312/MAX2314/MAX2316 are IF receivers designed for dual-band, dual-mode, and sin-gle-mode N-CDMA and W-CDMA cellular phone systems. The signal path consists of a variable gain amplifier (VGA) and I/Q demodulator. The devices feature guaranteed +2.7 V operation, a dynamic range of over 110dB, and high input IP3 (-33dBm at 35dB gain, 1.7 dBm at -35 dB ).

Unlike similar devices, the MAX2310 family of receivers includes dual oscillators and synthesizers to form a self-contained IF subsystem. The synthesizer's reference and RF dividers are fully programmable through a 3-wire serial bus, enabling dual-band system architectures using any common reference and IF frequency. The differential baseband outputs have enough bandwidth to suit both N-CDMA and W-CDMA systems, and offer saturated output levels of $2.7 \mathrm{Vp}-\mathrm{p}$ at a low +2.75 V supply voltage. Including the low-noise voltage-controlled oscillator (VCO) and synthesizer, the MAX2310 draws only 26 mA from a +2.75 V supply in CDMA (differential IF) mode. The MAX2310/MAX2312/MAX2314/MAX2316 are available in 28-pin QSOP packages.


> Applications
> Single/Dual/Triple-Mode CDMA Handsets
> Globalstar Dual-Mode Handsets
> Wireless Data Links
> Tetra Direct-Conversion Receivers
> Wireless Local Loop (WLL)
Complete IF Subsystem Includes VCO and
Synthesizer
Supports Dual-Band, Triple-Mode Operation
VGA with >110dB Gain Control
Quadrature Demodulator
High Output Level (2.7V)
Programmable Charge-Pump Current
300MHz
3-Wire Programmable Interface
Low Supply Voltage (+2.7V)

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
| :--- | :--- | :--- |
| MAX2310EEI | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 28 QSOP |
| MAX2312EEI | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 28 QSOP |
| MAX2314EEI | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 28 QSOP |
| MAX2316EEl | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 28 QSOP |

Pin Configurations appear at end of data sheet. Block Diagram appears at end of data sheet.

Selector Guide

| PART | MODE | DESCRIPTION | INPUT RANGE |
| :---: | :---: | :---: | :---: |
| MAX2310 | AMPS, <br> Cellular CDMA, <br> PCS CDMA | Dual Band, Triple Mode | 40 MHz to 300 MHz |
| MAX2312 | PCS CDMA | Single Band, Single Mode | 67 MHz to 300 MHz |
| MAX2314 | AMPS, <br> Cellular CDMA | Single Band, Dual Mode | 40 MHz to 150 MHz |
| MAX2316 | Cellular CDMA | Single Band, Single Mode or <br> Single Band, Dual Mode with <br> External Discriminator | 40 MHz to 150 MHz |

## CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

## ABSOLUTE MAXIMUM RATINGS

VCC to GND. SHDN to GND STBY, BUFEN, MODE, EN, DATA,
CLK, DIVSEL $\qquad$
 -0.3 V , the lesser of +4.2 V or $(\mathrm{VCC}+0.3 \mathrm{~V})$ AC Signals TankH $\pm$, TankL $\pm$,
$R E F, F M \pm, C D M A \pm$ $\qquad$ .1.0V peak

Digital Input Current $\overline{\text { SHDN }}$, MODE, DIVSEL,
 Continuous Power Dissipation ( $\mathrm{T}_{\mathrm{A}}=+70^{\circ} \mathrm{C}$ )
28-pin QSOP (derate $10 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ above $\mathrm{T}_{\mathrm{A}}=+70^{\circ} \mathrm{C}$ ) $\ldots . .800 \mathrm{~mW}$ Operating Temperature Range ........................... $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ Junction Temperature. $+150^{\circ} \mathrm{C}$
Storage Temperature Range ............................... $65^{\circ} \mathrm{C}$ to $+160^{\circ} \mathrm{C}$
Lead Temperature (soldering, 10s). $\qquad$
$+300^{\circ} \mathrm{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

$\left(\mathrm{VCC}=+2.7 \mathrm{~V}\right.$ to $+5.5 \mathrm{~V}, \mathrm{MODE}=\mathrm{DIVSEL}=\overline{\mathrm{SHDN}}=\overline{\mathrm{STBY}}=\overline{\mathrm{BUFEN}}=$ high, differential output load $=10 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$, registers set to default power-up settings. Typical values are at $\mathrm{V}_{\mathrm{CC}}=+2.75 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS |  | MIN | TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Supply Current (Note 1) | ICC | CDMA mode | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | 25.9 | 37.5 | mA |
|  |  |  | $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |  |  | 41.5 |  |
|  |  | FM IQ mode | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | 25.4 | 36.7 |  |
|  |  |  | $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |  |  | 40.6 |  |
|  |  | FM I mode | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | 24.7 | 35.7 |  |
|  |  |  | $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |  |  | 39.5 |  |
|  |  | STANDBY (VCO_H) | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | 12.3 | 18.8 |  |
|  |  |  | $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |  |  | 20.7 |  |
|  |  | STANDBY (VCO_L) | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | 11.5 | 18.4 |  |
|  |  |  | $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |  |  | 20.3 |  |
|  |  | Addition for LO out ( $\overline{\mathrm{BUFEN}}=$ low) |  | 3.5 |  |  |  |
| Shutdown Current | ICC | $\overline{\text { SHDN }}=$ low |  |  | 1.5 | 10 | $\mu \mathrm{A}$ |
| Register Shutdown Current | ICC |  |  |  | 3 | 5.8 | mA |
| Logic High |  |  |  | 2.0 |  |  | V |
| Logic Low |  |  |  |  |  | 0.5 | V |
| Logic High Input Current | $\mathrm{IIH}^{\text {H }}$ |  |  | 2 |  |  | $\mu \mathrm{A}$ |
| Logic Low Input Current | IIL |  |  |  |  | 2 | $\mu \mathrm{A}$ |
| VGC Control Input Current |  | $0.5 \mathrm{~V}<\mathrm{VVGC}<2.3 \mathrm{~V}$ |  | -5 |  | 5 | $\mu \mathrm{A}$ |
| VGC Control Input Current During Shutdown |  | $\overline{\text { SHDN }}=$ low |  |  |  | 1 | $\mu \mathrm{A}$ |
| Lock Indicator High (locked) |  | $50 \mathrm{k} \Omega$ load |  | 2.0 |  |  | V |
| Lock Indicator Low (unlocked) |  | $50 \mathrm{k} \Omega$ load |  |  |  | 0.5 | V |
| DC Offset Voltage |  | I+ to I- and Q+ to Q-, PLL locked |  | -20 | $\pm 1.5$ | +20 | mV |
| Common-Mode Output Voltage |  | $\mathrm{V}_{\mathrm{CC}}=2.75 \mathrm{~V}$ |  | VCC - 1.4 |  |  | V |

## CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

## AC ELECTRICAL CHARACTERISTICS

(MAX2310/MAX2314 or MAX2312/MAX2316 EV kit, $\mathrm{V}_{\mathrm{CC}}=+2.75 \mathrm{~V}$, registers set to default power-up states, $\mathrm{f}_{\mathrm{I}} \mathrm{N}=210.88 \mathrm{MHz}$ for CDMA, $f / \mathrm{N}=85.88 \mathrm{MHz}$ for $\mathrm{FM}, \mathrm{fREF}=19.68 \mathrm{MHz}$, synthesizer locked with passive 2 nd-order lead-lag loop filter, $\overline{\mathrm{SHDN}}=$ high, VGC set for +35 dB voltage gain, differential output load $=10 \mathrm{k} \Omega$, all power levels referred to $50 \Omega, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Input Frequency | fin | (Note 2) | 40 |  | 300 | MHz |
| Reference Frequency | freF | (Note 2) |  |  | 39 | MHz |
| Frequency Reference Signal Level | VREF |  | 0.2 |  |  | Vp-p |

SIGNAL PATH, CDMA MODE

| Input Third-Order Intercept | IIP3 | Gain $=-35 \mathrm{~dB}$ (Note 3) |  |  | 1.7 |  | dBm |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Gain $=+35 \mathrm{~dB}$ (Note 4) |  |  | -33.2 |  |  |
| Input 1dB Compression | $\mathrm{P}_{1 \mathrm{~dB}}$ | Gain = - |  | -9 | -6.4 |  | dBm |
|  |  | Gain $=+35 \mathrm{~dB}$ |  | -44 | -38.3 |  |  |
| Input 0.25dB Desensitization |  | (Note 5) | Gain $=-35 \mathrm{~dB}$ |  | -14.8 |  | dBm |
|  |  |  | Gain $=+35 \mathrm{~dB}$ |  | -49 |  |  |
| Minimum Voltage Gain | Av | $\mathrm{VGC}=0.5 \mathrm{~V}$ (Note 6) |  |  | -54.8 | -49 | dB |
| Maximum Voltage Gain | Av | $\mathrm{V}_{\mathrm{GC}}=2.3 \mathrm{~V}$ (Note 6) |  | 56 | 61.3 |  | dB |
| DSB Noise Figure | NF | Gain $=-35 \mathrm{~dB}$ |  |  | 62.9 |  | dB |
|  |  | Gain $=+35 \mathrm{~dB}$ |  |  | 6.36 |  |  |

SIGNAL PATH, FM_IQ MODE

| Input Third-Order Intercept | IIP3 | (Note 7) | Gain $=-35 \mathrm{~dB}$ | -6.0 |  |  | dBm |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Gain $=+35 \mathrm{~dB}$ |  | -31 |  |  |
| Input 1dB Compression | P1dB | (Notes 6, 8) | Gain $=-35 \mathrm{~dB}$ | -20 | -16.2 |  | dBm |
|  |  |  | Gain $=+35 \mathrm{~dB}$ | -44 | -38.4 |  |  |
| Minimum Voltage Gain | Av | VGC $=0.5 \mathrm{~V}$ (Note 6) |  |  | -50.2 | -47.4 | dB |
| Maximum Voltage Gain | Av | $\mathrm{V}_{\mathrm{GC}}=2.3 \mathrm{~V}$ ( Note 6) |  | 58.5 | 63.4 |  | dB |

SIGNAL PATH, CDMA and FM_IQ MODE

| Maximum Gain Variation Over Temperature |  | Normalized to $+25^{\circ} \mathrm{C}$ |  | $\pm 2.5$ | dB |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Baseband 0.5dB Bandwidth |  |  |  | 4.2 | MHz |
| Quadrature Suppression |  | $\mathrm{T}_{\text {A }}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$ (Note 6) | +28 | +35 | dB |
| LO to Baseband Leakage |  |  |  | 1 | mVp-p |
| Saturated Output Level | VSAT | Differential |  | 2.7 | Vp-p |
| PHASE-LOCKED LOOP |  |  |  |  |  |
| VCO Tune Range | fvCO_L | (Note 2) | 80 |  | MHz |
|  | fvCO_H |  | 135 |  |  |
| LOOUT Output Power | PLO | RL $=50 \Omega, \overline{\mathrm{BUFEN}}=$ low |  | -13.7 | dBm |

## CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

## AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2310/MAX2314 or MAX2312/MAX2316 EV kit, VCC $=+2.75 \mathrm{~V}$, registers set to default power-up states, $\mathrm{f} / \mathrm{N}=210.88 \mathrm{MHz}$ for CDMA, $\mathrm{f} \mathrm{IN}=85.88 \mathrm{MHz}$ for FM , $\mathrm{fREF}=19.68 \mathrm{MHz}$, synthesizer locked with passive 2 nd-order lead-lag loop filter, $\overline{\mathrm{SHDN}}=$ high, VGC set for +35 dB voltage gain, differential output load $=10 \mathrm{k} \Omega$, all power levels referred to $50 \Omega, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| VCO Minimum Divide Ratio | M1, M2 |  |  |  | 256 |  |
| VCO Maximum Divide Ratio | M1, M2 |  | 16383 |  |  |  |
| REF Minimum Divide Ratio | R1, R2 |  |  |  | 2 |  |
| REF Maximum Divide Ratio | R1, R2 |  | 2047 |  |  |  |
| Minimum Phase Detector Comparison Frequency |  | (Note 6) |  |  | 20 | kHz |
| Maximum Phase Detector Comparison Frequency |  | (Note 6) | 1500 |  |  | kHz |
| Base Band Spurious due to PLL |  |  |  |  | -50 | dBc |
| LOOUT at 85 MHz , VCO_L Enabled (Note 9) |  | 1 kHz offset |  | -72 |  | $\mathrm{dBc} / \mathrm{Hz}$ |
|  |  | 12.5 kHz offset |  | -100 |  |  |
|  |  | 30kHz offset |  | -110 |  |  |
|  |  | 120kHz offset |  | -119 |  |  |
|  |  | 900kHz offset |  | -125 |  |  |
| LOOUT at 210 MHz , VCO_H Enabled (Note 9) |  | 1 kHz offset |  | -64 |  | $\mathrm{dBc} / \mathrm{Hz}$ |
|  |  | 12.5 kHz offset |  | -91 |  |  |
|  |  | 30 kHz offset |  | -105 |  |  |
|  |  | 120kHz offset |  | -115 |  |  |
|  |  | 900 kHz offset |  | -125 |  |  |
| Charge-Pump Source/Sink Current |  | Acquisition, CPX = XX, TC = 1 (Note 10) | 1480 | 2100 | 2650 | $\mu \mathrm{A}$ |
|  |  | Locked, CPX = 00 | 105 | 150 | 190 |  |
|  |  | Locked, CPX = 01 | 150 | 210 | 265 |  |
|  |  | Locked, CPX = 10 | 210 | 300 | 380 |  |
|  |  | Locked, CPX = 11 | 300 | 425 | 530 |  |
| Charge-Pump Source/Sink Matching |  | Locked, all values of CPX, $0.5 \mathrm{~V}<\mathrm{V}_{C P}<\mathrm{V}_{C C}-0.5 \mathrm{~V}$ |  | 0.2 | 10 | \% |

Note 1: FM_IQ and FM_I modes are not available on MAX2312 and MAX2316.
Note 2: Recommended operating frequency range.
Note 3: $f_{1}=210.88 \mathrm{MHz}, f_{2}=210.89 \mathrm{MHz}, \mathrm{P}_{\mathrm{f} 1}=\mathrm{P}_{\mathrm{f} 2}=-15 \mathrm{dBm}$.
Note 4: $f_{1}=210.88 \mathrm{MHz}, f_{2}=210.89 \mathrm{MHz}, \mathrm{P}_{\mathrm{f} 1}=\mathrm{P} \mathrm{f} 2=-50 \mathrm{dBm}$.
Note 5: Small-signal gain at 200kHz below the LO frequency will be reduced by less than 0.25 dB when an interfering signal at 1.25 MHz below the LO frequency is applied at the specified level.

Note 6: Guaranteed by design and characterization.
Note 7: $\mathrm{f}_{1}=85.88 \mathrm{MHz}, \mathrm{f}_{2}=85.98 \mathrm{MHz}, \mathrm{P}_{\mathrm{f} 1}=\mathrm{P} \mathrm{f} 2=-15 \mathrm{dBm}$.
Note 8: $f_{1}=85.88 \mathrm{MHz}, \mathrm{f}_{2}=85.98 \mathrm{MHz}, \mathrm{P} 1 \mathrm{f}=\mathrm{P} 2=-50 \mathrm{dBm}$.
Note 9: Measured at LOOUT with BD $=0(\div 2$ selected $)$.
Note 10: Not available on MAX2316.

# CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer 

## Typical Operating Characteristics

(MAX2310/MAX2314 or MAX2312/MAX2316 EV kit, $\mathrm{V}_{\mathrm{CC}}=+2.75 \mathrm{~V}$, registers set to default power-up states, $\mathrm{f} / \mathrm{N}=210.88 \mathrm{MHz}$ for CDMA, $\mathrm{f} / \mathrm{N}=85.88 \mathrm{MHz}$ for FM , $\mathrm{fREF}=19.68 \mathrm{MHz}$, synthesizer locked with passive 2 nd-order lead-lag loop filter, $\overline{\mathrm{SHDN}}=$ high, VGC set for +35 dB voltage gain, differential output load $=10 \mathrm{k} \Omega$, all power levels referred to $50 \Omega, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise noted.)


GAIN vs. INPUT FREQUENCY


NOISE FIGURE vs. GAIN


RECEIVE SHUTDOWN CURRENT vs.
SUPPLY VOLTAGE


GAIN vs. BASEBAND FREQUENCY


NOISE FIGURE vs. TEMPERATURE


GAIN vs. VGC


THIRD-ORDER INPUT INTERCEPT vs. GAIN


VCO VOLTAGE vs. TIME


## CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

(MAX2310/MAX2314 or MAX2312/MAX2316 EV kit, $\mathrm{V}_{C C}=+2.75 \mathrm{~V}$, registers set to default power-up states, $\mathrm{f}_{\mathrm{IN}}=210.88 \mathrm{MHz}$ for CDMA, $\mathrm{fIN}=85.88 \mathrm{MHz}$ for FM , $\mathrm{fREF}=19.68 \mathrm{MHz}$, synthesizer locked with passive 2 nd-order lead-lag loop filter, $\overline{\mathrm{SHDN}}=$ high, VGC set for +35 dB voltage gain, differential output load $=10 \mathrm{k} \Omega$, all power levels referred to $50 \Omega, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise noted.)


TANKL PORT
1/S11 vs. FREQUENCY


TANKH PORT
1/S11 vs. FREQUENCY


LOOUT PORT
S22 vs. FREQUENCY



Pin Description

| PIN |  |  |  | NAME | FUNCTION |
| :---: | :---: | :---: | :---: | :---: | :---: |
| MAX2310 | MAX2312 | MAX2314 | MAX2316 |  |  |
| 1 | 1 | 1, 8 | 1 | BYP | Bypass Node. Must be capacitively decoupled (bypassed) to analog ground. |
| 2 | 2 | 2 | 2 | CP_OUT | Charge-Pump Output |
| 3 | 3 | 3 | 3 | GND | Analog Ground Reference |
| 4,5 | - | 4, 5 | 5,6 | TANKL+, TANKL- | Differential Tank Input for Low-Frequency Oscillator |
| - | 4 | - | 4 | DIVSEL | High selects M1/R1; low selects M2/R2. |

# CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer 

Pin Description (continued)

| PIN |  |  |  | NAME | FUNCTION |
| :---: | :---: | :---: | :---: | :---: | :---: |
| MAX2310 | MAX2312 | MAX2314 | MAX2316 |  |  |
| 6, 7 | 5,6 | - | - | TANKH+, TANKH- | Differential Tank Input for High-Frequency Oscillator |
| - | 7 | - | 7 | BUFEN | LO Buffer Amplifier-active low |
| - | - | 6, 7 | - | N.C. | No Connection. Must be left open-circuit. |
| 8 | - | - | - | MODE | Mode Select. High selects CDMA mode; low selects FM mode. |
| - | 8 | - | 8 | LOOUT | Internal VCO Output. Depending on setting of BD bit, LOOUT is either the VCO frequency (twice the IF frequency) or onehalf the VCO frequency (equal to the IF frequency). |
| 9 | 9 | 9 | 9 | $\mathrm{V}_{\mathrm{CC}}$ | +2.7V to +5.5V Supply for Digital Circuits |
| 10 | 10 | 10 | 10 | GND | Digital Ground |
| 11 | 11 | 11 | 11 | REF | Reference Frequency Input |
| 12 | 12 | 12 | 12 | $\overline{\text { SHDN }}$ | Shutdown Input-active low. Low powers down entire device, including registers and serial interface. |
| 13, 14 | 13, 14 | 13, 14 | 13, 14 | IOUT+, IOUT- | Differential In-Phase Baseband Output, or FM signal output FM_I mode is selected. |
| 15 | 15 | 15 | 15 | LOCK | Lock Output-open-collector pin. Logic high indicates phaselocked condition. |
| 16, 17 | 16, 17 | 16, 17 | 16, 17 | $\begin{aligned} & \text { QOUT-, } \\ & \text { QOUT+ } \end{aligned}$ | Differential Quadrature-Phase Baseband Output. Disabled if FM_I mode is selected. |
| 18 | 18 | 18 | 18 | CLK | Clock input of the 3-wire serial bus |
| 19 | 19 | 19 | 19 | $\overline{\mathrm{EN}}$ | Enable Input. When low, input shift register is enabled. |
| 20 | 20 | 20 | 20 | DATA | Data input of the 3-wire serial bus. |
| 21 | 21 | 21 | 21 | $\mathrm{V}_{\mathrm{CC}}$ | 2.7V to 5.5V Supply for Analog Circuits |
| 22 | 22 | 22 | 22 | VGC | VGA Gain Control Input. Control voltage range is 0.5 V to 2.3 V . |
| 23, 24 | 23, 24 | 23, 24 | 23, 24 | CDMA-, CDMA+ | Differential CDMA Input. Active in CDMA mode. |
| 25 | - | 25 | - | FM+ | Differential Positive Input. Active in FM mode. |
| - | 25 | - | 25 | N.C. | No Connection. |
| 26 | - | 26 | - | FM- | Differential Negative Input for FM signal. Bypass to GND for single-ended operation. |
| - | 26 | - | 26 | $\overline{\text { STBY }}$ | Standby Input-active low. Low powers down VGA and demodulator while keeping VCO, PLL, and serial bus on. |
| 27, 28 | 27, 28 | 27, 28 | 27, 28 | BYP | Bypass Node. Must be capacitively decoupled (bypassed) to analog $\mathrm{V}_{\mathrm{CC}}$. |

## CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer



Figure 1. MAX2310 Typical Operating Circuit

## Detailed Description

## MAX2310

The MAX2310 is intended for dual-band (PCS and cellular) and dual-mode code division multiple access (CDMA) and FM applications (Figure 1). The device includes an IF variable-gain amplifier, quadrature demodulator, dual VCOs, and dual-frequency synthesizers (Figure 7). Dual VCOs are provided for applications using different IF frequencies for each mode or band of operation. The analog FM output signal can be
configured for conversion to the I channel, or it may be converted in quadrature to both the I and Q channels. The MAX2310's operation modes are described in Table 1. These modes are set by programming the control register and setting logic levels on control pins. If MODE is left floating, the internal register controls the operation. If driven high or low, mode will override certain register bits, as shown in Table 1.

# CDMA IF VGAs and I／Q Demodulators with VCO and Synthesizer 

Table 1．MAX2310 Control Register States


Note：$H=$ high，$L=$ low，$F=$ floating pin，$X=$ don＇t care，Blank $=$ independent parameter， $1=$ logic high， $0=$ logic low．


#### Abstract

MAX2312／MAX2316 The MAX2312／MAX2316 quadrature demodulators are simplified versions of the MAX2310 that can be used in single－mode CDMA or dual mode using an external FM discriminator（Figures 2a and 2b）．The MAX2312 VCO is optimized for the 67 MHz to 300 MHz IF frequency range，while the MAX2316 VCO is optimized for the 40 MHz to 150 MHz IF frequency range． Both devices include a buffered output for the VCO． The buffered VCO output can be used to support sys－ tems implementing traditional limiting IF stages for FM demodulation in dual－mode phones as well as for the transmit LO in TDD systems．This buffered output can


be configured for the VCO frequency（twice the IF fre－ quency）or one－half the VCO frequency（IF frequency）． The BUFEN pin enables this feature．A standby mode， in which only the VCO and synthesizer are operational， can be selected through the serial interface or the STBY pin．The MAX2312／MAX2316s＇operational modes are described in Table 2．These modes are set by pro－ gramming the control register and／or setting logic lev－ els on control pins．If the control pins（ $\overline{\text { STBY，}}$ BUFEN， DIVSEL）are left floating，the internal register controls the operational mode．If driven high or low，the control pins will override certain register bits，as shown in Table 2.

## CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer



Figure 2a. MAX2312 Typical Operating Circuit

## CDMA IF VGAs and I／Q Demodulators with VCO and Synthesizer



Figure 2b．MAX2316 Typical Operating Circuit
9 －عてXVW／t トعてXVW／乙 トعてXVW／O トعてXVW

## CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

Table 2. MAX2312/MAX2316 Control Register States


Note: H = high, L = low, 1 = logic high, $0=$ logic low, $X=$ don't care, blank = independent parameter.

## CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer



Figure 3. MAX2314 Typical Operating Circuit

MAX2314
The MAX2314 supports CDMA cellular-band, dualmode operation. As with the MAX2310, the FM mode can be configured for conversion to the I port or quadrature conversion to both the I and Q ports (Figure 3). The MAX2314's operational modes are described in Table 3. These modes are set by programming the control register and setting logic levels on control pins.

## Applications Information

Variable-Gain Amplifier and Demodulator
The MAX2310 family provides a Variable-Gain Amplifier (VGA) with exceptional gain range. The MAX2310/ MAX2314 support multimode applications with dual differential inputs, selectable with the IN_SEL (IS) control bit. On the MAX2310 this function can be controlled with the MODE pin, which overrides the IS control bit. The VGA's gain is controlled over a 110dB range with

## CDMA IF VGAs and I／Q Demodulators with VCO and Synthesizer

## Table 3．MAX2314 Control Register States

|  |  | P I N | $\begin{aligned} & \mathbf{M} \\ & \mathbf{S} \\ & \mathbf{B} \end{aligned}$ | CONTROL REGISTER L <br> S  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| OPERATIONAL MODE | ACTION RESULT | \|⿳亠口冋阝 |  | $\begin{aligned} & 1 \\ & \text { 1} \\ & \text { a } \end{aligned}$ | $\begin{aligned} & \underset{\sim}{Z} \\ & \underset{\sim}{w} \\ & \underset{\sim}{n} \end{aligned}$ |  | $\begin{aligned} & \text { 岗 } \\ & \stackrel{1}{0} \end{aligned}$ | $\begin{aligned} & \text { Q } \\ & \text { 0 } \\ & 0 \\ & 0 \\ & > \end{aligned}$ | $\begin{aligned} & \text { u} \\ & 0 \\ & 0 \\ & 0 \\ & \hline \end{aligned}$ | $\begin{aligned} & \text { خ } \\ & \frac{1}{\mathbf{n}} \end{aligned}$ | $\left\lvert\, \begin{array}{\|l\|l\|l\|l\|} \underset{\sim}{\underset{\sim}{u}} \\ \hline \end{array}\right.$ |  | $\begin{aligned} & \underset{\sim}{山} \\ & \mathbf{\omega}_{1} \end{aligned}$ | $\left\lvert\,\right.$ | 文 |
| SHUTDOWN | Shutdown pin completely shuts down chip | L | X | X | X | X | X | X | X | X | X | X | X | X | X |
| SHUTDOWN | 0 in shutdown register bit leaves seri－ al port active | H | X | X | X | X | X | X | X | X | X | X | X | X | L |
| STANDBY | 0 in standby pin turns off VGA and modulator only | H |  |  | 0 |  |  |  | 0 | X | X |  |  | 0 | 1 |
| CDMA | CDMA operation | H |  |  | 0 |  |  |  | 0 | X | X | X | 1 | 1 | 1 |
| FM＿IQ | FM IQ quadrature operation | H |  |  | 0 |  |  |  | 0 | X | X | 0 | 0 | 1 | 1 |
| FM＿I | FM I operation | H |  |  | 0 |  |  |  | 0 | X | X | 1 | 0 | 1 | 1 |

Note：$H=$ high，$L=$ low， 1 ＝logic high， $0=$ logic low，$X=$ don＇t care，blank＝independent parameter
the VGC pin．The output of the VGA drives the RF ports of a quadrature demodulator．The MAX2310／MAX2314 provide two types of FM demodulation，controlled by the FM＿TYPE（FT）control bit．When FM＿TYPE is＂1，＂ the signal is passed through both the I and Q signal paths for subsequent lowpass filtering and A／D conver－ sion at baseband．If FM＿TYPE is＂ 0, ，＂the FM signal is passed through the I mixer only．

## Voltage－Controlled Oscillator， Buffers，and Quadrature Generation

 The LO signal for downconversion is provided by a voltage－controlled oscillator（VCO）consisting of an on－ chip differential oscillator，and an off－chip high－Q reso－ nant network．Figure 4 shows a simplified schematic of the VCO oscillator．Multiband operation is supported by the MAX2310 with dual VCOs．VCO＿H and VCO＿L are selectable with the MODE pin or the VCO＿SEL（VS）control bit．They oscillate at twice the desired LO fre－ quency．For applications requiring an external LO，the VCOs can be bypassed with the VCO＿BYP（VB）control bit．
The MAX2312／MAX2316 buffer the output of the VCO and provide this signal at the LOOUT pin．This signal is enabled by the BUFEN（BE）control bit or by the BUFEN control pin．The frequency of this signal is selected by the BUF＿DIV（BD）control bit，and can be either the VCO frequency or half the VCO frequency．
Quadrature downconversion is realized by providing in－ phase（I）and quadrature－phase（Q）components of the LO signal to the LO ports of the demodulator described above．The quadrature LO signals are generated by dividing the VCO output frequency using two latches． The appropriate latch outputs provide I and Q signals at the desired LO frequency．

# CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer 


#### Abstract

Synthesizer The VCO's output frequency is controlled by an internal phase-locked-loop (PLL) dual-modulus synthesizer. The loop filter is off-chip to simplify loop design for emerging applications. The tunable resonant network is also off-chip for maximum $Q$ and for system design flexibility. The VCO output frequency is divided down to the desired comparison frequency with the M counter. The $M$ counter consists of a 4-bit A swallow counter and a 10-bit P counter. A reference signal is provided from an external source and is divided down to the comparison frequency with the R counter. The two divided signals are compared with a three-state digital phase-frequency detector. The phase-detector output drives a charge pump as well as lock-detect logic and turbocharge control logic. The charge pump output (CP_OUT) pin is processed by the loop filter and drives the tunable resonant network, altering the VCO frequency and closing the loop. Multimode applications are supported by two independent programmable registers each for the M counter (M1, M2), the R counter (R1, R2), and the charge-pump output current magnitude (CP1, CP2). The DIVSEL (DS) bit selects which set of registers is used. It can be overridden by the MAX2310's MODE pin or the MAX2312/ MAX2316's DIVSEL pin. Programming these registers is discussed in the 3-Wire Interface and Registers section.




Figure 4. Voltage-Controlled Oscillators

When the part initially powers up or changes state, the synthesizer acquisition time can be reduced by using the Turbo feature, enabled by the TURBOCHARGE (TC) control bit. Turbo functionality provides a larger charge-pump current during acquisition mode. Once the VCO frequency is acquired, the charge-pump output current magnitude automatically returns to the preprogrammed state to maintain loop stability and minimize spurs in the VCO output signal.
The lock detect output indicates when the PLL is locked with a logic high.

## 3-Wire Interface and Registers

The MAX2310 family incorporates a 3-wire interface for synthesizer programming and device configuration (Figure 5). The 3-wire interface consists of a clock, data, and ENABLE. It controls the VCO dividers (M1 and M 2 ), reference frequency dividers (R1 and R2), and a 13-bit control register. The control register is used to set up the operational modes (Table 4). The input shift is 17 data bits long and requires a total of 18 clock bits (Figure 6). A single clock pulse is required before enable drops low to initialize the data bus.
Whenever the $M$ or $R$ divide register value is programmed and downloaded, the control register must also be subsequently updated. This prevents turbolock from going active when not desired.
The $\overline{\text { SHDN }}$ control bit is notable because it differs from the $\overline{\text { SHDN }}$ pin. When the SHDN control bit is low, the registers and serial interface are left active, retaining the values stored in the latches, while the rest of the device is shut off. In contrast, the $\overline{\text { SHDN }}$ pin, when low, shuts down everything, including the registers and serial interface. See the functional diagram in Figure 7.

Registers
Figure 8 shows the programming logic. The 17-bit shift register is programmed by clocking in data at the rising edge of CLK. Before the shift register is able to accept data, it must be initialized by driving it with at least one full clock cycle at the CLK input with $\overline{\mathrm{EN}}$ high (see Figure 6). Pulling enable low will allow data to be clocked into the shift register; pulling enable high loads the register addressed by A0, A1, and A2, respectively (Figure 8). Table 5 lists the power-on default values of all registers. Table 6 lists the charge-pump current, depending on CPO and CP1.

## CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

MAX2310/MAX2312/MAX2314/MAX2316


Figure 5. 3-Wire Control Block Diagram


Figure 6. 3-Wire Interface Timing Diagram

# CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer 



Figure 7. Functional Diagram

## CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

Table 4. Control Register, Default State: 0B57h, Address: 110b

| BIT ID | BIT NAME | POWERUP STATE | $\begin{gathered} \text { BIT } \\ \text { LOCATION } \\ 0=\text { LSB } \end{gathered}$ | FUNCTION |
| :---: | :---: | :---: | :---: | :---: |
| TM | TEST_MODE | 0 | 12 | Must be 0 for normal operation. |
| POL | CP_POL | 1 | 11 | Logic "1" causes the charge-pump output CP_OUT to source current when fref/R > fvco/M. This state is used when the VCO tune polarity is such that increasing voltage produces increasing frequency. Logic "0" causes CP_OUT to source current when fvco/M $>f_{\text {REF }} / R$. This state is used when increasing tune voltage causes the VCO frequency to decrease. |
| TE | TEST_ENABLE | 0 | 10 | Must be 0 for normal operation. |
| TC | TURBO_CHARGE | 1 | 9 | Logic "1" activates turbocharge mode, which provides rapid frequency acquisition in the PLL. Not available on MAX2316. |
| DS | DIV_SEL | 1 | 8 | Logic "1" selects M1/R1 divide ratios. Logic "0" selects M2/R2. |
| VB | VCO_BYP | 0 | 7 | Logic "1" bypasses the VCO inputs for external VCO operation. |
| VS | VCO_SEL | 1 | 6 | Logic "1" selects VCO_H. Logic "0" selects VCO_L. |
| BD | BUF_DIV | 0 | 5 | Logic "1" selects divide-by-2 on LOOUT port. Logic "0" bypasses divider. |
| BE | BUFEN | 1 | 4 | Logic "1" disables LOOUT. Logic "0" enables LOOUT. |
| FT | FM_TYPE | 0 | 3 | Active in FM mode. Logic " 0 " selects quadrature demodulator for FM mode. Logic "1" selects downconversion to I port. |
| IS | IN_SEL | 1 | 2 | Logic "0" selects FM input port. Logic "1" selects CDMA input. |
| SB | $\overline{\text { STBY }}$ | 1 | 1 | Logic "0" enables standby mode, which shuts down the VGA and demodulator stages, leaving the VCO locked and the registers active. |
| SD | $\overline{\text { SHDN }}$ | 1 | 0 | Logic "0" enables register-based shutdown. This mode shuts down everything except the $M$ and $R$ latches and the serial bus. |

## Table 5. Register Defaults

| REGISTER | DEFAULT |
| :---: | :---: |
| M1 | 10519DEC |
| M2 | 4269DEC |
| R1 | 492DEC |
| R2 | 492DEC |
| CTRL | OB57HEX |
| CP0 | 11 BIN |
| CP1 | 11 BIN |

Table 6. Charge-Pump Control Bits

| $\mathbf{C P 1}$ | CPO | CHARGE-PUMP CURRENT <br> AFTER ACQUISITION <br> $(\boldsymbol{\mu} \mathbf{A})$ |
| :---: | :---: | :---: |
| 0 | 0 | 150 |
| 0 | 1 | 210 |
| 1 | 0 | 300 |
| 1 | 1 | 425 |

## CDMA IF VGAs and I／Q Demodulators with VCO and Synthesizer



Figure 8．Programming Logic

## CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

MAX2310/MAX2312/MAX2314/MAX2316

TOP VIEW




# CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer 

## Chip Information

TRANSISTOR COUNT: 6422


## CDMA IF VGAs and I/Q Demodulators with VCO and Synthesizer

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)


## Revision History

Pages changed at Rev 2: 1, 4, 18, 22

