## Low Power and Low Cost RTC with Alarm Function and Dual IRQ pins

The ISL12057 device is a low power real time clock that is pin compatible and functionally equivalent to Maxim DS1337 with clock/calendar and alarm function.

The oscillator uses an external, low-cost 32.768 kHz crystal. The real time clock tracks time with separate registers for hours, minutes, and seconds. The device has calendar registers for date, month, year and day of the week. The calendar is accurate through 2099, with automatic leap year correction.

## Pinouts

ISL12057
(8 LD SOIC, MSOP)
TOP VIEW


ISL12057
( 8 LD $\mu$ TDFN)
TOP VIEW


## Features

- Pin Compatible to Maxim DS1337
- Functionally Equivalent to Maxim DS1337
- Real Time Clock/Calendar
- Tracks Time in Hours, Minutes, and Seconds
- Day of the Week, Date, Month, and Year
- Dual Interrupts for Frequency Output and Alarm interrupts
- 4 Selectable Frequency Outputs
- 2 Alarms
- Settable to the Second, Minute, Hour, Day of the Week, and Date
- $\mathrm{I}^{2} \mathrm{C}$ Interface
- 400kHz Data Transfer Rate
- Small Package Options
- 8 Ld $2 m m \times 2 m m \mu$ TDFN
- 8 Ld MSOP
- 8 Ld SOIC
- Pb-Free (RoHS Compliant)


## Applications

- Utility Meters
- HVAC Equipment
- Audio/Video Components
- Set-Top Box/Television
- Modems
- Network Routers, Hubs, Switches, Bridges
- Cellular Infrastructure Equipment
- Fixed Broadband Wireless Equipment
- Pagers/PDA
- Point Of Sale Equipment
- Test Meters/Fixtures
- Office Automation (Copiers, Fax)
- Home Appliances
- Computer Products
- Other Industrial/Medical/Automotive


## Ordering Information

| PART <br> NUMBER | PART <br> MARKING | VDD RANGE <br> (V) | TEMP. RANGE <br> $\left({ }^{\circ} \mathrm{C}\right)$ | PKG. <br> DWG. \# |  |
| :--- | :--- | :--- | :--- | :--- | :--- |
| ISL12057IBZ (Note 1) | 12057 IBZ | 1.4 to 3.6 | -40 to +85 | 8 Ld SOIC |  |
| ISL12057IBZ-T* (Note 1) | 12057 IBZ | 1.4 to 3.6 | -40 to +85 | 8 Ld SOIC (Tape and Reel) |  |
| ISL12057IUZ (Note 1) | 12057 | 1.4 to 3.6 | -40 to +85 | M8.15 Ld MSOP |  |
| ISL12057IUZ-T* (Note 1) | 12057 | 1.4 to 3.6 | -40 to +85 | 8 Ld MSOP (Tape and Reel) | M8.118 |
| ISL12057IRUZ-T* (Note 2) | 057 | 1.4 to 3.6 | -40 to +85 | 8 Ld $\mu$ TDFN (Tape and Reel) | L8.2x2 |

*Please refer to TB347 for details on reel specifications.
NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and $100 \%$ matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb -free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb -free soldering operations. Intersil Pb -free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Block Diagram



Pin Descriptions

| PIN NUMBER | SYMBOL | DESCRIPTION |
| :---: | :---: | :---: |
| 1 | X1 | The X 1 pin is the input of an inverting amplifier and is intended to be connected to one pin of an external 32.768 kHz quartz crystal. This pin can also be driven by an external 32.768 kHz oscillator with X 2 pin floating. |
| 2 | X2 | The X 2 pin is the output of an inverting amplifier and is intended to be connected to one pin of an external 32.768 kHz quartz crystal. |
| 3 | $\overline{\mathrm{IRQ2}}$ | Interrupt Output 2 is a multi-functional pin that can be used as alarm interrupt. This pin is open drain and requires an external pull-up resistor. This pin is at high impedance at power up. |
| 4 | GND | Ground |
| 5 | SDA | Serial Data (SDA) is a bidirectional pin used to transfer serial data into and out of the device. It has an open drain output and may be wire OR'ed with other open drain or open collector outputs. |
| 6 | SCL | The Serial Clock (SCL) input is used to clock all serial data into and out of the device. |
| 7 | $\overline{\mathrm{IRQ1}} / \mathrm{F}_{\text {OUT }}$ | Interrupt Output 1/Frequency Output is a multi-functional pin that can be used as alarm interrupt or frequency output pin. The function is set via the configuration register. This pin is open drain and requires an external pull-up resistor. It has a default output of 32.768 kHz at power up. |
| 8 | $\mathrm{V}_{\mathrm{DD}}$ | Power supply |


| Absolute Maximum Ratings |  |
| :---: | :---: |
| Voltage on $\mathrm{V}_{\mathrm{DD}}$ (respect to GND) | -0.2V to 4V |
| Voltage on $\overline{\mathrm{IRQ1}} / \mathrm{F}_{\text {OUT }}, \overline{\mathrm{IRQ} 2}, \mathrm{SCL}$ and SDA (respect to GND) | -0.2V to 6V |
| Voltage on X1 and X2 Pins (respect to GND) . | -0.2V to 4V |
| ESD Rating ((Per MIL-STD-883 Method 3014) |  |
| Human Body Model | 4 kV |
| Machine Model. | >350V |

## Thermal Information

| Thermal Resistance (Typical) | $\theta_{\mathrm{JA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$ |
| :---: | :---: |
| 8 Lead SOIC (Note 3) | 120 |
| 8 Lead MSOP (Note 3). | 169 |
| 8 Lead $\mu$ TDFN (Note 3) | 160 |
| Storage Temperature | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Pb-free Reflow Profile . . . . . http://www.intersil.com/pbfr | . . .see link below p |

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:
3. $\theta_{\mathrm{JA}}$ is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

DC Operating Characteristics - RTC Temperature $=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$, unless otherwise stated.

| SYMBOL | PARAMETER | CONDITIONS | $\begin{gathered} \text { MIN } \\ \text { (Note 6) } \end{gathered}$ | $\begin{gathered} \text { TYP } \\ \text { (Note 5) } \end{gathered}$ | $\begin{gathered} \text { MAX } \\ \text { (Note 6) } \end{gathered}$ | UNITS | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {DD }}$ | Full Operation Power Supply |  | 1.8 |  | 3.6 | V |  |
| $\mathrm{V}_{\text {DDT }}$ | Timekeeping Power Supply |  | 1.4 |  | 1.8 | V |  |
| ${ }^{\text {d D } 1}$ | Standby Supply Current | $\mathrm{V}_{\mathrm{DD}}=3.6 \mathrm{~V}$ |  | 600 | 950 | nA | 4, 10 |
|  |  | $\mathrm{V}_{\mathrm{DD}}=3.3 \mathrm{~V}$ |  | 500 |  | nA |  |
| ${ }^{\text {IDD2 }}$ | Timekeeping Current | $\mathrm{V}_{\mathrm{DD}}=1.8 \mathrm{~V}$ |  | 400 | 650 | nA | 4, 10 |
|  |  | $\mathrm{V}_{\mathrm{DD}}=1.6 \mathrm{~V}$ |  | 350 |  | nA |  |
| ${ }^{\text {I DD3 }}$ | Supply Current With I ${ }^{2}$ C Active at Clock Speed of 400 kHz | $\mathrm{V}_{\mathrm{DD}}=3.6 \mathrm{~V}$ |  | 15 | 40 | $\mu \mathrm{A}$ | 4 |
| $\mathrm{I}_{1}$ | Input Leakage Current on SCL |  | -100 |  | 100 | nA |  |
| ILO | I/O Leakage Current on SDA |  | -100 |  | 100 | nA |  |
| $\overline{\text { IRQ1/ }}$ Fout and $\overline{\text { IRQ2 }}$ |  |  |  |  |  |  |  |
| VoL | Output Low Voltage | $\mathrm{V}_{\mathrm{DD}}=1.8 \mathrm{~V}, \mathrm{IOL}=3 \mathrm{~mA}$ |  |  | 0.4 | v |  |

Serial Interface Specifications Over the recommended operating conditions unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN <br> (Note 6) | TYP <br> (Note 5) | MAX <br> (Note 6) | UNITS | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SERIAL INTERFACE SPECS |  |  |  |  |  |  |  |
| $\mathrm{V}_{\text {IL }}$ | SDA and SCL Input Buffer LOW Voltage |  | -0.3 |  | $0.3 \times V_{\text {DD }}$ | V |  |
| $\mathrm{V}_{\mathrm{IH}}$ | SDA and SCL Input Buffer HIGH Voltage |  | $0.7 \times V_{\text {DD }}$ |  | 5.5 | V |  |
| Hysteresis | SDA and SCL Input Buffer Hysteresis |  |  | $0.04 \times \mathrm{V}_{\text {DD }}$ |  | V |  |
| VPULLUP | Maximum Pull-up voltage on SDA during $I^{2} \mathrm{C}$ communication |  |  |  | $\mathrm{V}_{\mathrm{DD}}+2$ | V | 9 |
| $\mathrm{V}_{\mathrm{OL}}$ | SDA Output Buffer LOW Voltage, Sinking 3mA | $\mathrm{V}_{\mathrm{DD}}>1.8 \mathrm{~V}, \mathrm{~V}_{\text {PULLUP }}=5.0 \mathrm{~V}$ | 0 |  | 0.4 | V |  |
| Cpin | SDA and SCL Pin Capacitance | $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{f}=1 \mathrm{MHz}, \mathrm{~V}_{\mathrm{DD}}=5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IN}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{OUT}}=0 \mathrm{~V} \end{aligned}$ |  |  | 10 | pF | 7, 8 |
| $\mathrm{f}_{\text {SCL }}$ | SCL Frequency |  |  |  | 400 | kHz |  |
| $\mathrm{t}_{\mathrm{IN}}$ | Pulse width Suppression Time at SDA and SCL Inputs | Any pulse narrower than the max spec is suppressed. |  |  | 50 | ns |  |
| $\mathrm{t}_{\text {AA }}$ | SCL Falling Edge to SDA Output Data Valid | SCL falling edge crossing $30 \%$ of $\mathrm{V}_{\mathrm{DD}}$, until SDA exits the $30 \%$ to $70 \%$ of $V_{D D}$ window. |  |  | 900 | ns | 9 |

Serial Interface Specifications Over the recommended operating conditions unless otherwise specified. (Continued)

| SYMBOL | PARAMETER | TEST CONDITIONS | $\begin{gathered} \text { MIN } \\ \text { (Note 6) } \end{gathered}$ | TYP <br> (Note 5) | $\begin{gathered} \text { MAX } \\ \text { (Note 6) } \end{gathered}$ | UNITS | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {t BuF }}$ | Time the Bus Must Be Free Before the Start of a New Transmission | SDA crossing $70 \%$ of $V_{D D}$ during a STOP condition, to SDA crossing 70\% of $V_{D D}$ during the following START condition | 1300 |  |  | ns |  |
| tow | Clock LOW Time | Measured at the $30 \%$ of $\mathrm{V}_{\text {DD }}$ crossing | 1300 |  |  | ns |  |
| $\mathrm{t}_{\mathrm{HIGH}}$ | Clock HIGH Time | Measured at the $70 \%$ of $V_{\text {DD }}$ crossing | 600 |  |  | ns |  |
| tsu:STA | START Condition Setup Time | SCL rising edge to SDA falling edge. Both crossing 70\% of $V_{D D}$ | 600 |  |  | ns |  |
| $\mathrm{t}_{\text {HD: STA }}$ | START Condition Hold Time | From SDA falling edge crossing 30\% of $\mathrm{V}_{\mathrm{DD}}$ to SCL falling edge crossing $70 \%$ of $V_{D D}$ | 600 |  |  | ns |  |
| ${ }^{\text {tsu }}$ : DAT | Input Data Setup Time | From SDA exiting the 30\% to $70 \%$ of $\mathrm{V}_{\mathrm{DD}}$ window, to SCL rising edge crossing $30 \%$ of $\mathrm{V}_{\mathrm{DD}}$ | 100 |  |  | ns |  |
| $\mathrm{t}_{\mathrm{HD}: \text { DAT }}$ | Input Data Hold Time | From SCL falling edge crossing $30 \%$ of $V_{D D}$ to SDA entering the $30 \%$ to $70 \%$ of $V_{D D}$ window | 0 |  | 900 | ns |  |
| tsu:sto | STOP Condition Setup Time | From SCL rising edge crossing 70\% of $\mathrm{V}_{\mathrm{DD}}$, to SDA rising edge crossing $30 \%$ of $V_{D D}$ | 600 |  |  | ns |  |
| thD:STO | STOP Condition Hold Time | From SDA rising edge to SCL falling edge. Both crossing $70 \%$ of $V_{D D}$ | 600 |  |  | ns |  |
| ${ }^{\text {t }}$ H | Output Data Hold Time | From SCL falling edge crossing $30 \%$ of $V_{D D}$, until SDA enters the $30 \%$ to $70 \%$ of $V_{D D}$ window | 0 |  |  | ns |  |
| $\mathrm{t}_{\mathrm{R}}$ | SDA and SCL Rise Time | From $30 \%$ to $70 \%$ of $\mathrm{V}_{\mathrm{DD}}$ | $20+0.1 \times \mathrm{Cb}$ |  | 300 | ns | 7, 8 |
| $\mathrm{t}_{\mathrm{F}}$ | SDA and SCL Fall Time | From $70 \%$ to $30 \%$ of $V_{\text {DD }}$ | $20+0.1 \times \mathrm{Cb}$ |  | 300 | ns | 7, 8, 9 |
| Cb | Capacitive Loading of SDA or SCL | Total on-chip and off-chip | 10 |  | 400 | pF | 7, 8 |
| Rpu | SDA and SCL Bus Pull-Up Resistor Off-Chip | Maximum is determined by $t_{R}$ and $t_{F}$ For $\mathrm{Cb}=400 \mathrm{pF}$, max is about $2 \mathrm{k} \Omega$ to $2.5 \mathrm{k} \Omega$. <br> For $\mathrm{Cb}=40 \mathrm{pF}$, max is about $15 \mathrm{k} \Omega$ to ~20k $\Omega$ | 1 |  |  | $\mathrm{k} \Omega$ | 7, 8 |

NOTES:
4. $\overline{\mathrm{RQ} 1} /$ FOUT inactive.
5. Typical values are for $\mathrm{T}=+25^{\circ} \mathrm{C}$ and 3.3 V supply voltage.
6. Parameters with MIN and/or MAX limits are $100 \%$ tested at $+25^{\circ} \mathrm{C}$, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Limits should be considered typical and are not production tested.
8. These are $I^{2} \mathrm{C}$ specific parameters and are not production tested, however, they are used to set conditions for testing devices to validate specification.
9. Parts will work with SDA pull-up voltage above the $V_{\text {PULLUP }}$ limit but the $t_{A A}$ and $t_{F}$ in the $I^{2} C$ parameters are not guaranteed.
10. Specified at $+25^{\circ} \mathrm{C}$.

## SDA vs SCL Timing



## Symbol Table

| WAVEFORM | INPUTS | OUTPUTS |
| :---: | :---: | :---: |
|  | Must be steady | Will be steady |
|  | May change from LOW to HIGH | Will change from LOW to HIGH |
| $\square!$ | May change from HIGH to LOW | Will change from HIGH to LOW |
|  | Don't Care: Changes Allowed | Changing: <br> State Not Known |
|  | N/A | Center Line is High Impedance |

EQUIVALENT AC OUTPUT LOAD CIRCUIT FOR $\mathrm{V}_{\mathrm{DD}}=5 \mathrm{~V}$


FIGURE 1. STANDARD OUTPUT LOAD FOR TESTING THE DEVICE WITH $\mathrm{V}_{\mathrm{DD}}=5.0 \mathrm{~V}$

Typical Performance Curves Temperature is $+25^{\circ} \mathrm{C}$ unless otherwise specified


FIGURE 2. $I_{D D 1}$ vs $V_{D D}$


FIGURE 4. IDD vs $V_{D D}$ vs Fout

## General Description

The ISL12057 device is a low power real time clock with clock/calendar, power fail indicator, and alarm function.

The oscillator uses an external, low-cost 32.768 kHz crystal. The real time clock tracks time with separate registers for hours, minutes, and seconds. The device has calendar registers for date, month, year and day of the week. The calendar is accurate through 2099, with automatic leap year correction.

The ISL12057 has two flexible alarms; each can be set to any clock/calendar value for a match. For example, every minute, every Tuesday or at 5:23 AM on 1st day of a month. The alarm status is available by checking the Status Register, or the device can be configured to provide a hardware interrupt via the $\overline{\mathrm{IRQ} 1} / \mathrm{F}_{\mathrm{OUT}}$ or $\overline{\mathrm{RQQ2}} \mathrm{pin}$. There is a repeat mode for the alarm allowing a periodic interrupt every second or every minute.


FIGURE 3. IDD1 vs TEMPERATURE


FIGURE 5. FOUT VS $V_{\text {DD }}$ WITH A TYPICAL 32.768kHZ CRYSTAL

## Pin Description

## X1, X2

The X 1 and X 2 pins are the input and output, respectively, of an inverting amplifier. An external 32.768 kHz quartz crystal is used with the ISL12057 to supply a timebase for the real time clock. Refer to Figure 6.

The device can also be driven directly from a 32.768 kHz square wave source with peak-to-peak voltage from 0 V to VDD at X 1 pin with X 2 pin floating.


FIGURE 6. RECOMMENDED CRYSTAL CONNECTION

## $\overline{\text { IRQ1/Fout (Interrupt Output 1/Frequency Output) }}$

This dual function pin can be used as an alarm interrupt or frequency output pin. The $\overline{\mathrm{IRQ1}} / \mathrm{F}_{\text {OUT }}$ mode is selected via the control register (address 0Eh). The $\overline{\mathrm{IRQ} 1 / F_{\text {OUT }} \text { is an }}$ open drain output.

This pin has a default output of 32.768 kHz at power-up.

- Interrupt Mode. The pin provides an interrupt signal output. This signal notifies a host processor that an alarm has occurred and requests action.
- Frequency Output Mode. The pin outputs a clock signal which is related to the crystal frequency. The frequency output is user selectable and enabled via the $\mathrm{I}^{2} \mathrm{C}$ bus.


## $\overline{I R Q 2}$ (Interrupt Output 2)

The $\overline{\mathrm{IRQ} 2}$ pin is used as an Alarm1 interrupt or/and Alarm2 interrupt. The $\overline{\mathrm{IRQ2}}$ mode is selected via the control register (address 0Eh). The $\overline{\mathrm{IRQ2}}$ is an open drain output.

This pin is high impedance at power-up.
The pin provides an interrupt signal output. This signal notifies a host processor that an alarm has occurred and requests action.

## Serial Clock (SCL)

The SCL input is used to clock all serial data into and out of the device. The input buffer on this pin is always active (not gated). The SCL pin can accept a logic high voltage up to 5.5 V .

## Serial Data (SDA)

SDA is a bi-directional pin used to transfer data into and out of the device. It has an open drain output and may be ORed with other open drain or open collector outputs. The input buffer is always active (not gated) in normal mode.

An open drain output requires the use of a pull-up resistor, and it can accept a pull-up voltage up to 5.5 V . The output circuitry controls the fall time of the output signal with the use of a slope controlled pull-down. The circuit is designed for $400 \mathrm{kHz} \mathrm{I}^{2} \mathrm{C}$ interface speeds.

NOTE: Parts will work with SDA pull-up voltage above the $V_{\text {PULLUP }}$ limit but the $\mathrm{t}_{\mathrm{AA}}$ and $\mathrm{t}_{\mathrm{F}}$ in the $\mathrm{I}^{2} \mathrm{C}$ parameters are not guaranteed.

## $V_{D D}, G N D$

Chip power supply and ground pins. The device will have full operation with a power supply from 1.8 V to 3.6 VDC , and timekeeping function with a power supply from 1.4 V to 1.8 V .

A $0.1 \mu \mathrm{~F}$ decoupling capacitor is recommended on the $\mathrm{V}_{\mathrm{DD}}$ pin to ground.

## Functional Description

## Real Time Clock Operation

The Real Time Clock (RTC) uses an external 32.768 kHz quartz crystal to maintain an accurate internal representation of second, minute, hour, day of week, date, month, and year. The RTC also has leap-year correction. The RTC also
corrects for months having fewer than 31 days and has a bit that controls 24 -hour or AM/PM format. The clock will begin incrementing after power-up with valid oscillator condition.

## ACCURACY OF THE REAL TIME CLOCK

The accuracy of the Real Time Clock depends on the frequency of the quartz crystal that is used as the time base for the RTC. Since the resonant frequency of a crystal is temperature dependent, the RTC performance will also be dependent upon temperature. The frequency deviation of the crystal is a function of the turnover temperature of the crystal from the crystal's nominal frequency. For example, a ~20ppm frequency deviation translates into an accuracy of $\sim 1$ minute per month. These parameters are available from the crystal manufacturer.

## $1^{2} C$ Serial Interface

The ISL12057 has an I ${ }^{2}$ C serial bus interface that provides access to the real time clock registers, control and status registers and the alarm registers. The $I^{2} \mathrm{C}$ serial interface is compatible with other industry $\mathrm{I}^{2} \mathrm{C}$ serial bus protocols using a bidirectional data signal (SDA) and a clock signal (SCL).

## Register Descriptions

The registers are accessible following a slave byte of " $1101000 x$ " and reads or writes to addresses [00h:0Fh]. The defined addresses and default values are described in Table 1.

## REGISTER ACCESS

The contents of the registers can be modified by performing a byte or a page write operation directly to any register address. The address will wrap around from OFh to 00h.

The registers are divided into 3 sections. These are:

1. Real Time Clock ( 7 bytes): Address 00 h to 06 h .
2. Alarm ( 7 bytes): Address 07 h to 0Dh.
3. Control and Status (2 bytes): Address OEh to OFh.

There are no addresses above 0Fh.
A register can be read by performing a random read at any address at any time. This returns the contents of that register location. Additional registers are read by performing a sequential read. For the RTC registers, the read instruction latches all clock registers into a buffer, so an update of the clock does not change the time being read. A sequential read will not result in the output of data from the memory array. At the end of a read, the master supplies a stop condition to end the operation and free the bus. After a read or write instruction, the address remains at the previous address +1 so the user can execute a current address read and continue reading the next register.

TABLE 1. REGISTER MEMORY MAP

| ADDR | SECTION | REG NAME | BIT |  |  |  |  |  |  |  | REG |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | RANGE | DEFAULT |
| 00H | RTC | SC | 0 | SC22 | SC21 | SC20 | SC13 | SC12 | SC11 | SC10 | 0-59 | 00h |
| 01H |  | MN | 0 | MN22 | MN21 | MN2O | MN13 | MN12 | MN11 | MN10 | 0-59 | 00h |
| 02H |  | HR | 0 | $\overline{\text { MIL }}$ | $\overline{\text { AM/PM }}$ | HR20 | HR13 | HR12 | HR11 | HR10 | $\begin{gathered} 1-12 \\ + \text { AM/PM } \end{gathered}$ | 00h |
|  |  |  |  |  | HR21 |  |  |  |  |  | 0-23 |  |
| 03H |  | DW | 0 | 0 | 0 | 0 | 0 | DW12 | DW11 | DW10 | 1-7 | 01h |
| 04H |  | DT | 0 | 0 | DT21 | DT20 | DT13 | DT12 | DT11 | DT10 | 1-31 | 01h |
| 05H |  | MO | CENTUR Y | 0 | 0 | MO20 | MO13 | MO12 | MO11 | MO10 | $\begin{gathered} \text { 0-12 } \\ \text { +Century } \end{gathered}$ | 01h |
| 06h |  | YR | YR23 | YR22 | YR21 | YR20 | YR13 | YR12 | YR11 | YR10 | 0-99 | 00h |
| 07h | Alarm1 | A1SC | A1M1 | A1SC22 | A1SC21 | A1SC20 | A1SC13 | A1SC12 | A1SC11 | A1SC10 | 0-59 | 00h |
| 08h |  | A1MN | A1M2 | A1MN22 | A1MN21 | A1MN20 | A1MN13 | A1MN12 | A1MN11 | A1MN10 | 0-59 | 00h |
| 09h |  | A1HR | A1M3 | A1 $\overline{\mathrm{MIL}}$ | A1 $\overline{\mathrm{AM}} / \mathrm{PM}$ | A1HR20 | A1HR13 | A1HR12 | A1HR11 | A1HR10 | $\begin{gathered} \text { 1-12 } \\ +\mathrm{AM} / \mathrm{PM} \end{gathered}$ | 00h |
|  |  |  |  |  | A1HR21 |  |  |  |  |  | 0-23 |  |
| OAh |  | $\frac{\mathrm{A} 1 \mathrm{DW} /}{\mathrm{DT}}$ | A1M4 | A1DW/ $\overline{\mathrm{DT}}$ | 0 | 0 | 0 | A1DW12 | A1DW11 | A1DW10 | 1-7 | 00h |
|  |  |  |  |  | A1DT21 | A1DT20 | A1DT13 | A1DT12 | A1DT11 | A1DT10 | 1-31 | 00h |
| OBh | Alarm2 | A2MN | A2M2 | A2MN22 | A2MN21 | A2MN20 | A2MN13 | A2MN12 | A2MN11 | A2MN10 | 0-59 | 00h |
| 0Ch |  | A2HR | A2M3 | A2 $\overline{\mathrm{MIL}}$ | A2 $\overline{\mathrm{AM}} / \mathrm{PM}$ | A2HR20 | A2HR13 | A2HR12 | A2HR11 | A2HR10 | $\begin{gathered} 1-12 \\ +\mathrm{AM} / \mathrm{PM} \end{gathered}$ | 00h |
|  |  |  |  |  | A2HR21 |  |  |  |  |  | 0-23 |  |
| ODh |  | $\frac{\mathrm{A} 2 \mathrm{DW} /}{\mathrm{DT}}$ | A2M4 | A2DW/DT | 0 | 0 | 0 | A2DW12 | A2DW11 | A2DW10 | 1-7 | 00h |
|  |  |  |  |  | A2DT21 | A2DT20 | A2DT13 | A2DT12 | A2DT11 | A2DT10 | 1-31 | 00h |
| OEh | Control | INT | $\overline{\text { EOSC }}$ | 0 | 0 | RS2 | RS1 | INTCN | A2IE | A1IE | N/A | 18h |
| OFh | Status | SR | OSF | 0 | 0 | 0 | 0 | 0 | A2F | A1F | N/A | 80h |

## Real Time Clock Registers

## Addresses [00h to 06h]

## RTC REGISTERS (SC, MN, HR, DW, DT, MO, YR)

These registers depict BCD representations of the time. As such, SC (Seconds, address 00h) and MN (Minutes, address 01h) range from 0 to 59, HR (Hour, address 02h) can either be a 12 -hour or 24 -hour mode, DW (Day of the Week, address 03 h ) is 1 to 7 , DT (Date, address 04 h ) is 1 to 31 , MO (Month, address 05h) is 1 to 12 , and YR (Year, address 06 h ) is 0 to 99.

The DW register provides a Day of the Week status and uses 3 bits DW2 to DW0 to represent the seven days of the week. The counter advances in the cycle 1-2-3-4-5-6-7-1-2-... The assignment of a numerical value to a specific day of the week is arbitrary and may be decided by the system software designer.

## 24-HOUR TIME

If the $\overline{\text { MIL }}$ bit of the HR register is " 0 ", the RTC uses a 24-hour format and bit 5 of the HR register is the second 10 -hour bit ( $20-23$ hours). If the MIL bit is " 1 ", the RTC uses a 12-hour format and bit 5 of the HR register is the $\overline{\mathrm{AM}} / \mathrm{PM}$
bit with logic high being PM. The clock defaults to 24 -hour format time.

## CENTURY INDICATOR

The century bit (bit 7 of the MO register) is toggled when the years register overflows from 99 to 00 to indicator the change of century.

## LEAP YEARS

Leap years add the day February 29 and are defined as those years that are divisible by 4. Years divisible by 100 are not leap years, unless they are also divisible by 400 . This means that the year 2000 is a leap year, the year 2100 is not. The ISL12057 does not correct for the leap year in the year 2100.

## Addresses [0Eh to OFh]

The Control and Status Registers consist of the Status Register, Interrupt and Alarm Register.

## Interrupt Control Register (INT) [Address 0Eh]

TABLE 2. INTERRUPT CONTROL REGISTER (INT)

| ADDR | $\mathbf{7}$ | $\mathbf{6}$ | $\mathbf{5}$ | $\mathbf{4}$ | $\mathbf{3}$ | $\mathbf{2}$ | $\mathbf{1}$ | $\mathbf{0}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| OEh | EOSC | 0 | 0 | RS2 | RS1 | INTCN | A2IE | A1IE |
| Default | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

## OSCILLATOR ENABLE BIT (EOSC)

The $\overline{\mathrm{EOSC}}$ bit enables the crystal oscillator function when it is set to " 0 ". When the $\overline{\mathrm{EOSC}}$ bit is set to " 1 ", the crystal oscillator function is disable and the device enters into power saving mode. The $\overline{\text { EOSC }}$ bit is set to " 0 " at power-up.

## FREQUENCY OUT CONTROL BITS (RS2, RS1)

These bits select the output frequency at the $\overline{\mathrm{RQQ1}} / \mathrm{F}_{\text {OUT }}$ pin. INTCN must be set to " 0 " for frequency output at the $\overline{\mathrm{IRQ}} / \mathrm{F}_{\text {OUT }}$ pin. Please see Table 3 for Frequency Selection of the Fout pin.

TABLE 3. FREQUENCY SELECTION OF FOUT PIN

| FREQUENCY <br> FOUT (Hz) | RS2 | RS1 | COMMENT |
| :---: | :---: | :---: | :--- |
| 32768 | 1 | 1 | Free running crystal clock |
| 8192 | 1 | 0 | Free running crystal clock |
| 4096 | 0 | 1 | Free running crystal clock |
| 1 | 0 | 0 | Sync at RTC write |

## INTERRUPT CONTROL BIT (INTCN) AND ALARM INTERRUPT ENABLE BITS (A2IE, A1IE)

The INTCN bit controls the relationship between the alarm interrupts and the $\overline{\mathrm{IRQ} 1} / \mathrm{F}_{\text {OUT }}$ and $\overline{\mathrm{IRQ} 2}$ pins. The A2IE and A1IE bits enable the alarm interrupts, A2F and A1F, to assert the $\overline{\mathrm{IRQ} 1} / \mathrm{F}_{\text {OUT }}$ and $\overline{\mathrm{IRQ} 2}$ pins. Please see Table 4 for Alarm Interrupt Selection with INTCN, A2IE and A1IE bits.

TABLE 4. ALARM INTERRUPT SELECTION WITH INTCN, A2IE AND A1IE BITS

| INTCN | A2IE | A1IE | $\overline{\text { IRQ1/FOUT }}$ | $\overline{\text { IRQ2 }}$ |
| :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | FOUT | HIGH |
| 0 | 0 | 1 | FOUT | A1F |
| 0 | 1 | 0 | FOUT | A2F |
| 0 | 1 | 1 | FOUT | A1F or A2F |
| 1 | 0 | 0 | HIGH | HIGH |
| 1 | 0 | 1 | HIGH | A1F |
| 1 | 1 | 0 | A2F | HIGH |
| 1 | 1 | 1 | A2F | A1F |

## Status Register (SR) [Address 0Fh]

The Status Register is located in the memory map at address 0Fh. This is a volatile register that provides status of oscillator failure and alarm interrupts.

TABLE 5. STATUS REGISTER (SR)

| ADDR | $\mathbf{7}$ | $\mathbf{6}$ | $\mathbf{5}$ | $\mathbf{4}$ | $\mathbf{3}$ | $\mathbf{2}$ | $\mathbf{1}$ | $\mathbf{0}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| OFh | OSF | 0 | 0 | 0 | 0 | 0 | A2F | A1F |
| Default | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## ALARM1 INTERRUPT BIT (A1F)

These bits announce if the Alarm1 matches the real time clock. If there is a match, the respective bit is set to " 1 ". This bit is manually reset to " 0 " by the user. A write to this bit in the SR can only set it to " 0 ", not " 1 ".

## ALARM2 INTERRUPT BIT (A2F)

These bits announce if the Alarm2 matches the real time clock. If there is a match, the respective bit is set to " 1 ". This bit is manually reset to " 0 " by the user. A write to this bit in the SR can only set it to " 0 ", not " 1 ".

## OSCILLATOR FAILURE BIT (OSF)

This bit is set to a " 1 " when there is no oscillation on X1 pin. This is set by hardware (ISL12057 internally), and can only be disabled by having an oscillation on X1 and and manually reset to "0" to reset it..

## Alarm1 Registers

## Addresses [Address 07h to 0Ah]

The Alarm1 register bytes are set up identical to the RTC register bytes, except that the MSB of each byte functions as an enable bit (enable $=$ " 0 "). These enable bits specify which alarm registers (seconds, minutes, etc) are used to make the comparison. When all the enable bits are set to " 1 ", the Alarm1 will trigger once per second. Note that there is no alarm byte for month and year.

The Alarm1 function works as a comparison between the Alarm1 registers and the RTC registers. As the RTC advances, the Alarm1 will be triggered once a match occurs between the Alarm1 registers and the RTC registers. Any one Alarm1 register, multiple registers, or all registers can be enabled for a match.

To clear an Alarm1, the A1F status bit must be set to " 0 " with a write.

TABLE 6. ALARM1 INTERRUPT WITH ENABLE BITS SELECTION

| A1DWIDT | A1M1 | A1M2 | A1M3 | A1M4 | ALARM1 INTERRUPT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $X$ | 1 | 1 | 1 | 1 | Every Second |
| $X$ | 0 | 1 | 1 | 1 | Match Second |
| $X$ | 1 | 0 | 1 | 1 | Match Minute |

TABLE 6. ALARM1 INTERRUPT WITH ENABLE BITS SELECTION (Continued)

| A1DWI $\overline{\text { DT }}$ | A1M1 | A1M2 | A1M3 | A1M4 | ALARM1 INTERRUPT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| X | 1 | 1 | 0 | 1 | Match Hour |
| 0 | 1 | 1 | 1 | 0 | Match Date |
| 1 | 1 | 1 | 1 | 0 | Match Day |
| 0 | 0 | 0 | 1 | 1 | Match Second and Minute |
| 0 | 0 | 1 | 0 | 1 | Match Second and Hour |
| 0 | 0 | 0 | 0 | 0 | Match Second, Minute <br> and Hour |
| $\cdot$ | $\cdot$ | $\cdot$ | $\cdot$ | $\cdot$ | $\cdot$ |
| 0 | 1 | 0 | 0 | 0 | Match Minute Hour and <br> Date |
| 0 | 0 | 0 | 0 | 0 | Match Second, Minute <br> Hour and Date |
| $\cdot$ | $\cdot$ | $\cdot$ | $\cdot$ | $\cdot$ | $\cdot$ <br> $\cdot$ <br> $\cdot$ |
| 1 | 1 | 0 | 0 | 0 | Match Minute, Hour, and <br> Day |
| 1 | 0 | 0 | 0 | 0 | Match Second, Minute, <br> Hour, and Day |

Note: X is don't care, it can be set to 0 or 1 .
Following is example of Alarm1 Interrupt.
Example - A single alarm will occur on Monday at 11:30am (Monday is when DW = 2).
A. Set Alarm1 registers as follows:

| ALARM1 <br> REGISTER | $\mathbf{7}$ | $\mathbf{6}$ | $\mathbf{5}$ | $\mathbf{4}$ | $\mathbf{3}$ | $\mathbf{2}$ | $\mathbf{1}$ | $\mathbf{0}$ | HEX | DESCRIPTION |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 80 h |  |
| A1HR | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 30 h | Minutes set to 30, <br> enabled |  |
| A1DW/DT | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 42 h | Day set to 1, <br> enabled |

After these registers are set, an alarm will be generated when the RTC advances to exactly 11:30am on January 1 (after seconds changes from 59 to 00) by setting the A1F bit in the status register to " 1 ".

## Alarm2 Registers

## Addresses [Address 12h to 14h]

The Alarm2 register bytes are set up identical to the RTC register bytes except that the MSB of each byte functions as an enable bit (enable = " 0 "). These enable bits specify which alarm registers (minutes, hour, and date/day) are used to
make the comparison. When all the enable bits are set to " 1 ", the Alarm2 will trigger once per minute. Note that there are no alarm bytes for second, month and year.

The Alarm2 function works as a comparison between the Alarm2 registers and the RTC registers. As the RTC advances, the Alarm 2 will be triggered once a match occurs between the Alarm2 registers and the RTC registers. Any one Alarm2 register, multiple registers, or all registers can be enabled for a match.

To clear an Alarm2, the A2F status bit must be set to "0" with a write.

TABLE 7. ALARM2 INTERRUPT WITH ENABLE BITS SELECTION

| A2DWIDT | A2M2 | A2M3 | A2M4 | ALARM2 INTERRUPT |
| :---: | :---: | :---: | :---: | :---: |
| X | 1 | 1 | 1 | Every Minute (Second=00) |
| X | 0 | 1 | 1 | Match Minute |
| X | 1 | 0 | 1 | Match Hour |
| 0 | 1 | 1 | 0 | Match Date |
| 1 | 1 | 1 | 0 | Match Day |
| X | 0 | 0 | 1 | Match Minute and Hour |
| 0 | 1 | 0 | 0 | Match Hour and Date |
| 0 | 0 | 1 | 0 | Match Minute and Date |
| 0 | 0 | 0 | 0 | Match Minute, Hour, and Date |
| 1 | 0 | 1 | 0 | Match Minute and Day |
| 1 | 1 | 0 | 0 | Match Hour and Day |
| 1 | 0 | 0 | 0 | Match Minute, Hour, and Day |

Note: X is don't care, it can be set to 0 or 1.
Following is example of Alarm2 Interrupt.
Example - A single alarm will occur on every 1st day of the month at 20:00 military time.
A. Set Alarm registers as follows:

| ALARM2 <br> REGISTER |  |  |  |  |  |  |  |  | $\mathbf{7}$ | $\mathbf{6}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\mathbf{4}$ | $\mathbf{3}$ | $\mathbf{2}$ | $\mathbf{1}$ | $\mathbf{0}$ | HEX | DESCRIPTION |  |  |  |
| A2MN | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 80 h | Minutes disabled |
| A2HR | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20h | Hours set to 20, <br> enabled |
| A2DW/DT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01h | Date set to 1st, <br> enabled |

After these registers are set, an alarm will be generated when the RTC advances to exactly 20:00 on Monday (after minutes changes from 59 to 00 ) by setting the A2F bit in the status register to " 1 ".

## $I^{2} \mathrm{C}$ Serial Interface

The ISL12057 supports a bi-directional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL12057 operates as a slave device in all applications.

All communication over the $\mathrm{I}^{2} \mathrm{C}$ interface is conducted by sending the MSB of each byte of data first.

## Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 7). On power-up of the ISL12057, the SDA pin is in the input mode.
All I ${ }^{2}$ C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL12057 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see

Figure 7). A START condition is ignored during the power-up sequence.
All $I^{2} \mathrm{C}$ interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 7). A STOP condition at the end of a read operation or at the end of a write operation to memory only places the device in its standby mode.

An acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting 8 bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the 8 bits of data (see Figure 8).

The ISL12057 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL12057 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.


FIGURE 7. VALID DATA CHANGES, START, AND STOP CONDITIONS


FIGURE 8. ACKNOWLEDGE RESPONSE FROM RECEIVER


FIGURE 9. SEQUENTIAL BYTE WRITE SEQUENCE

## Device Addressing

Following a start condition, the master must output a Slave Address Byte. The 7 MSBs are the device identifier. These bits are "1101000". Slave bits "1101" access the register. Slave bits "000" specify the device select bits.

The last bit of the Slave Address Byte defines a read or write operation to be performed. When this $R / \bar{W}$ bit is a " 1 ", then a read operation is selected. A " 0 " selects a write operation (refer to Figure 10).
After loading the entire Slave Address Byte from the SDA bus, the ISL12057 compares the device identifier and device select bits with "1101000". Upon a correct compare, the device outputs an acknowledge on the SDA line.

Following the Slave Byte is a one byte word address. The word address is either supplied by the master device or obtained from an internal counter. On power-up, the internal address counter is set to address $0 h$, so a current address read of the RTC array starts at address Oh. When required, as part of a random read, the master must supply the 1 Word Address Bytes as shown in Figure 11.

In a random read operation, the slave byte in the "dummy write" portion must match the slave byte in the "read" section. For a random read of the Clock/Control Registers, the slave byte must be " $1101000 x$ " in both places.


FIGURE 10. SLAVE ADDRESS, WORD ADDRESS, AND DATA BYTES

## Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL12057 responds with an ACK. At this time, the $I^{2} C$ interface enters a standby state.

## Read Operation

A Read operation consists of a three byte instruction followed by one or more Data Bytes (see Figure 11). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R//W bit set to " 0 ", an Address Byte, a second START, and a second Identification byte with the R/W bit set to "1". After each of the three bytes, the ISL12057 responds with an ACK. Then the ISL12057 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a STOP condition) following the last bit of the last Data Byte (see Figure 11).

The Data Bytes are from the memory location indicated by an internal pointer. This pointer's initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location 13 h , the pointer "rolls over" to 00 h , and the device continues to output data for each ACK received.

## Application Section



FIGURE 11. READ SEQUENCE

## Oscillator Crystal Requirements

The ISL12057 uses a standard 32.768 kHz crystal. Either through hole or surface mount crystals can be used. Table 8 lists some recommended surface mount crystals and the parameters of each. This list is not exhaustive and other surface mount devices can be used with the ISL12057 if their specifications are very similar to the devices listed. The crystal should have a required parallel load capacitance of 6 pF and an equivalent series resistance of less than 50k. The crystal's temperature range specification should match the application. Many crystals are rated for $-10^{\circ} \mathrm{C}$ to $+60^{\circ} \mathrm{C}$ (especially through-hole and tuning fork types), so an appropriate crystal should be selected if extended temperature range is required.

TABLE 8. SUGGESTED SURFACE MOUNT CRYSTALS

| MANUFACTURER | PART NUMBER |
| :---: | :---: |
| Citizen | CM200S |
| MicroCrystal | MS3V |
| ECS | ECX-306 |

## Layout Considerations

The crystal input at X1 has a very high impedance, and oscillator circuits operating at low frequencies (such as 32.768 kHz ) are known to pick up noise very easily if layout precautions are not followed. Most instances of erratic clocking or large accuracy errors can be traced to the susceptibility of the oscillator circuit to interference from adjacent high speed clock or data lines. Careful layout of the RTC circuit will avoid noise pickup and insure accurate clocking.

Figure 12 shows a suggested layout for the ISL12057 device using a surface mount crystal. Two main precautions should be followed:

1. Do not run the serial bus lines or any high speed logic lines in the vicinity of the crystal. These logic level lines can induce noise in the oscillator circuit to cause misclocking.
2. Add a ground trace around the crystal with one end terminated at the chip ground. This will provide termination for emitted noise in the vicinity of the RTC device.


FIGURE 12. SUGGESTED LAYOUT FOR ISL12057 AND CRYSTAL

In addition, it is a good idea to avoid a ground plane under the X 1 and X 2 pins and the crystal, as this will affect the load capacitance and therefore the oscillator accuracy of the circuit. If the $\overline{\mathrm{IRQ}} / \mathrm{F}_{\text {OUT }}$ pin is used as a clock, it should be routed away from the RTC device as well. The trace for the $\mathrm{V}_{\mathrm{CC}}$ pins can be treated as a ground, and should be routed around the crystal.

Mini Small Outline Plastic Packages (MSOP)


NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension " $D$ " does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15 mm ( 0.006 inch) per side.
4. Dimension "E1" does not include interlead flash or protrusions and are measured at Datum Plane. $-\mathrm{H}-$ Interlead flash and protrusions shall not exceed 0.15 mm ( 0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within $0.10 \mathrm{~mm}(0.004)$ at seating Plane.
6. " $L$ " is the length of terminal for soldering to a substrate.
7. " $N$ " is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm ( 0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07 mm ( 0.0027 inch).
10. Datums $-\mathrm{A}-$ and $-\mathrm{B}-$ to be determined at Datum plane $-\mathrm{H}_{-}$.
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

M8.118 (JEDEC MO-187AA)
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

| SYMBOL | INCHES |  | MILLIMETERS |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |  |
| A | 0.037 | 0.043 | 0.94 | 1.10 | - |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 | - |
| A2 | 0.030 | 0.037 | 0.75 | 0.95 | - |
| b | 0.010 | 0.014 | 0.25 | 0.36 | 9 |
| c | 0.004 | 0.008 | 0.09 | 0.20 | - |
| D | 0.116 | 0.120 | 2.95 | 3.05 | 3 |
| E1 | 0.116 | 0.120 | 2.95 | 3.05 | 4 |
| e | 0.026 |  | BSC | 0.65 |  |
| BSC | - |  |  |  |  |
| E | 0.187 | 0.199 | 4.75 | 5.05 | - |
| L | 0.016 | 0.028 | 0.40 | 0.70 | 6 |
| L1 | 0.037 |  | REF | 0.95 |  |
| REF | - |  |  |  |  |
| N | 8 |  |  | 8 |  |
| R | 0.003 | - | 0.07 | - | 7 |
| R1 | 0.003 | - | 0.07 | - | - |
| 0 | $5^{\circ}$ | $15^{\circ}$ | $5^{\circ}$ | $15^{\circ}$ | - |
| $\alpha$ | $0^{\circ}$ | $6^{\circ}$ | $0^{\circ}$ | $6^{\circ}$ | - |

Rev. 2 01/03

## Package Outline Drawing

## L8.2x2

8 Lead Ultra Thin Dual Flat No-Lead COL Plastic Package (UTDFN COL)
Rev 3, 11/07

$\xlongequal{\text { TYPICAL RECOMMENDED LAND PATTERN }}$

$\underline{\underline{\text { BOTTOM VIEW }}}$


NOTES:

1. Dimensions are in millimeters.

Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal $\pm 0.05$
4. Dimension $b$ applies to the metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin \#1 identifier is optional, but must be located within the zone indicated. The pin \#1 identifier may be either a mold or mark feature.

## Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension " $D$ " does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15 mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25 mm ( 0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. " $L$ " is the length of terminal for soldering to a substrate.
7. " N " is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36 mm ( 0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61 mm ( 0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C) 8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

| SYMBOL | INCHES |  | MILLIMETERS |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |  |  |  |  |  |  |  |  |
| A | 0.0532 | 0.0688 | 1.35 | 1.75 | - |  |  |  |  |  |  |  |
| A1 | 0.0040 | 0.0098 | 0.10 | 0.25 | - |  |  |  |  |  |  |  |
| B | 0.013 | 0.020 | 0.33 | 0.51 | 9 |  |  |  |  |  |  |  |
| C | 0.0075 | 0.0098 | 0.19 | 0.25 | - |  |  |  |  |  |  |  |
| D | 0.1890 | 0.1968 | 4.80 | 5.00 | 3 |  |  |  |  |  |  |  |
| E | 0.1497 | 0.1574 | 3.80 | 4.00 | 4 |  |  |  |  |  |  |  |
| e | 0.050 |  | BSC | 1.27 |  |  |  |  |  |  |  |  |
| BSC | - |  |  |  |  |  |  |  |  |  |  |  |
| H | 0.2284 | 0.2440 | 5.80 | 6.20 | - |  |  |  |  |  |  |  |
| h | 0.0099 | 0.0196 | 0.25 | 0.50 | 5 |  |  |  |  |  |  |  |
| L | 0.016 | 0.050 | 0.40 | 1.27 | 6 |  |  |  |  |  |  |  |
| N | 8 |  |  |  |  |  |  |  |  |  |  |  |
| $\alpha$ | $0^{\circ}$ | $8^{\circ}$ | $0^{\circ}$ | $8^{\circ}$ | - |  |  |  |  |  |  |  |

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