HARRIS SEMICONDUCTOR

CD54AC191/3A
CD54ACT191/3A

Presettable Synchronous 4-Bit Binary Up/Down Counters

June 1997

COMPLETE DATA SHEET COMING SOON!

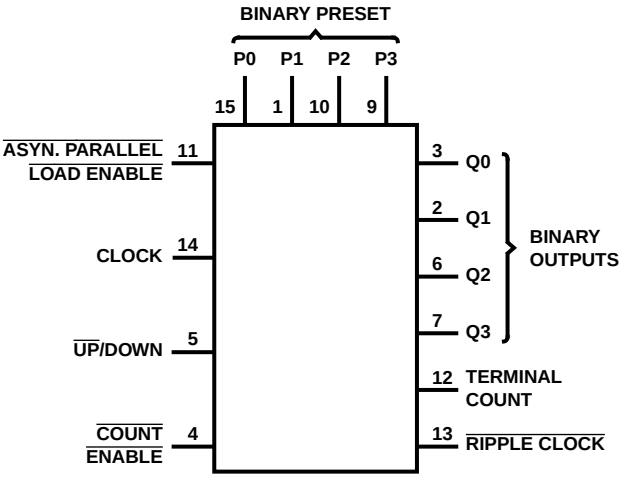
Description

The CD54AC191/3A and CD54ACT191/3A are asynchronously presettable binary up/down synchronous counters that utilize the Harris Advanced CMOS Logic technology. Presetting the counter to the number on preset data inputs (P0-P3) is accomplished by setting LOW the asynchronous parallel load input ($\overline{PL}$). Counting occurs when $\overline{PL}$ is HIGH. Count Enable ($\overline{CE}$) is LOW, and the Up/Down ($\overline{U}$/D) input is either LOW for up-counting or HIGH for down-counting. The counter is incremented or decremented synchronously with the LOW-to-HIGH transition of the clock.

When an overflow or underflow of the counter occurs, the Terminal Count (TC) output, which is LOW during counting, goes HIGH and remains HIGH for one clock cycle. This output can be used for look-ahead carry in high-speed cascading. The TC output also initiates the Ripple Clock ($\overline{RC}$) output which, normally HIGH, goes LOW and remains LOW for the low-level portion of the clock pulse. These counters can be cascaded using the Ripple Count output.

The CD54AC191/3A and CD54ACT191/3A are supplied in 16-lead dual-in-line ceramic packages (F suffix).

Functional Diagram



ACT INPUT LOAD TABLE

INPUT	UNIT LOAD (NOTE 1)
P0 - P3, $\overline{PL}$	0.75
CL, $\overline{U}$/D, $\overline{CE}$	0.85

NOTE:

1. Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA Max at +25°C.

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to +6V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±50mA
DC Output Source or Sink Current, Per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±50mA
DC V_{CC} or GND Current, I_{CC} or I_{GND}
For Up to 4 Outputs Per Device, Add ±25mA For Each Additional Output . . . . . ±100mA

Power Dissipation Per Package, P_D
T_A = -55°C to +100°C (Package F) 500mW
T_A = +100°C to +125°C (Package F) . . . . . Derate Linearly at 8mW/°C to 300mW
Operating Temperature Range, T_A
Package Type F . . . . . -55°C to +125°C
Storage Temperature, T_{STG} . . . . . -65°C to +150°C
Lead Temperature (During Soldering)
At Distance 1/16in. ± 1/32in. (1.59mm ± 0.79mm)
From Case For 10s Max . . . . . +265°C
Unit Inserted Into a PC Board (Min Thickness 1/16in., 1.59mm)
With Solder Contacting Lead Tips Only . . . . . +300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Supply Voltage Range, V_{CC}
Unless Otherwise Specified, All Voltages Referenced to GND
T_A = Full Package Temperature Range
CD54AC Types . . . . . 1.5V to 5.5V
CD54ACT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}

Operating Temperature, T_A . . . . . -55°C to +125°C
Input Rise and Fall Slew Rate, dt/dv
at 1.5V to 3V (AC Types) . . . . . 0ns/V to 50ns/V
at 3.6V to 5.5V (AC Types) . . . . . 0ns/V to 20ns/V
at 4.5V to 5.5V (AC Types) . . . . . 0ns/V to 10ns/V

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3896**