FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27222-1E

ASSP For Power Supply Applications

6-ch DC/DC Converter IC

With Synchronous Rectification for voltage step-up and step-down

MB3827

■ DESCRIPTION

The MB3827 is a pulse width modulation (PWM) type 6-channel DC/DC converter IC with, synchronous rectification for voltage step-up and step-down. The MB3827 is ideal for low voltage, high efficiency, compact applications and for down conversion and up/down conversion (with two types of voltage step-up/step-down methods allowing input/output relations to be set independently).

In addition the MB3827 features a built-in self-supply power channel (channel 7) providing a wide range of supply voltages, and operates from two dry-cell batteries.

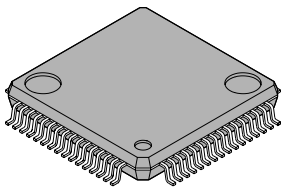
This product is ideal for high performance portable devices such as digital still cameras.

■ FEATURES

- Compatible with step-up/step-down switching methods (channel 1)
- Compatible with step-up/step-down Zeta methods (channels 2 to 6)
- Synchronous rectification (channels 1 and 2)
- Low start-up voltage : 1.8 V (channel 7 for self-power supply)
- Power supply voltage range : 4 V to 13 V (channels 1 to 6)
- Built-in high-precision reference voltage generator : 2.5 V±1%
- Oscillator frequency range : 100 kHz to 800 kHz
- Error amplifier output for soft start (channels 1 to 6)

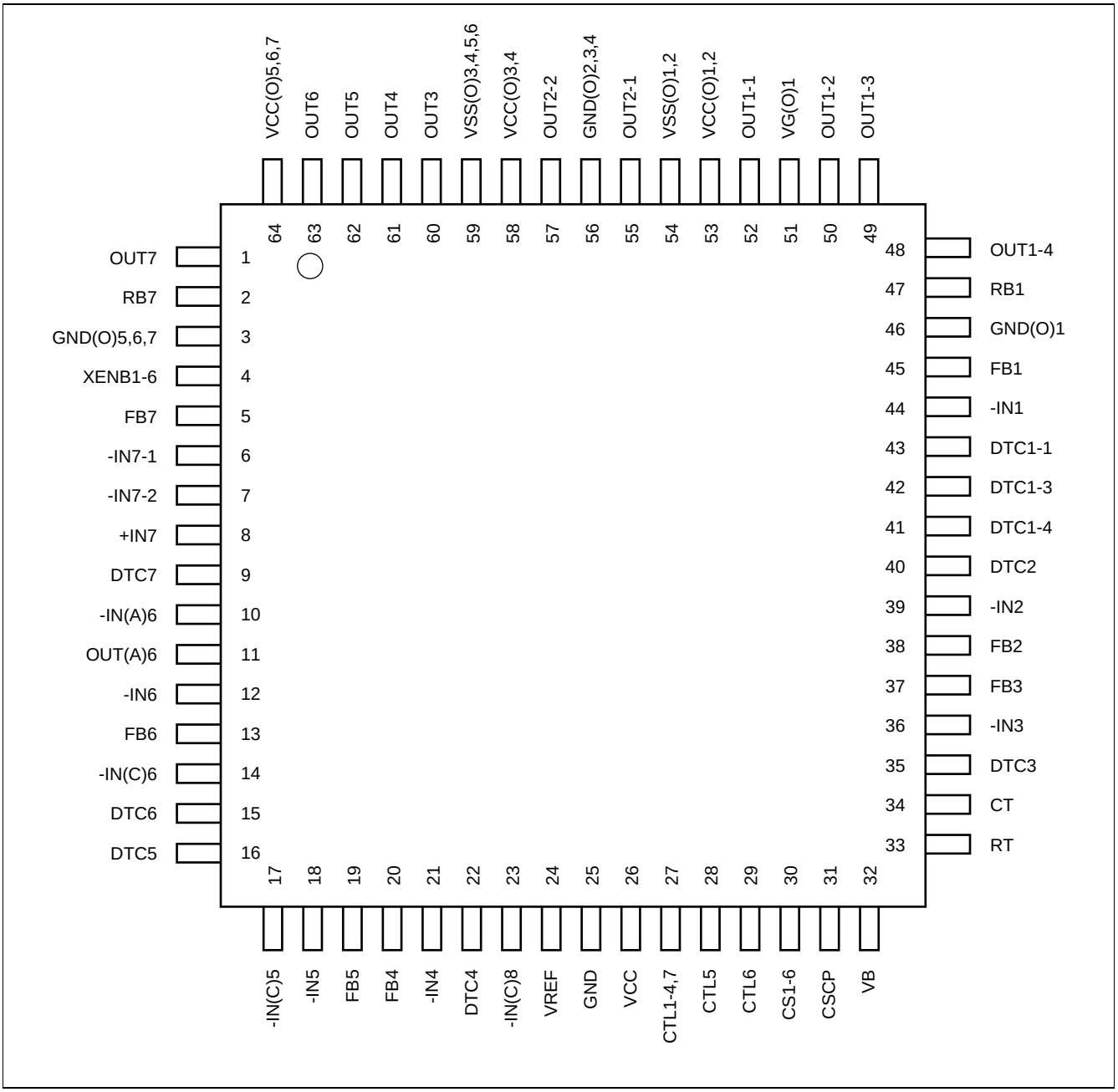
■ PACKAGE

64-pin plastic LQFP



(FPT-64P-M03)

■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin No.		Symbol	I/O	Descriptions
CH 1	45	FB1	O	Channel 1 error amplifier output pin.
	44	–IN1	I	Channel 1 error amplifier inverted input pin.
	43	DTC1-1	I	Channel 1 step-down main side dead time control pin.
	42	DTC1-3	I	Channel 1 step-up main side dead time control pin.
	41	DTC1-4	I	Channel 1 step-up synchronous rectifier side dead time control pin.
	52	OUT1-1	O	Channel 1 step-down main side output pin.
	50	OUT1-2	O	Channel 1 step-down synchronous rectifier side output pin.
	47	RB1	—	Channel 1 step-up main side output current setting pin.
	49	OUT1-3	O	Channel 1 step-up main side output pin.
	48	OUT1-4	O	Channel 1 step-up synchronous rectifier side output pin.
CH 2	38	FB2	O	Channel 2 error amplifier output pin.
	39	–IN2	I	Channel 2 error amplifier inverted input pin.
	40	DTC2	I	Channel 2 dead time control pin.
	55	OUT2-1	O	Channel 2 main side output pin.
	57	OUT2-2	O	Channel 2 synchronous rectifier side output pin.
CH 3	37	FB3	O	Channel 3 error amplifier output pin.
	36	–IN3	I	Channel 3 error amplifier inverted input pin.
	35	DTC3	I	Channel 3 dead time control pin.
	60	OUT3	O	Channel 3 output pin.
CH 4	20	FB4	O	Channel 4 error amplifier output pin.
	21	–IN4	I	Channel 4 error amplifier inverted input pin.
	22	DTC4	I	Channel 4 dead time control pin.
	61	OUT4	O	Channel 4 output pin.
CH 5	19	FB5	O	Channel 5 error amplifier output pin.
	18	–IN5	I	Channel 5 error amplifier inverted input pin.
	17	–IN(C)5	I	Channel 5 short detection comparator input pin.
	16	DTC5	I	Channel 5 dead time control pin.
	62	OUT5	O	Channel 5 output pin.

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Pin No.		Symbol	I/O	Descriptions
CH 6	10	–IN(A)6	I	Channel 6 inverted amplifier input pin.
	11	OUT(A)6	O	Channel 6 inverted amplifier output pin.
	13	FB6	O	Channel 6 error amplifier output pin.
	12	–IN6	I	Channel 6 error amplifier inverted input pin.
	14	–IN4(C)6	I	Channel 6 short detection comparator input pin.
	15	DTC6	I	Channel 6 dead time control pin.
	63	OUT6	O	Channel 6 output pin.
CH 7 (for self power supply)	5	FB7	O	Channel 7 error amplifier output pin.
	6	–IN7-1	I	Channel 7 error amplifier 1 inverted input pin.
	8	+IN7	I	Channel 7 error amplifier non-inverted input pin.
	7	–IN7-2	I	Channel 7 error amplifier 2 inverted input pin.
	9	DTC7	I	Channel 7 dead time control pin.
	1	OUT7	O	Channel 7 output pin.
	2	RB7	—	Channel 7 output current setting pin.
Triangular-Wave Oscillator Circuit	33	RT	—	Triangular wave frequency setting resistor connection pin.
	34	CT	—	Triangular wave frequency setting capacitor connection pin.
Control Circuit	27	CTL1-4, 7	I	Power supply control circuit pin.(channel 1 to 4 and 7) “H” level: Power supply active mode “L” level: Standby mode
	28	CTL5	I	Channel 5 control circuit pin. When CTL1-4,7 pins = “H” level “H” level: Channel 5 in active mode “L” level: Channel 5 in standby mode
	29	CTL6	I	Channel 6 control circuit pin. When CTL1-4,7 pins = “H” level “H” level: Channel 6 in active mode “L” level: Channel 6 in standby mode
	23	–IN(C)8	I	Short detection comparator input pin.
	31	CSCP	—	Short protection circuit capacitor connection pin.
	30	CS1-6	—	Soft start circuit capacitor connection pin (channel 1 to 6).
	4	XENB1-6	I	VREF control pin (channel 1 to 6 output control pin). When CTL1-4, 7 pin = “H” “H” level: VREF “L” level, channel 1 to 6 output “OFF” “L” level: VREF “H” level, channel 1 to 6 output “active”

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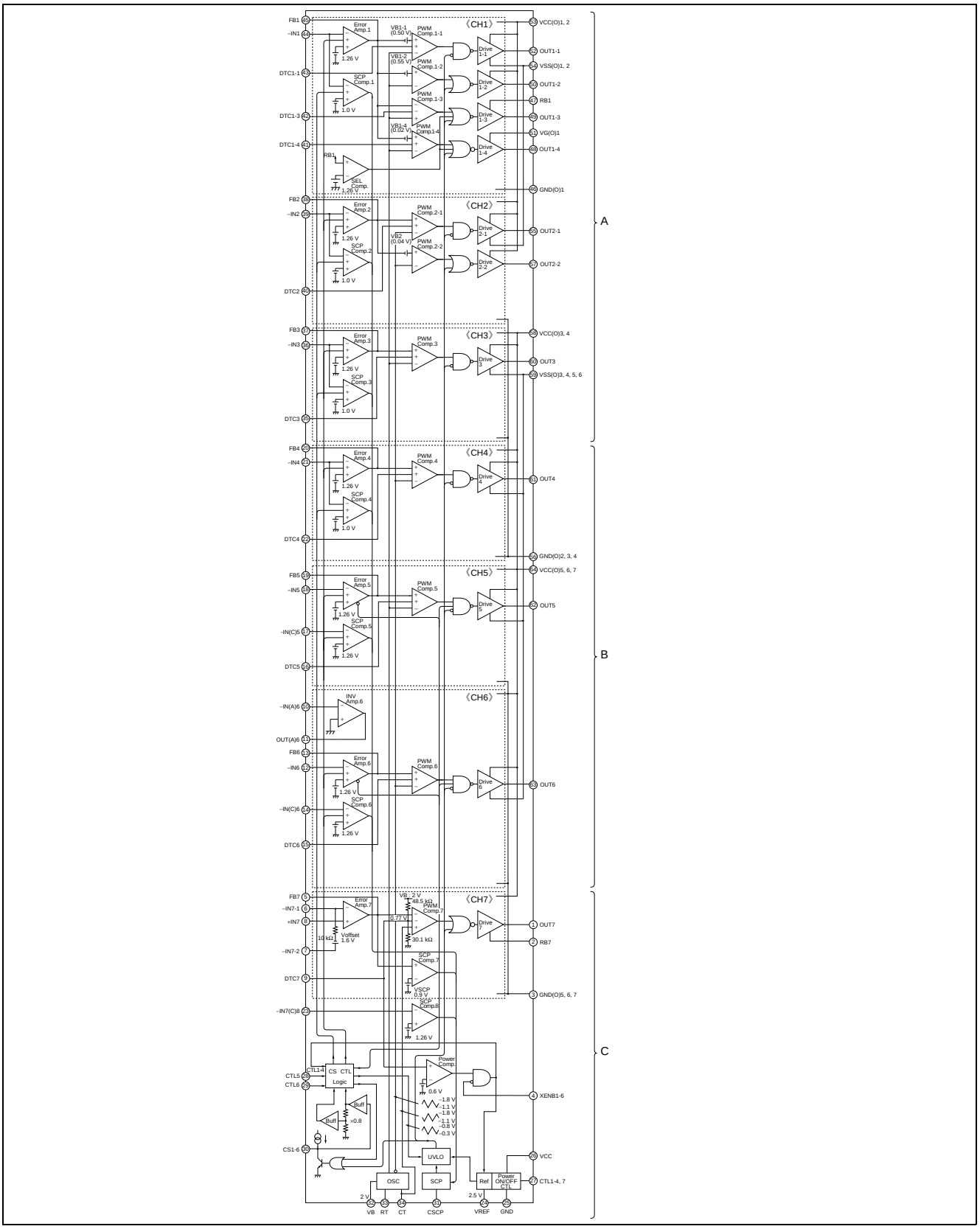
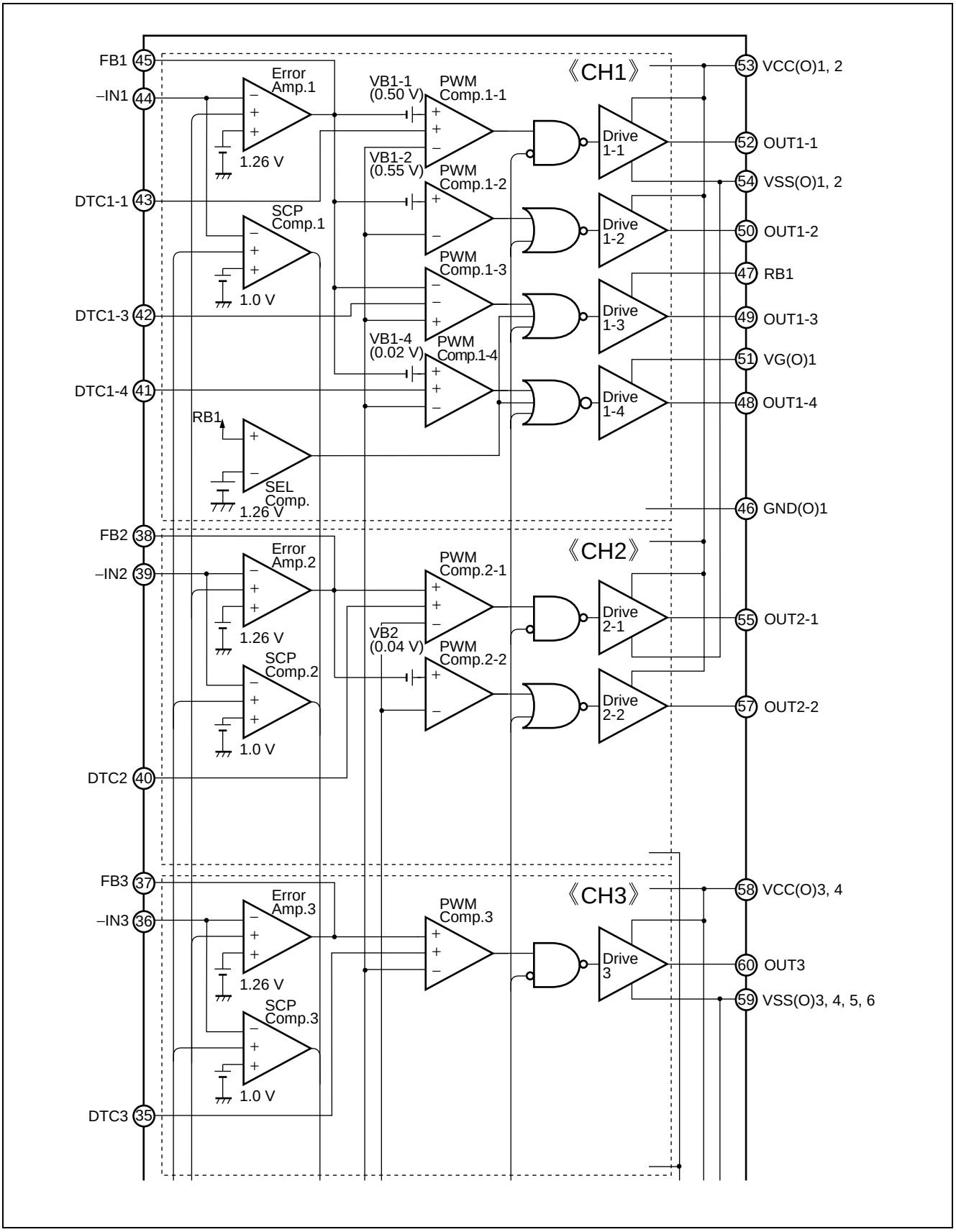
Pin No.		Symbol	I/O	Description
Power Supply Circuit	26	VCC	—	Reference voltage and control circuit power supply pin.
	53	VCC(O)1,2	—	Output circuit power supply pin (Channel 1, 2).
	58	VCC(O)3,4	—	Output circuit power supply pin (Channel 3, 4).
	64	VCC(O)5,6,7	—	Output circuit power supply pin (Channel 5, 6, 7).
	54	VSS(O)1,2	—	Main side output circuit power supply pin (Channel 1, 2).
	51	VG(O)1	—	Step-up synchronous rectifier side output circuit power supply pin (Channel 1).
	59	VSS(O)3,4,5,6	—	Output circuit power supply pin (Channel 3, 4, 5, 6).
	24	VREF	O	Reference voltage output pin.
	32	VB	O	Triangular wave oscillator regulator output pin.
	25	GND	—	Ground pin.
	46	GND(O)1	—	Output circuit ground pin (Channel 1).
	56	GND(O)2,3,4	—	Output circuit ground pin (Channel 2, 3, 4).
	3	GND(O)5,6,7	—	Output circuit ground pin (Channel 5, 6, 7).

■ BLOCK DIAGRAM

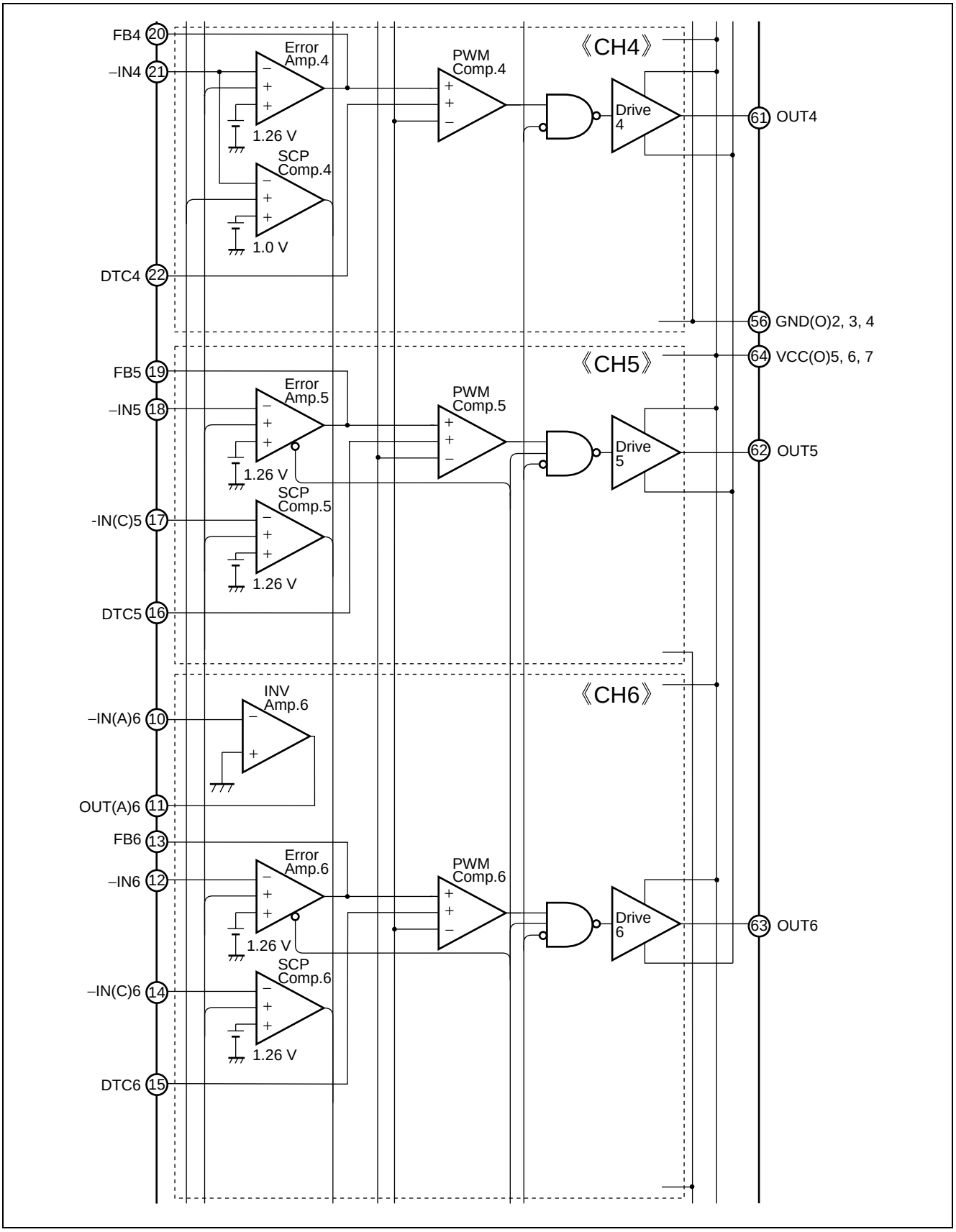
- **General view**



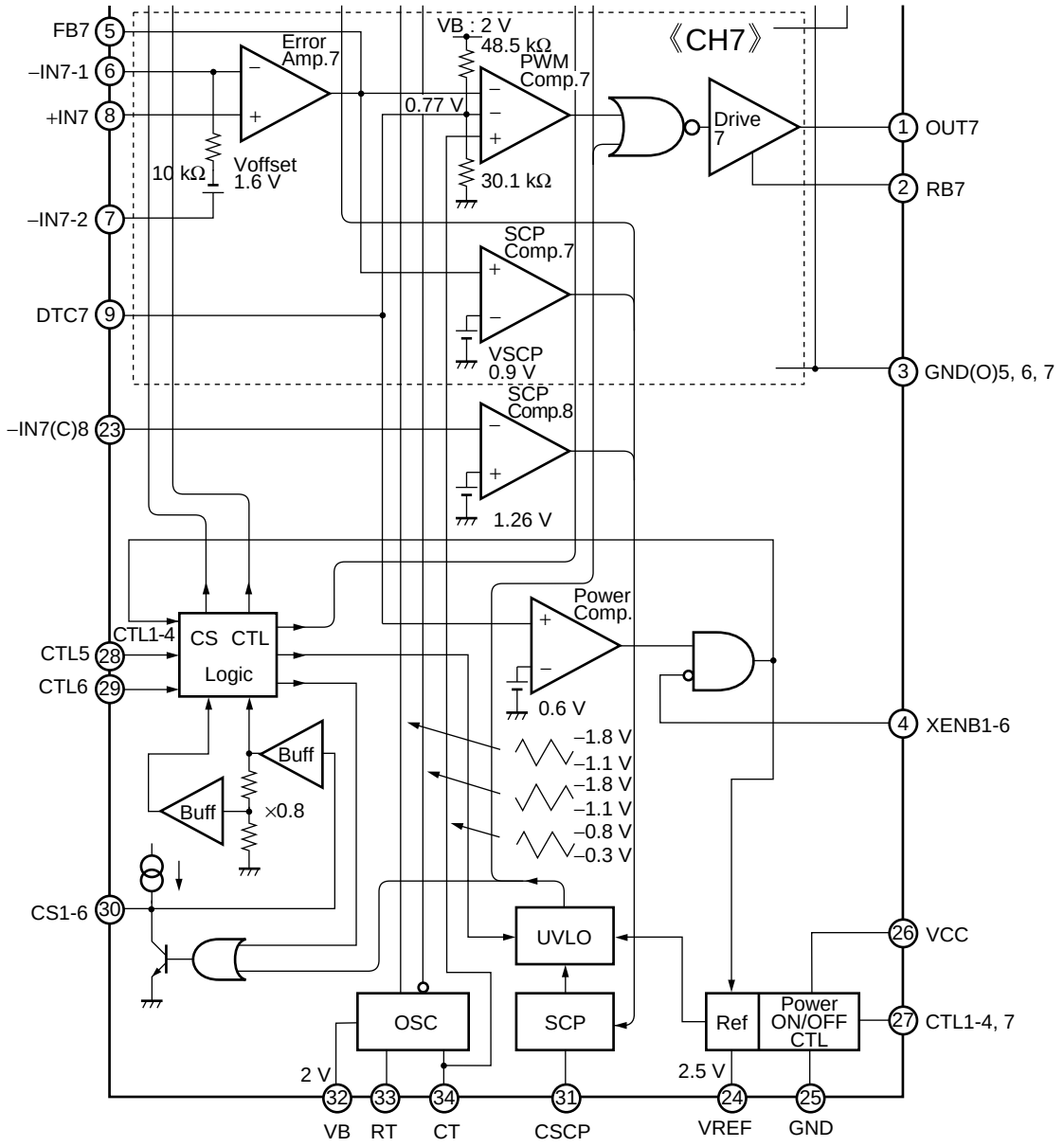
- **Enlarged view of A**



- **Enlarged view of B**



- **Enlarged view of C**



■ ABSOLUTE MAXIMUM RAGINGS

Parameter	Symbol	Conditions	Rating		Unit
			Min.	Max.	
Power supply voltage	V_{CC}	—	—	17	V
	V_G	—	—	17	V
Output current	Io	OUT pin	—	20	mA
Peak output current	Io	OUT pin, Duty ≤ 5%	—	200	mA
Power dissipation	P_D	Ta ≤ +25°C	—	1000*	mW
Storage temperature	Tstg	—	–55	+125	°C

* : The packages are mounted on the dual-sided epoxy board (10 cm × 10 cm).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Power supply voltage	V_{CC}	Channel 7	1.8	9	13	V
		Channel 1 to 6	4	9	13	V
Reference voltage output current	I_{OR}	—	–1	—	0	mA
Input voltage	V_{IN}	+IN,–IN,–IN(C) pin	0	—	V_{CC} – 1.8	V
Control input voltage	V_{CTL}	CTL pin	0	—	13	V
Output current	I_O	OUT pin	1	2	15	mA
Output current setting resistor	R_B	RB pin	2.2	24	51	kΩ
Triangular wave oscillator frequency	f_{OSC}	—	100	500	800	kHz
Timing capacitor	C_T	—	47	100	1000	pF
Timing resistor	R_T	—	13	18	47	kΩ
Soft-start capacitor	C_S	—	—	0.1	1.0	µF
	C_{DTC}	DTC7 pin	—	1	10	µF
Short detection capacitor	C_{SCP}	—	—	0.1	1.0	µF
Operating ambient temperature	Ta	—	–30	+25	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(Ta = +25°C, V_{CC} = 9 V, V_{SS} = 4.4 V, V_G = 11 V)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
Reference voltage block (Ref)	Output voltage	V_{REF}	24	—	2.475	2.5	2.525	V
	Output voltage temperature stability	$\Delta V_{REF}/V_{REF}$	24	Ta = –30°C to +85°C	—	0.5*	—	%
	Input stability	Line	24	V_{CC} = 4 V to 13 V	–10	—	10	mV
	Load stability	Load	24	VREF = 0 mA to –1 mA	–10	—	10	mV
	Short-circuit output current	I_{OS}	24	VREF = 2 V	–20	–5	–1	mA
Under voltage lockout protection circuit block (CH1 to 6) (UVLO)	Threshold voltage	V_{TH}	52	V_{CC} = ⌐	2.6	2.8	3.0	V
	Hysteresis width	V_H	52	—	—	0.2	—	V
	Reset voltage	V_{RST}	52	—	1.35	1.50	1.65	V
Under voltage lockout protection circuit block (CH7) (UVLO)	Threshold voltage	V_{TH}	1	V_{CC} = ⌐	1.3	1.5	1.7	V
Soft-start block (CS)	Input standby voltage	V_{STB}	30	—	—	50	100	mV
	Charge current	I_{CS}	30	—	–1.4	–1.0	–0.6	µA
Short circuit detection block (SCP)	Threshold voltage	V_{TH}	31	—	0.63	0.68	0.73	V
	Input standby voltage	V_{STB}	31	—	—	50	100	mV
	Input latch voltage	V_I	31	—	—	50	100	mV
	Input source current	I_{CSCP}	31	—	–1.4	–1.0	–0.6	µA
Triangular waveform oscillator block (OSC)	Oscillator frequency	f_{OSC}	52,50,49,48, 55,57,60,61, 62,63	C_T = 100 pF, R_T = 18 kΩ	450	500	550	kHz
	Frequency voltage stability	$\Delta f/f_{dV}$	52,50,49,48, 55,57,60,61, 62,63	V_{CC} = 4 V to 13 V	—	1	10	%
	Frequency temperature stability	$\Delta f/f_{dT}$	52,50,49,48, 55,57,60,61, 62,63	Ta = –30°C to +85°C	—	1*	—	%

*: Standard design value.

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(Ta = +25°C, V_{CC} = 9 V, V_{SS} = 4.4 V, V_G = 11 V)

Parameter		Symbol	Pin No	Conditions	Value			Unit
					Min.	Typ.	Max.	
Error amplifier block (CH1 to CH6)	Threshold voltage	V_{TH}	45,38,37, 20,19,13	FB = 1.0 V	1.45	1.50	1.55	V
	V_T temperature stability	$\Delta V_T / V_T$	45,38,37, 20,19,13	Ta = –30°C to +85°C	—	0.5*	—	%
	Input bias current	I_B	45,39,36,21	–IN = 0 V (CH1 to 4)	–320	–80	—	nA
			18,12	–IN = 0 V (CH5,6)	–120	–30	—	nA
	Voltage gain	A_V	45,38,37, 20,19,13	DC	60	100	—	dB
	Frequency bandwidth	B_W	45,38,37, 20,19,13	A_V = 0 dB	—	1.0*	—	MHz
	Output voltage	V_{OH}	45,38,37, 20,19,13	—	2.2	2.4	—	V
		V_{OL}	45,38,37, 20,19,13	—	—	20	200	mV
	Output source current	I_{SOURCE}	45,38,37, 20,19,13	FB = 1.35 V	—	–2.0	–1.0	mA
	Output sink current	I_{SINK}	45,38,37, 20,19,13	FB = 1.35 V (CH1)	50	100	—	µA
				FB = 1.35 V (CH2)	65	130	—	µA
				FB = 1.35 V(CH3 to 6)	75	150	—	µA
Error amplifier block (CH7)	Input offset voltage	V_{IO}	6	–IN2 = 0V,FB = 0.55V	—	—	20	mV
			7	+IN = 0 V	1.45	1.55	1.65	V
	V_T temperature stability	$\Delta V_T / V_T$	5	Ta = –30°C to +85°C	—	0.5*	—	%
	Input bias current	I_B	7	–IN2 = V_{CC}	—	15	30	µA
			8	+IN = 0 V	–100	–20	—	nA
	Common mode input voltage rage	V_{CM}	5	—	0	—	V_{CC}–0.9	V
	Voltage gain	A_V	5	DC	60	75	—	dB
	Frequency bandwidth	BW	5	A_V = 0 dB	—	1.0*	—	MHz
	Output voltage	V_{OH}	5	—	1.1	1.3	—	V
		V_{OL}	5	—	—	20	200	mV
	Output source current	I_{SOURCE}	5	FB = 0.55 V	—	–2.0	–1.0	mA
	Output sink current	I_{SINK}	5	FB = 0.55 V	65	130	—	µA

*: Standard design value.

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(Ta = +25°C, V_{CC} = 9 V, V_{SS} = 4.4 V, V_G = 11 V)

Parameter		Sym-bol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
Inverse amplifier block (CH6) (INV Amp.)	Threshold voltage	V_{TH}	11	—	–10	0	10	mV
	Input bias current	I_B	10	–IN = –0.1 V	–120	–30	—	nA
	Voltage gain	A_V	11	DC	60	100	—	dB
	Frequency bandwidth	BW	11	A_V = 0 dB	—	1.0*	—	MHz
	Output voltage	V_{OH}	11	—	2.2	2.4	—	V
		V_{OL}	11	—	—	20	100	mV
	Output source current	I_{SOURCE}	11	OUT = 1.26 V	—	–2.0	–1.0	mA
	Output sink current	I_{SINK}	11	OUT = 1.26 V	75	150	—	µA
Short detection comparator block (CH1-4) (SCP Comp.)	Threshold voltage	V_{TH}	52,50,49, 48,55,57, 60,61	—	0.97	1.00	1.03	V
	Input bias current	I_B	44,39,36, 21	–IN = 0 V	–320	–80	—	nA
Short detection comparator block (CH5,6)(SCP Comp.)	Input offset voltage	V_{IO}	62,63	—	1.22	1.26	1.30	V
	Input bias current	I_B	17,14,23	–IN(C) = 0 V	–200	–50	—	nA
Short detection comparator block (CH7)(SCP Comp.)	Threshold voltage	V_{TH}	1	—	0.8	0.9	1.0	V
PWM comparator block (CH1) (PWM Comp.-1)	Threshold voltage	V_{T0}	52	Duty cycle = 0 %	0.5	0.6	—	V
		V_{T100}	52	Duty cycle = 100 %	—	1.3	1.4	V

*: Standard design value.

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(Ta = +25°C, V_{CC} = 9 V, V_{SS} = 4.4 V, V_G = 11 V)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
PWM comparator block (CH1) (PWM Comp.-2)	Threshold voltage	V_{T100}	50	Duty cycle = 100 %	0.450	0.550	—	V
		V_{T0}	50	Duty cycle = 0 %	—	1.250	1.350	V
PWM comparator block (CH1) (PWM Comp.-3)	Threshold voltage	V_{T0}	49	Duty cycle = 0 %	1.0	1.1	—	V
		V_{T100}	49	Duty cycle = 100 %	—	1.8	1.9	V
PWM comparator block (CH1) (PWM Comp.-4)	Threshold voltage	V_{T100}	48	Duty cycle = 100 %	0.980	1.080	—	V
		V_{T0}	48	Duty cycle = 0 %	—	1.780	1.880	V
PWM comparator block (CH2) (PWM Comp.-1)	Threshold voltage	V_{T0}	55	Duty cycle = 0 %	1.0	1.1	—	V
		V_{T100}	55	Duty cycle = 100 %	—	1.8	1.9	V
PWM comparator block (CH2) (PWM Comp.-2)	Threshold voltage	V_{T100}	57	Duty cycle = 100 %	0.960	1.060	—	V
		V_{T0}	57	Duty cycle = 0 %	—	1.760	1.860	V
PWM comparator block (CH3 to 6) (PWM Comp.)	Threshold voltage	V_{T0}	60,61,62, 63	Duty cycle = 0 %	1.0	1.1	—	V
		V_{T100}	60,61,62, 63	Duty cycle = 100 %	—	1.8	1.9	V

*: Standard design value.

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(Ta = +25°C, V_{CC} = 9 V, V_{SS} = 4.4 V, V_G = 11 V)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
PWM comparator block (CH7) (PWM Comp.)	Threshold voltage	V_{T0}	1	Duty cycle = 0 %	0.2	0.3	—	V
		V_{Tmax}	1	—	—	0.77	0.87	V
	Maximum duty cycle	Dtr	1	C_T=100pF,R_T=18kΩ, R_B=24kΩ,R_L=390kΩ	70	80	90	%
Dead time control block (CH1-6) (PWM Comp.)	Threshold voltage	V_{TD0}	52,49,48,55, 60,61,62,63	Duty cycle = 0 %	1.0	1.1	—	V
		V_{TD100}	52,49,48,55, 60,61,62,63	Duty cycle = 100 %	—	1.8	1.9	V
	Input current	I_{DTC}	43,42,41,40, 35,22,16,15	DTC = 0.4 V	–1.0	–0.3	—	µA
Dead time control block (CH7) (PWM Comp.)	Threshold voltage	V_{TD0}	1	Duty cycle = 0 %	0.2	0.3	—	V
		V_{TD100}	1	Duty cycle = 100 %	—	0.8	0.9	V
Output block (CH1-6) (Drive-1)	Output source current	I_{SOURCE}	52,55,60, 61,62,63	Duty ≤ 5 %, OUT= 4.4V	—	–90	—	mA
	Output sink current	I_{SINK}	52,55,60, 61,62,63	Duty ≤ 5 %, OUT= 9V	—	80	—	mA
	Output voltage	V_{OH}	52,55,60, 61,62,63	I_O = –15 mA	3.5	4.0	—	V
		V_{OL}	52,55,60, 61,62,63	I_O = 15 mA	—	100	300	mV
Output block (CH1,2) (Drive-2)	Output source current	I_{SOURCE}	50,57	Duty ≤ 5 %, OUT= 0V	—	–100	—	mA
	Output sink current	I_{SINK}	50,57	Duty ≤ 5 %, OUT= 4V	—	80	—	mA
	Output voltage	V_{OH}	50,57	I_O = –15 mA	3.5	4.0	—	V
		V_{OL}	50,57	I_O = 15 mA	—	100	300	mV
Output block (CH1) (Drive-3)	Output source current	I_{SOURCE}	49	R_B= 24kΩ, OUT= 0.7V	–2.6	–2.0	–1.4	mA
	Output sink current	I_{SINK}	49	Duty ≤ 5 %, OUT= 0.7V	—	40	—	mA

*: Standard design value.

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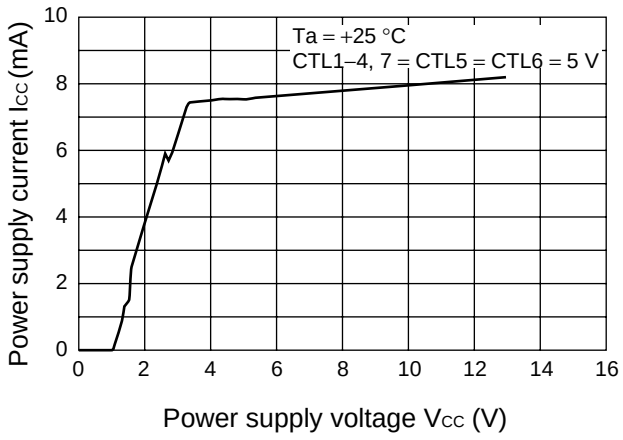
(Ta = +25°C, V_{CC} = 9 V, V_{SS} = 4.4 V, V_G = 11 V)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
Output block (CH1) (Drive-4)	Output source current	I_{SOURCE}	48	Duty ≤ 5 %, OUT= 5V	—	–100	—	mA
	Output sink current	I_{SINK}	48	Duty ≤ 5 %, OUT= 2V	—	120	—	mA
	Output voltage	V_{OH}	48	I_O = –15 mA	9.7	10	—	V
		V_{OL}	48	I_O = 15 mA	—	1.0	1.3	V
Output block (CH7) (Drive)	Output source current	I_{SOURCE}	1	R_B= 24kΩ, OUT= 0.7V	–2.6	–2.0	–1.4	mA
	Output sink current	I_{SINK}	1	Duty ≤ 5 %, OUT= 0.7V	—	40	—	mA
Control block (CTL1 to 4,7,XENB1 to 6) (CTL,XENB)	CTL input condition	V_{IH}	27,4	Active mode	1.5	—	13	V
		V_{IL}	27,4	Standby mode	0	—	0.5	V
	Input current	I_{CTL}	27,4	CTL=5V, XENB=5V	—	100	200	µA
Control block (CTL5,6) (CTL)	CTL input condition	V_{IH}	28,9	Active mode	2.1	—	13	V
		V_{IL}	28,9	Standby mode	0	—	0.7	V
	Input current	I_{CTL}	28,9	CTL= 5V	—	50	100	µA
General	Standby current	I_{CCS}	26	CTL1-4,7= 0V	—	—	10	µA
		$I_{CCS(O)}$	53,58,64	CTL1-4,7= 0V	—	—	10	µA
		I_G	51	CTL1-4,7= 0V	—	—	10	µA
	Power supply current	I_{CC}	26,53,58, 64	CTL1-4,7= CTL5 =CTL6=5V	—	8	12	mA

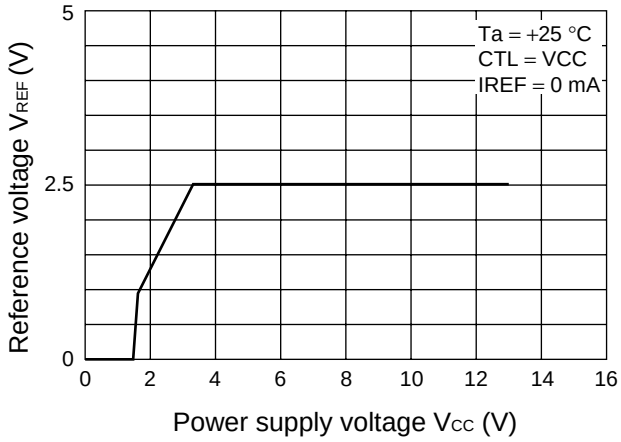
* Standard design value.

■ TYPICAL CHARACTERISTICS

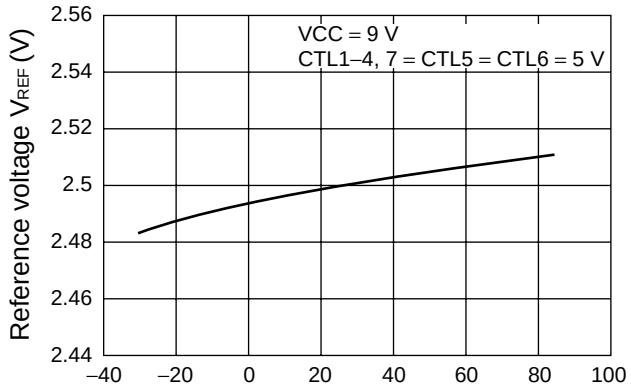
Power supply current vs. power supply voltage



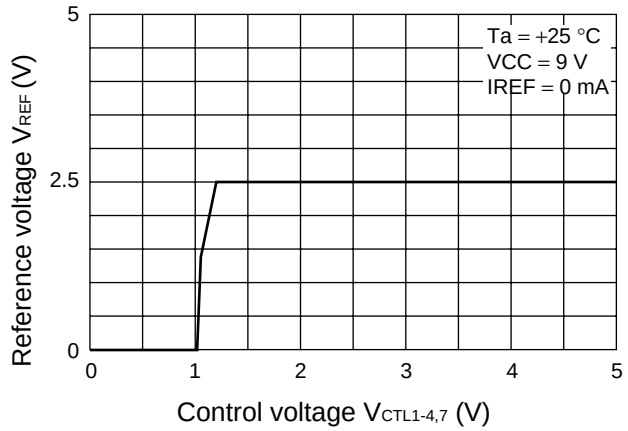
Reference voltage vs. power supply voltage



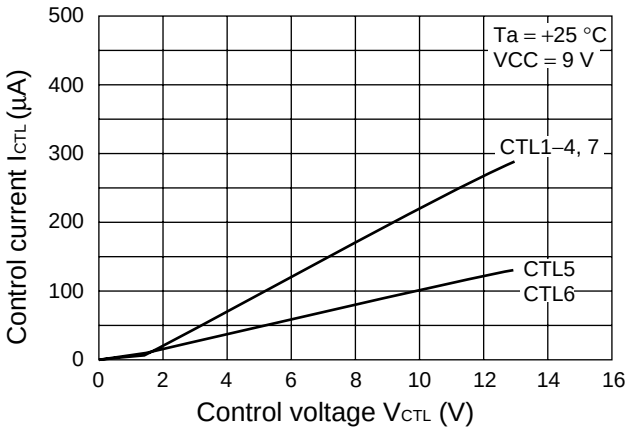
Reference voltage vs. ambient temperature



Reference voltage vs. control voltage



Control current vs. control voltage



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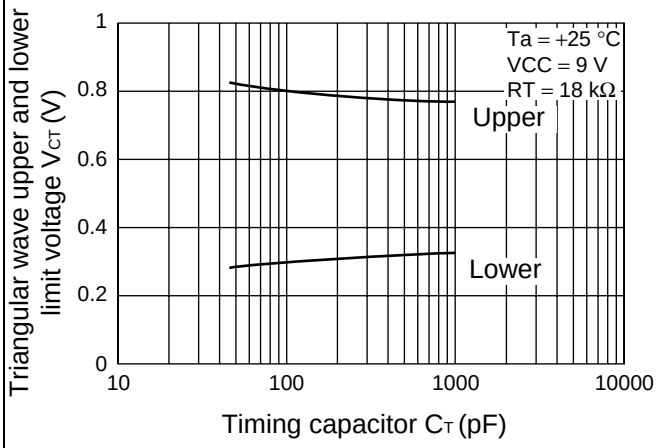
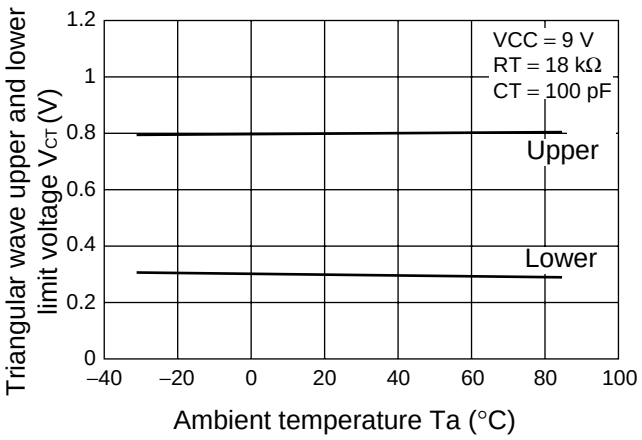
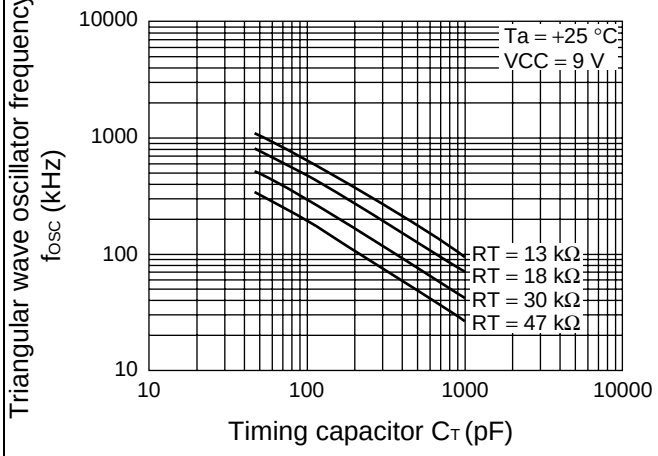
Triangular wave upper and lower limit voltage vs. timing capacitor



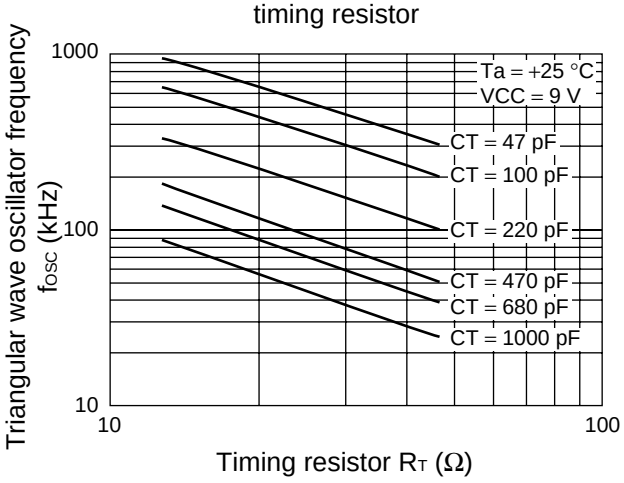
Triangular wave upper and lower limit voltage vs. ambient temperature



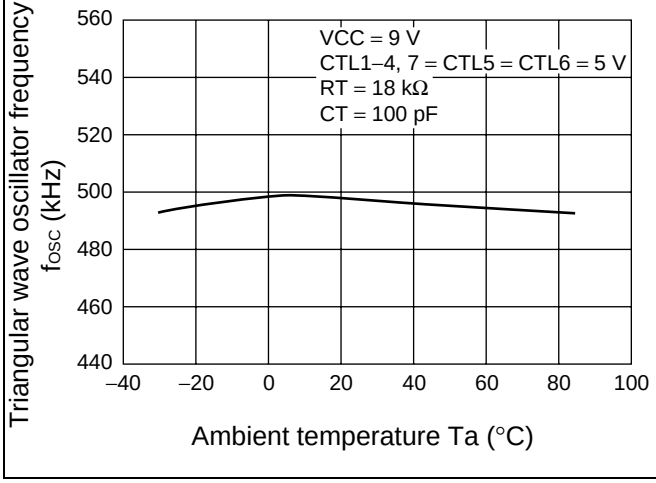
Triangular wave oscillator frequency vs. timing capacitor



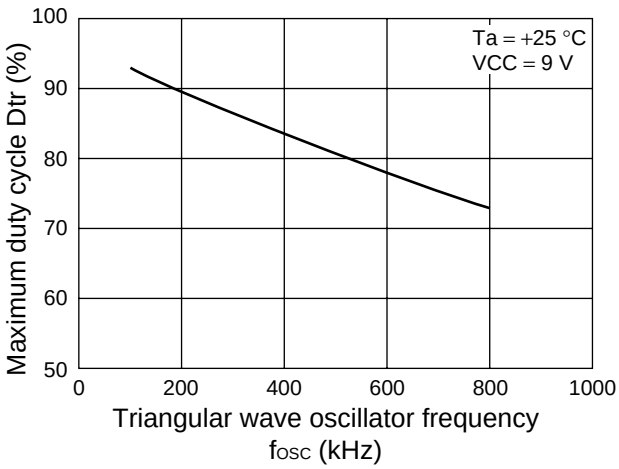
Triangular wave oscillator frequency vs. timing resistor



Triangular wave oscillator frequency vs. ambient temperature



Maximum duty cycle vs. triangular wave oscillator frequency (CH7)



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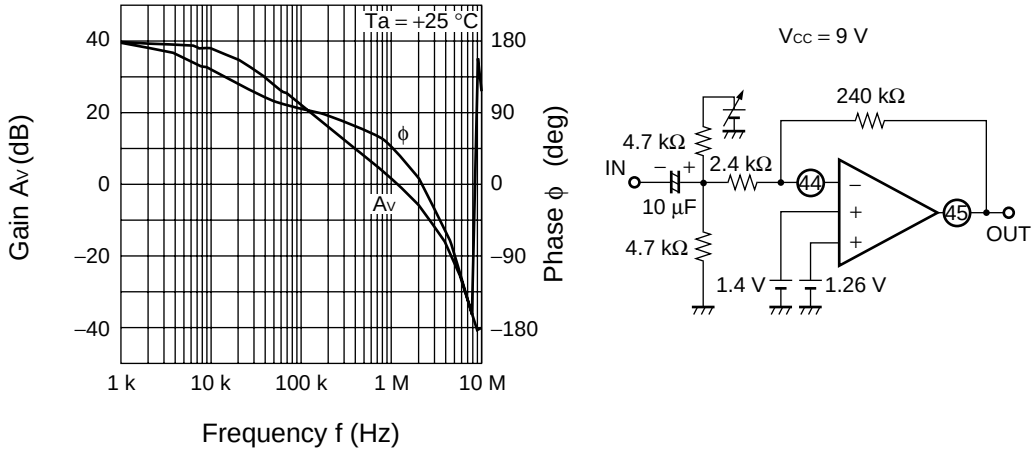
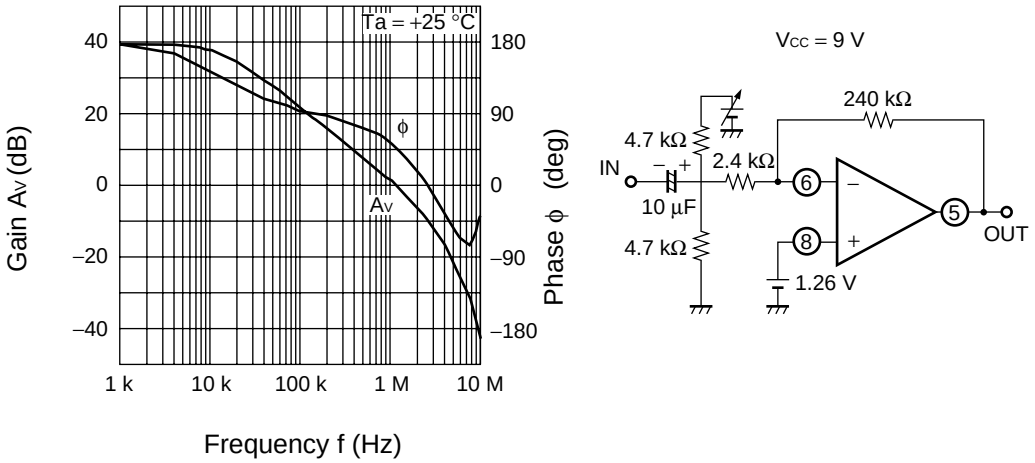
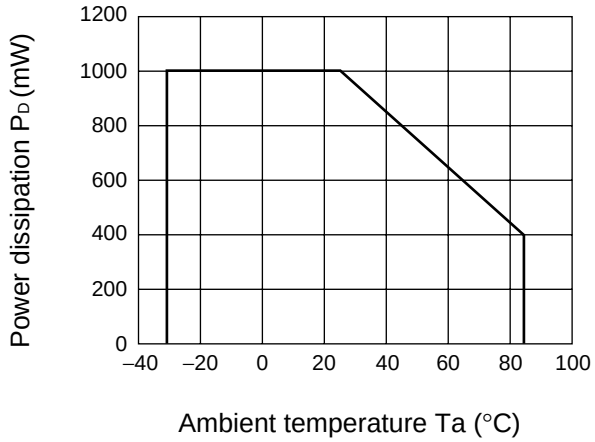
Error amplifier gain and phase vs. frequency (CH1)



Error amplifier gain and phase vs. frequency (CH7)



Power dissipation vs. ambient temperature



■ FUNCTIONAL DESCRIPTION

1. Switching Regulator Function

(1) Reference voltage circuit

The reference voltage circuit generates a temperature-compensated reference voltage (≒ 2.50 V) using the voltage supplied from the power supply terminal (pin 26). This voltage is used as the reference voltage for the internal circuits of the IC. The reference voltage of up to 1mA can also be supplied to an external device from the VREF terminal (pin 24).

(2) Triangular-wave oscillator circuit

By connecting a timing capacitor and a resistor to the CT (pin 34) and the RT (pin 33) terminals, it is possible to generate any desired triangular oscillation waveform (CT : amplitude 0.3V to 0.8V, CT1 : amplitude 1.1V to 1.8V in phase with CT, and CT2 : amplitude 1.1V to 1.8V in inverse phase with CT). The triangular wave is input to CT1, CT2 and the PWM comparator within the IC.

(3) Error amplifier (Error Amp.)

The error amp. is an amplifier circuit that detects the output voltage from the switching regulator and produces the PWM control signal. The broad in-phase input voltage range of 0 V to Vcc – 1.8 V (1-6 ch) and 0 V to Vcc – 0.9 V (channel 7) provides easy setting from external power supplies.

Also, it is possible to provide stable phase compensation for a system by setting up any desired level of loop gain, by connecting feedback resistance and a capacitor between the error amp. output pin and the inverse input pin.

(4) Inverter amplifier (Inv. Amp.)

The inverter amplifier detects the output voltage (negative voltage) from the switching regulator, and outputs a control signal to the error amplifier.

(5) PWM comparator (PWM Comp.)

The voltage-pulse width modulator controls the output duty according to the input voltage.

(Channel 1 to 2, main side, and channel 3 to 7)

During the interval that the error amplifier output voltage and DTC are higher than the triangular wave, the output transistor is turned on.

(Channel 1 step-down synchronous rectifier side)

During the interval when the error amplifier output voltage is lower than the triangular wave, the output transistor is turned on.

(Channel 1 step-up synchronous rectifier side)

During the interval when the error amplifier output voltage and DTC3 voltage are lower than the triangular wave, the output transistor is turned on.

(6) Output circuit

The output circuits is comprised of a totem-pole configuration on both the main side and synchronous rectifier side, and can drive an external PNP transistor (main side) or NPN transistor (channel 1 step-up main side, channel 7) or N-ch MOSFET (synchronous rectifier side).

2. Channel Control Function

Channel on and off levels are dependent on the voltage levels of the CTL1-4,7 terminal (pin 27), XENB1-6 terminal (pin 4), CTL5 terminal (pin 28), and CTL6 terminal (pin 29).

Each Channel On/Off Setting Conditions.

Voltage level of CTL pin				Channel on/off setting conditions				
CTL1-4,7	**XENB1-6**	**CTL5**	**CTL6**	**Power**	**CH7**	**CH1 to 4**	**CH5**	**CH6**
L	X	X	X	OFF (standby state)				
H	H	X	X	ON		OFF	ON	OFF
	L	L	L			ON		
			H					ON
		H	L				OFF	OFF
			H					ON

Note: When the RB1 pin is connected to the V_{REF} pin, the OUT1-3 and OUT1-4 pins are held at “L” level.

X : Don’t care.

3. Protective Functions

(1) Timer-latch short protection circuit

The short detection comparator in each channel detects the output voltage level, and when any channel output voltage falls below the short detection voltage, or the –IN(C)8 terminal (pin 23) voltage falls below the reference voltage, the timer circuit starts operating and the capacitor C_{SCP} connected to the CSCP terminal (pin 31) starts charging.

When the capacitor voltage reaches approximately 0.68 V, the output transistor is turned off and the dead time becomes 100%.

When actuated, this protection circuit can be reset by turning on the power supply again.(See “METHOD OF SETTING TIME CONSTANT FOR TIMER-LATCH SHORT PROTECTION CIRCUIT”.)

(2) Under voltage lockout protection circuit

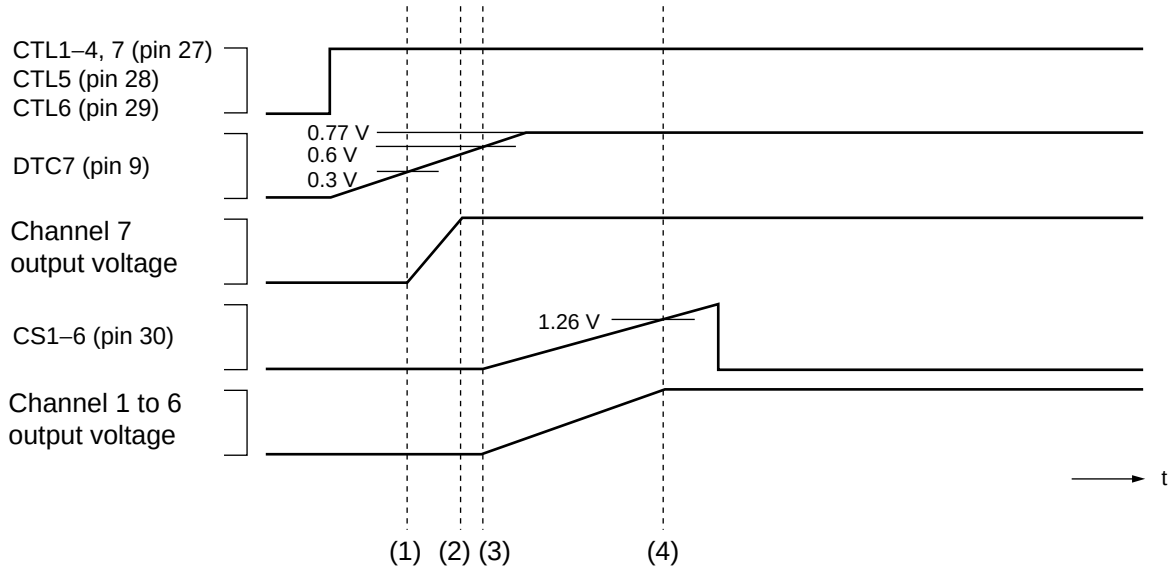
A transient state at power-on or a momentary drop of the power supply voltage causes the control IC to mal-function, resulting in system breakdown or system deterioration. Malfunction like the above-mentioned will be prevented, by detecting the internal reference voltage with respect to the power supply voltage, this protection circuit resets the latch circuit to turn off the output transistor and set the duty (OFF) = 100 %, while at the same time holding the CSCP terminal (pin 31) at the “L”. The reset is cleared when the power supply voltage becomes greater than or equal to the threshold voltage level of this protection circuit.

4. Soft Start Operation

(1) Operating Description

- **Simultaneous “H” level of CTL1-4, 7 terminal, and CTL5 terminal, CTL6 terminal**

When CTL1-4, 7 terminal (pin 27) , and CTL5 terminal (pin 28) , CTL6 terminal (pin 29) are started at the same time, the capacitor (C_{DTC}) connected to DTC7 terminal (pin 9) starts charging. When the DTC7 terminal (pin 9) voltage reaches 0.6V, the capacitors (C_S) connected to the CS1-6 terminal (pin 30) start charging. The error amplifier thus provides the output voltage from channels 1 to 6 with a soft start operation in proportion to the voltage at pin CS1-6.

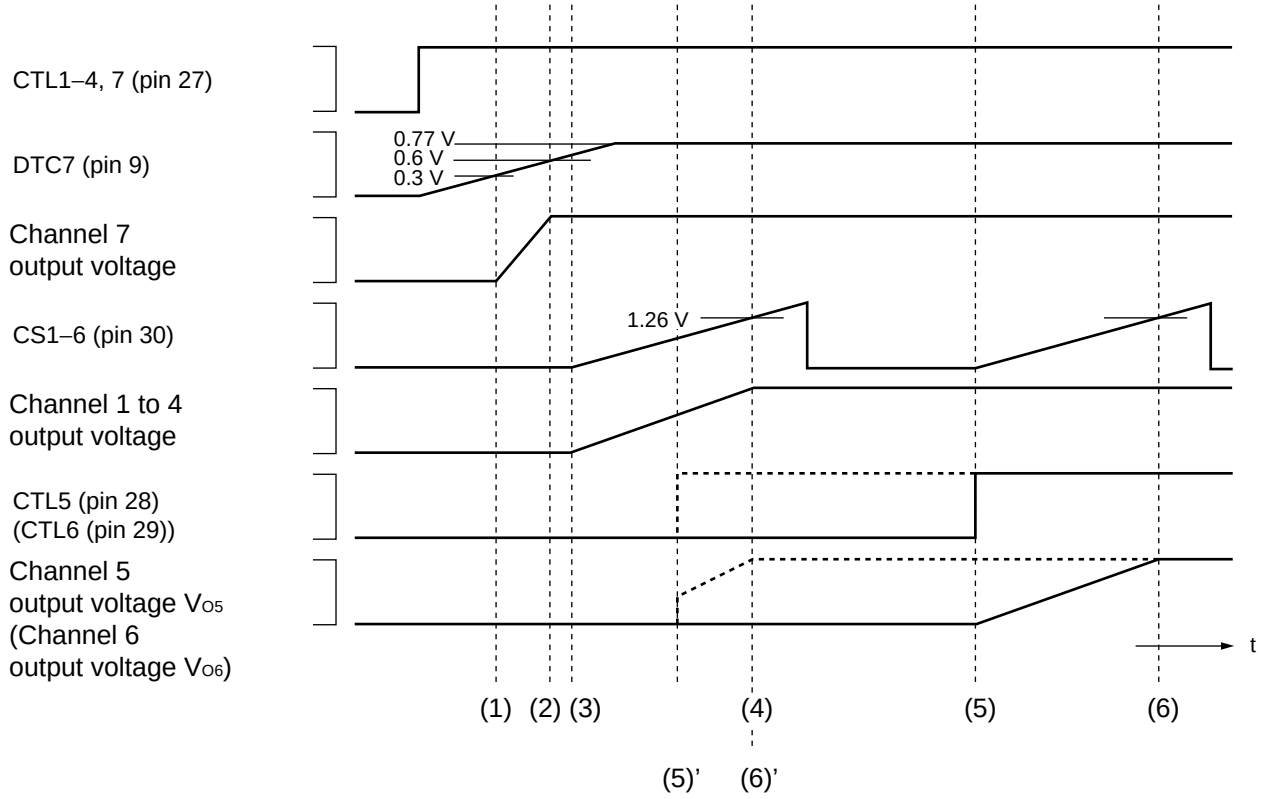


(1) to (2) : Channel 7 soft start interval

(3) to (4) : Channel 1 to 6 soft start interval

- **Starting CTL5 (CTL6) after a soft start on channels 1 to 4 and 7**

When CTL5 (CTL6) is started after a soft start on channels 1-4 and 7, the capacitor (C_S) connected to the CS1-6 terminal (pin 30) start charging. The error amplifier thus provides the output voltage from channel 5 (6) with a soft start operation in comparison with the voltage at pin CS1-6.



(1) to (2) : Channel 7 soft start interval

(3) to (4) : Channel 1 to 4 soft start interval

(5) to (6) : Channel 5 (channel 6) soft start interval

(5)' to (6)': Channel 5 (channel 6) soft start interval (wave form) as CTL5 (CTL6) goes "L" to "H" during a soft start on channels 1-4.

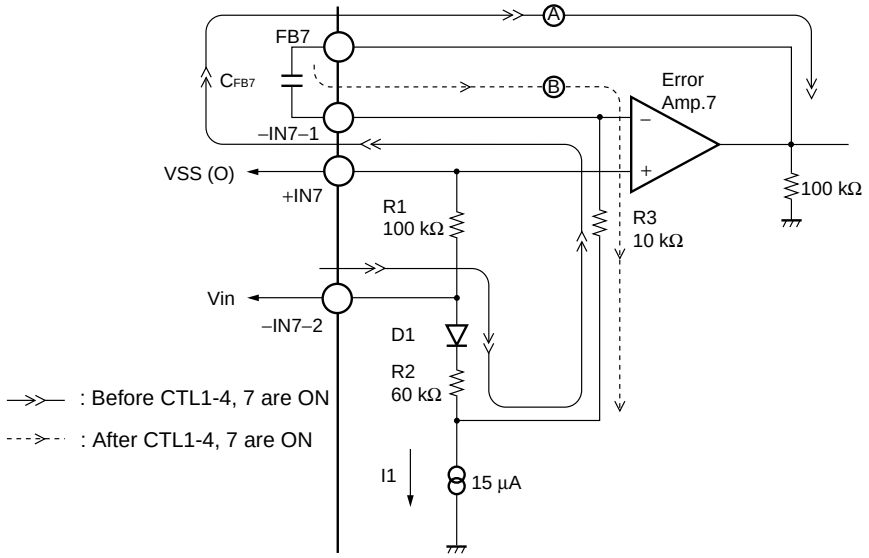
(2) Setting Methods

- **Channel 7 soft start interval**

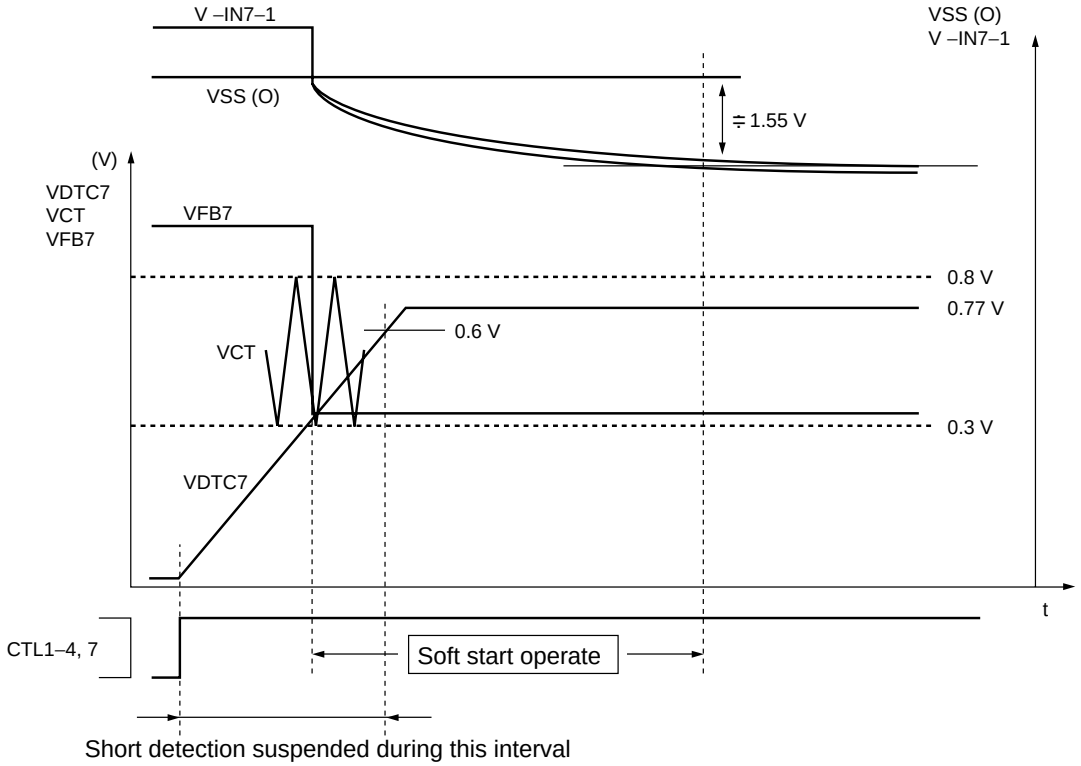
Before CTL1-4, 7 are ON: Vin is applied along path (A) below and charges C_{FB7}.
After CTL1-4, 7 are ON: Along path (B), C_{FB7} is discharged by R2, R3, D1 at I1 to 15 µA on a time constant, and with the fall of V-IN7-1, channel 7 is activated with a soft start.

Note : The short detection function is suspended while VDTC is below 0.6V.

Channel 7 equivalent circuit of soft start section



Channel 7 soft start operating waveform



- **Channel 1 to 6 soft start time**

  $t_S(sec) \fallingdotseq 1.26 \times Cs\ (\mu F)$

Note : The short detection function operates during soft starts on channel 1 to channel 6.

■ METHOD OF SETTING THE OSCILLATOR FREQUENCY SETTING

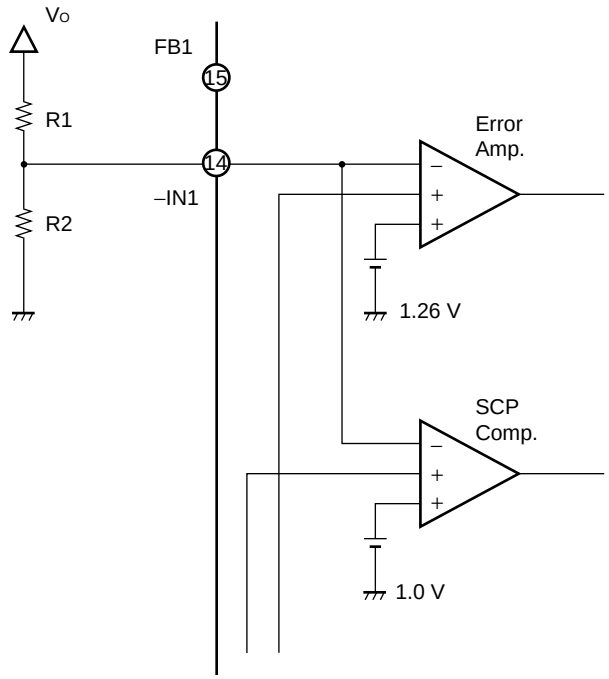
The oscillator frequency can be set by the timing resistor R_T connected to the RT pin (pin 33), and the timing capacitor C_T connected to the CT pin (pin 34).

Oscillator frequency:

$$f_{OSC}\ [kHz] \fallingdotseq \frac{900000}{C_T\ [pF] \times R_T\ [k\Omega]}$$

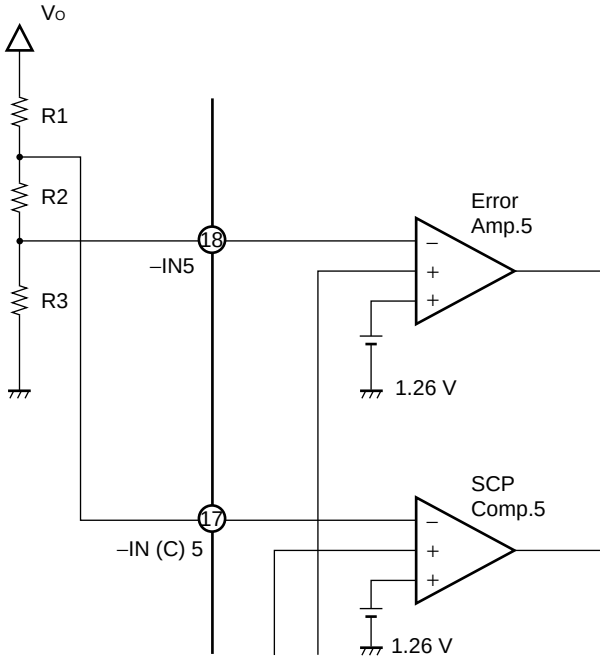
■ METHODS OF SETTING THE OUTPUT VOLTAGE

1. Channel 1 to 4



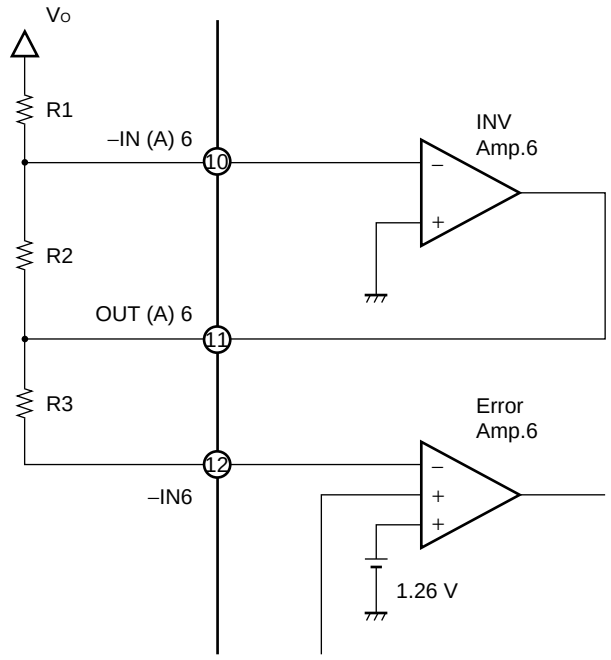
$$V_O = \frac{1.26\ V}{R2}\ (R1 + R2)$$

2. Channel 5



$$V_O = \frac{1.26\ V}{R3}\ (R1 + R2 + R3)$$

3. Channel 6

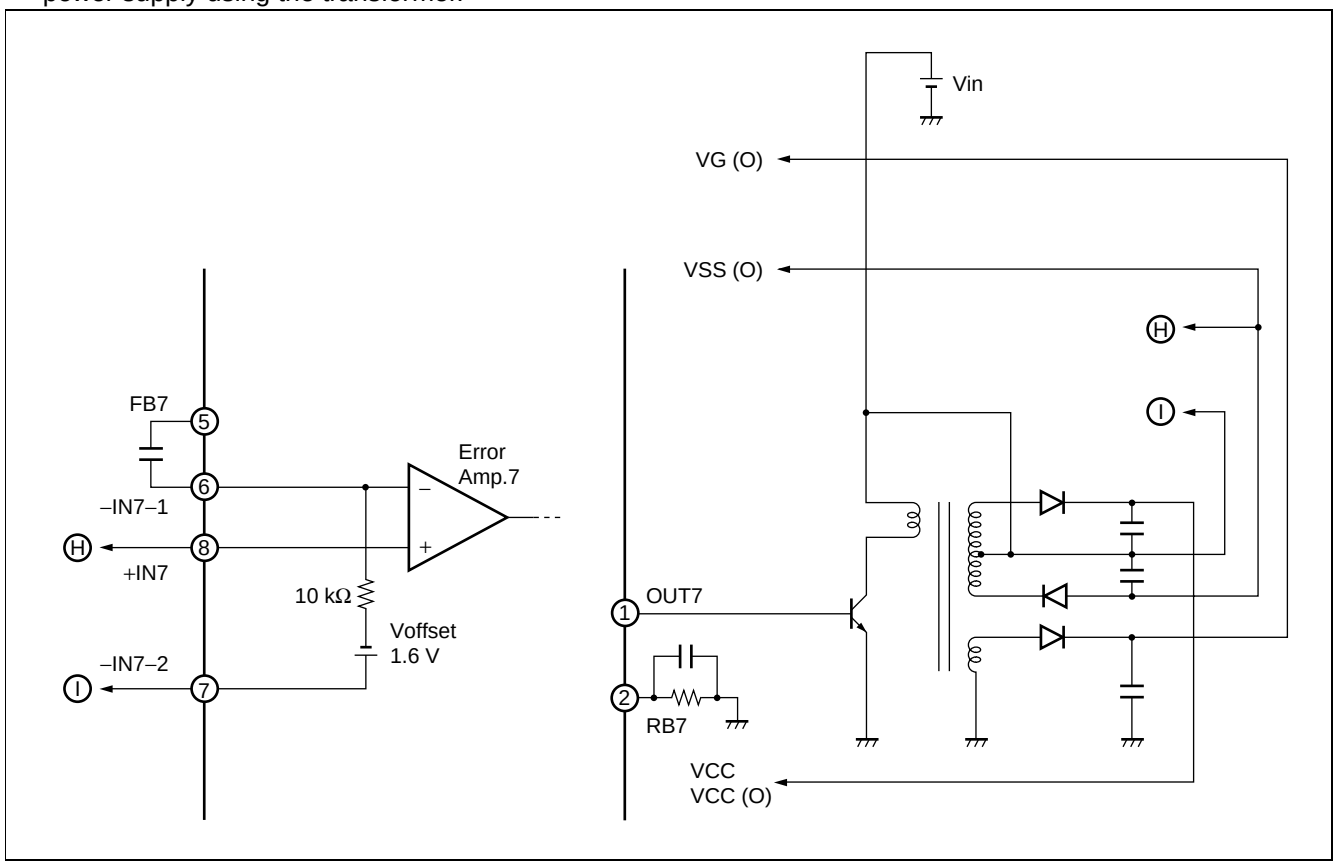


$$V_O = \frac{V_{-IN\,(A)\,6} - V_{OUT\,(A)\,6}}{R2} R1$$

$$\left[V_{OUT\,(A)\,6} = V_{-IN6} \right]$$

■ SAMPLE POWER SUPPLY USING SELF-POWER SUPPLY (Channel 7)

The MB3827 has a built-in self-supply channel (channel 7), capable of supplying the IC with power through transformer winding, with low input voltage ($V_{in} \geq 1.8V$) drive capability. Following figure shows a sample of a power supply using the transformer.



Note: The following settings are shown in “APPLICATION EXAMPLE”.

- VSS(0) is Vin –1.6V, from the voltage offset between –IN7-1 and –IN7-2.
- VCC and VCC(0) are set at the winding that produces Vin +1.6V.
- VG(0) is set at the winding that produces 8V.

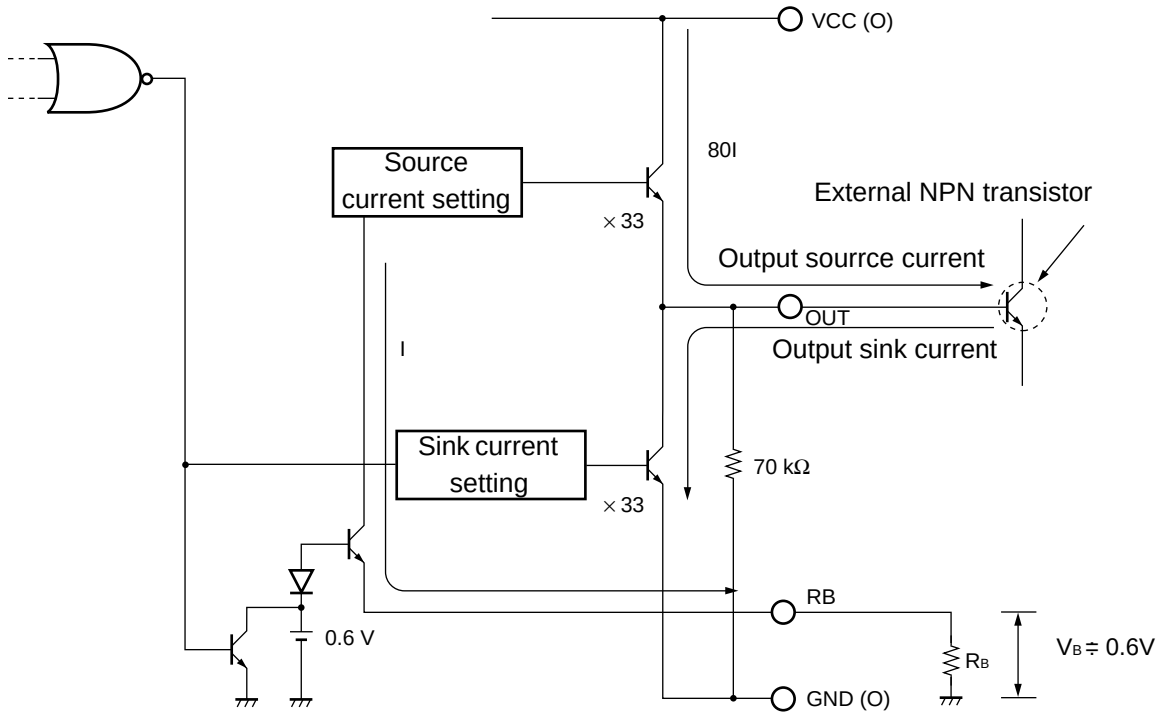
Note that because channels 1-6 operate at $Vcc \geq 4V$, Vcc and Vcc(0) must be set at the winding that produces V_{IN} + 2.2V in order to operate at $V_{IN} \geq 1.8V$.

■ METHOD OF SETTING THE OUTPUT CURRENT

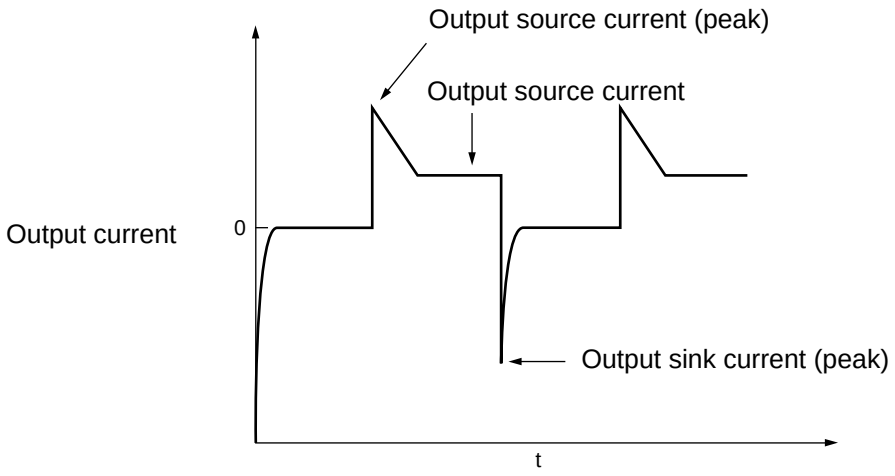
"Output circuit (main side)" shows the configuration of the output circuits (Drive1-3,Drive7), and "Output current waveform" illustrates how the source current value of the output current waveform has a constant current setting (When channel 1 operates as a step-up unit). Note that the source current is set by the following formula

Output source current = $(V_B/R_B) \times 80 \fallingdotseq 48/R_B$ [A] ($V_B \fallingdotseq 0.6V$)

Output circuit (main side)



Output current waveform



■ METHOD OF SETTING TIME CONSTANT FOR TIMER-LATCH SHORT PROTECTION CIRCUIT

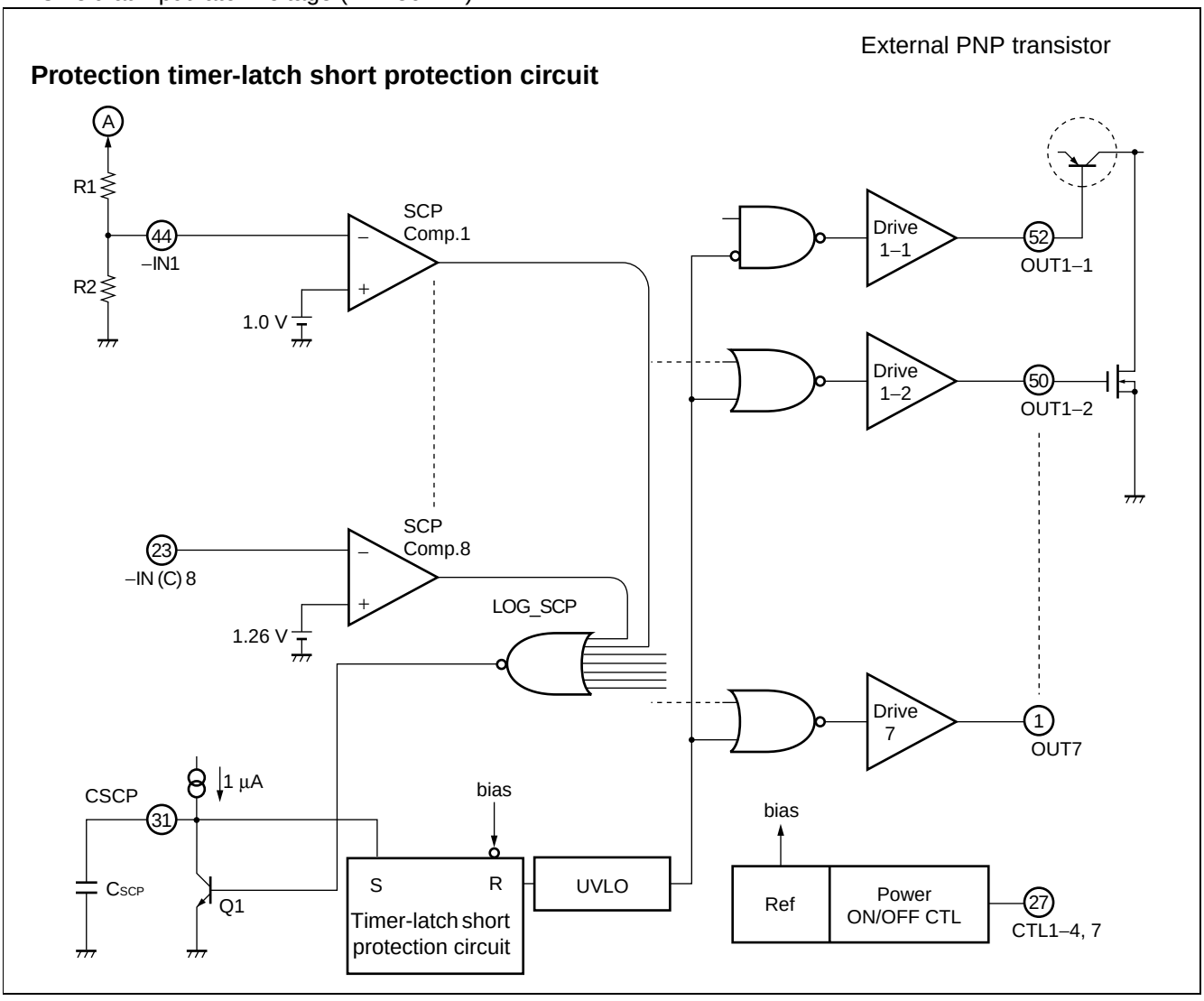
The short detection comparator (SCP comparator) in each of the channels constantly compares the error amplifier output level to the reference voltage and the –IN(C)8 terminal (pin 23).
While the switching regulator load conditions are stable on all channels, or when the voltage level at the –IN(C)8 pin is higher than the reference voltage, LOG_SCP output remains at "H" level, transistor Q1 is on, and the CSCP terminal (pin 31) is held at input standby voltage ($V_{STB} \fallingdotseq 50mV$).
If the load conditions change rapidly due to a short-circuiting of load, causing the output voltage to drop, or if the voltage at the –IN(C)8 terminal falls below the reference voltage level, the output from the short detection comparator on the corresponding channel or the input at the –IN(C)8 terminal goes to "H" level. This causes transistor Q1 to turn off and the external short protection capacitor C_{SCP} connected to the CSCP pin to charge at 1.0 µA.

Short Detection Time (t_{PE})

$t_{PE}(sec) \fallingdotseq 0.68 \times C_{SCP}$ (µF)

When the capacitor C_{SCP} is charged to the threshold voltage $V_{TH} \fallingdotseq 0.68$ V the SR latch is set, and the external PNP is turned off (dead time is set to 100%). At this point the SR latch input is closed and the CSCP terminal is held at input latch voltage ($V_I \fallingdotseq 50$ mV).

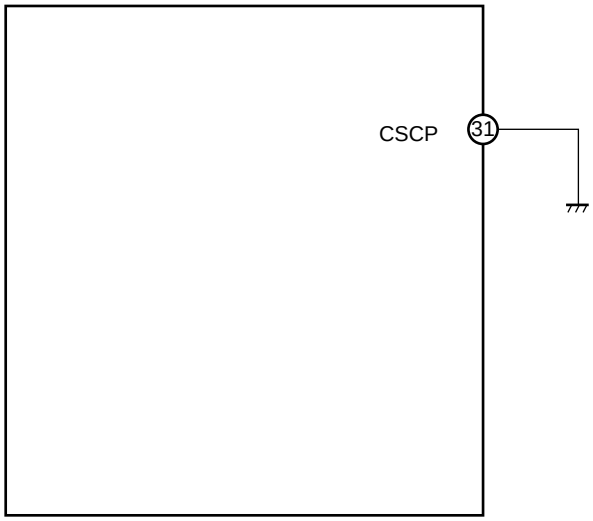
Protection timer-latch short protection circuit



■ TREATMENT WITHOUT USING CSCP

When you do not use the timer-latch short protection circuit, connect the CSCP terminal (pin 31) to GND with the shortest distance.

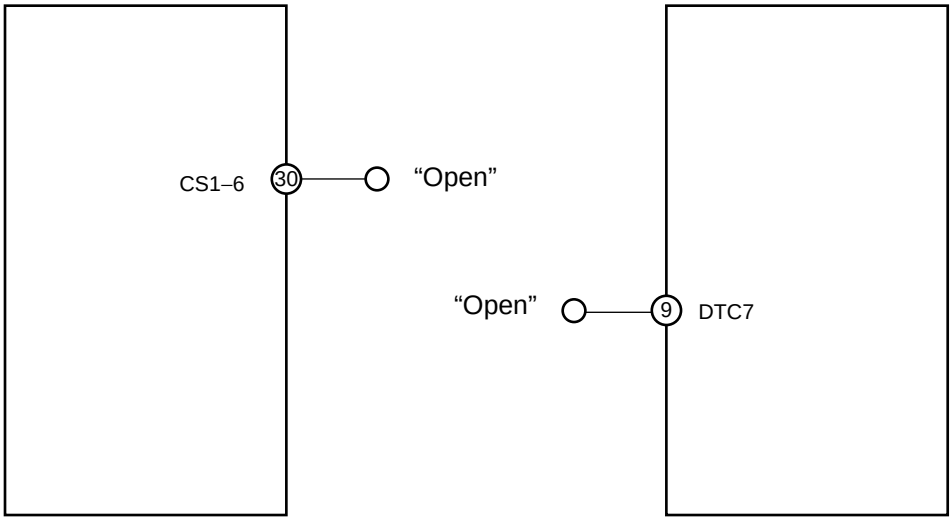
Treatment when not using CSCP



■ PROCESSING WITHOUT USING CS PIN

When not using the soft start function on channels 1 to 6, the CS1-6 terminal (pin 30)should be left open.
When not using the soft start function on channel 7, the DTC7 terminal (pin 9) should be left open.

When no soft start time is set



■ METHOD OF SETTING THE DEAD TIME

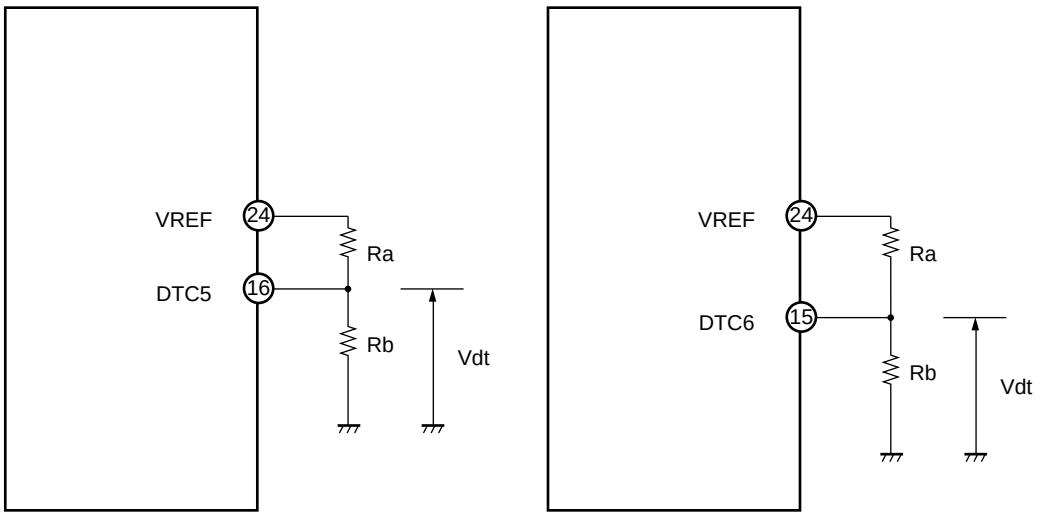
When setting step-up/step-down switching, Zeta type, or fly-back type step-up or inverter output, the output transistor at start-up is in full-on (ON duty cycle = 100%) state. To prevent this, the DTC voltage from the DTC1-1 terminal (pin 43) to the DTC6 terminal (pin 15) voltage is determined from the VREF voltage, as shown in following figure , so that the output transistor dead time (the maximum value of the ON interval) can be set easily.

When the voltage on the DTC5 and DTC6 terminals is lower than the triangular-wave output voltage from the oscillator, the output transistor turns off. The dead time calculation formula assuming that triangular-wave amplitude ≒ 0.7 V and triangular-wave maximum voltage ≒ 1.8 V is given below.

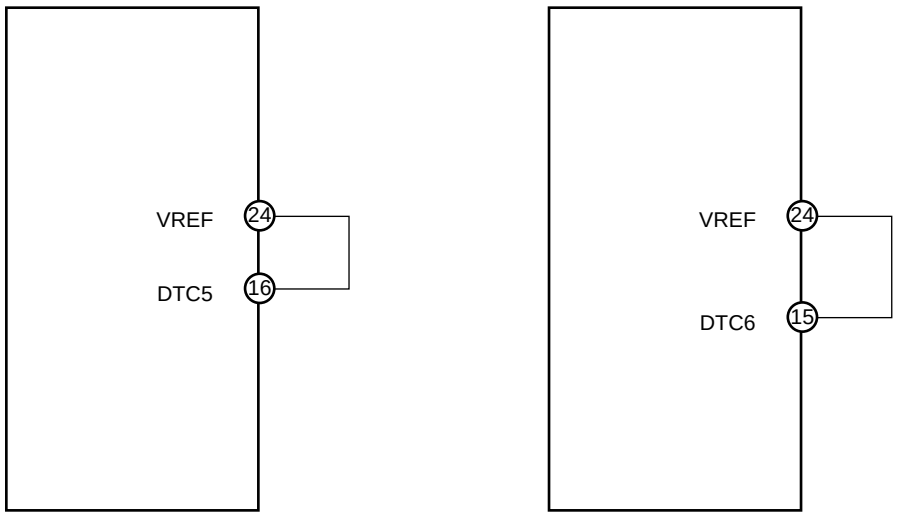
$$\text{DUTY(ON)max} \fallingdotseq \frac{\text{Vdt} - 1.1}{0.7} \times 100[\%],\ \text{Vdt} = \frac{\text{Rb}}{\text{Ra} + \text{Rb}} \times \text{VREF}$$

When you do not use these DTC5 and DTC6 terminals, connect then to VREF terminal (pin 24) as shown following figure (Not setting the channel 5,6 dead time).

Setting the channel 5, 6 dead time (same as for other channels)



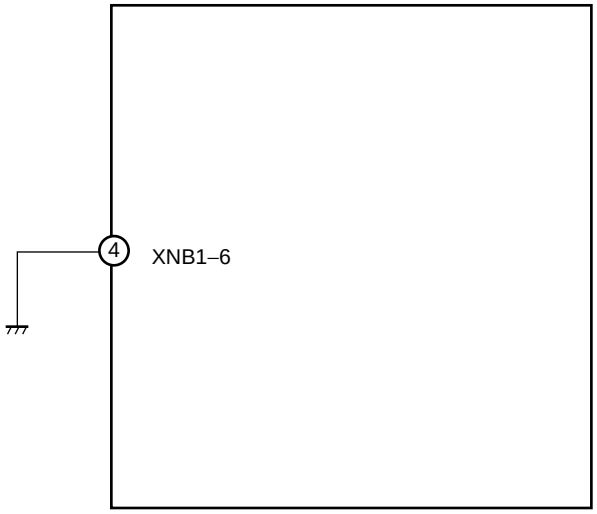
Not setting the channel 5,6 dead time (same as for other channels)



■ PROCESSING WHEN NOT USING THE XENB1-6 PIN

When V_{REF} control (channel 1 to 6 output control) is not used, the XENB1-6 terminal (pin 4) should be shorted to GND using the shortest available connection.

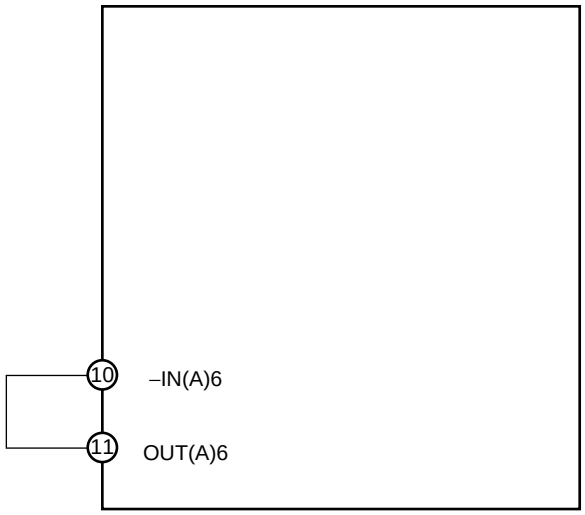
When not using the XENB1-6 pin



■ PROCESSING WHEN NOT USING THE CHANNEL 6 INV AMP.

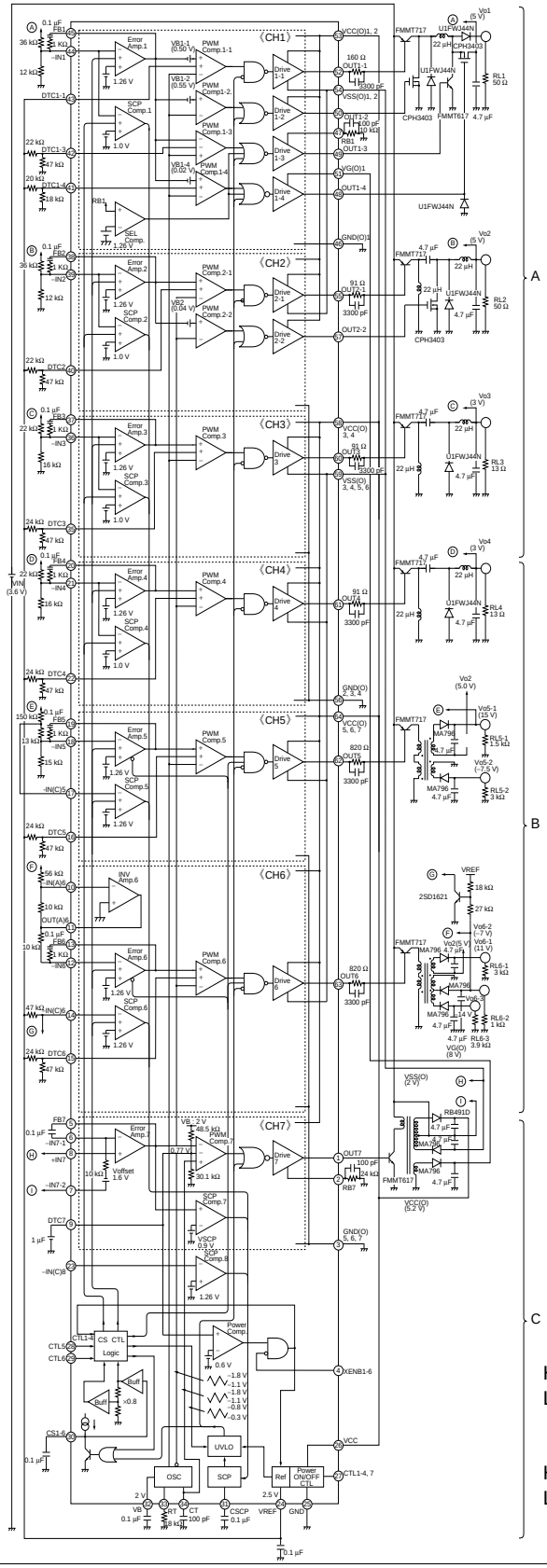
When the channel 6 INV amplifier is not in use, the -IN(A)6 terminal (pin 10), and OUT(A)6 terminal (pin 11) should be shorted using the shortest available connection.

When not using the channel 6 INV Amp.



■ APPLICATION EXAMPLE

- **General view**

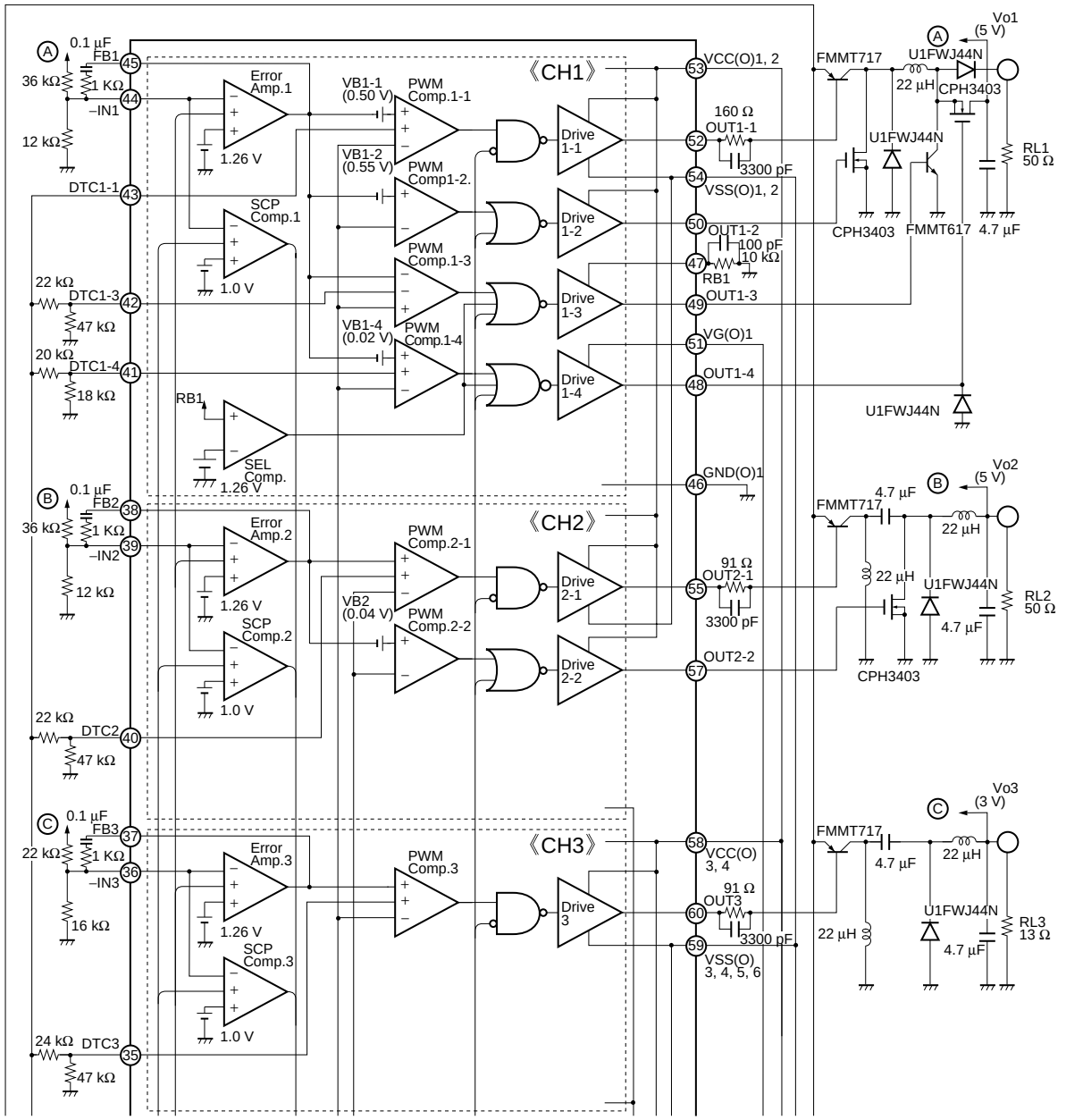


FMMT717: ZETEX plc.
FMMT617: ZETEX plc.
CPH3403: SANYO Electric Co., Ltd.
U1FWJ44N: TOSHIBA CORPORATION
MA796: Matsushita Electronic Components Co., Ltd.
2SD1621: SANYO Electric Co., Ltd.
RB491D: ROHM CO.LTD

H: Power/CH1 to 6 in OFF
L: Control by CTL terminal function

H: ON (Power/CH1 to 4,7)
L: OFF (Standby mode)

- **Enlarged view of A**



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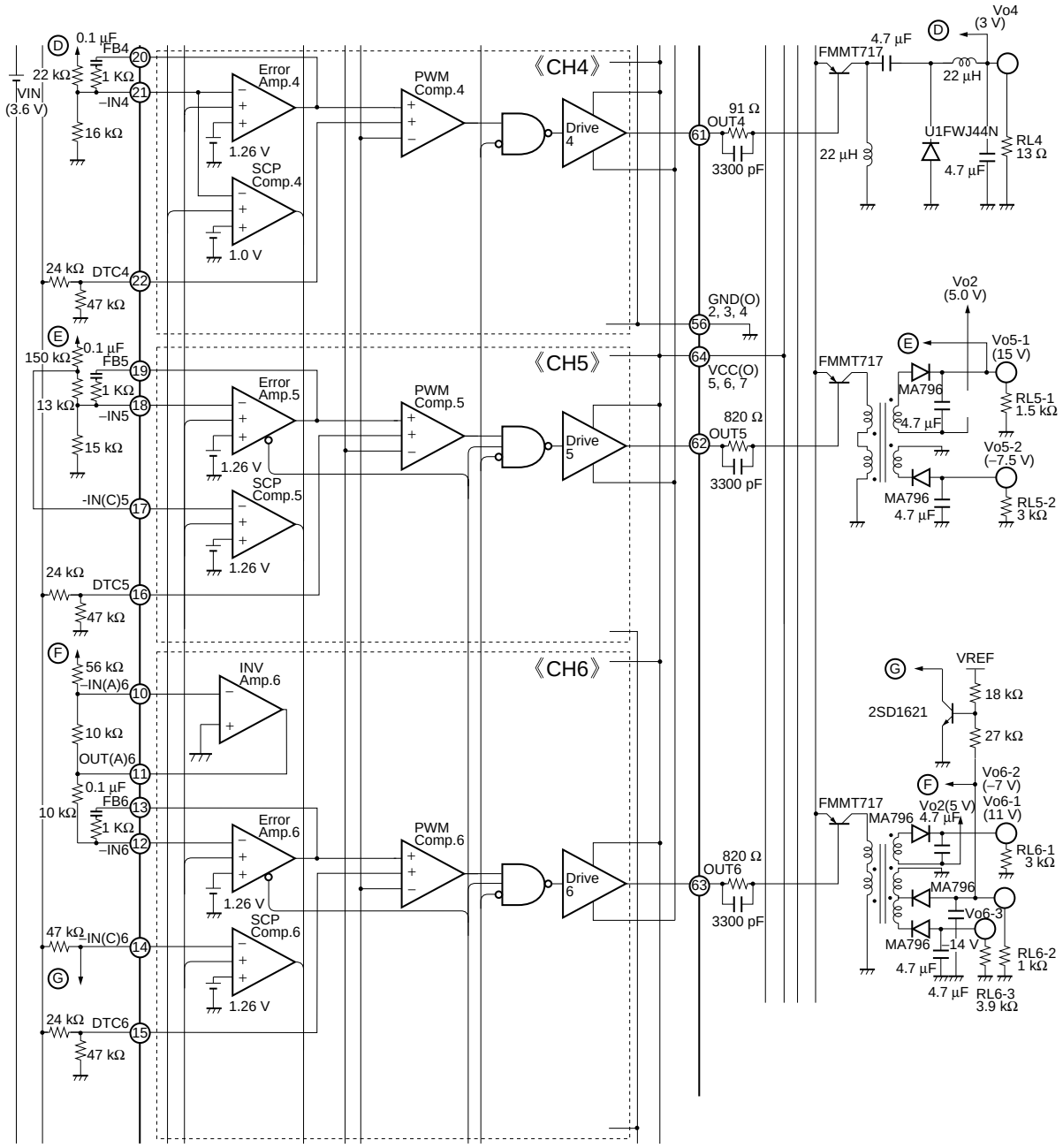
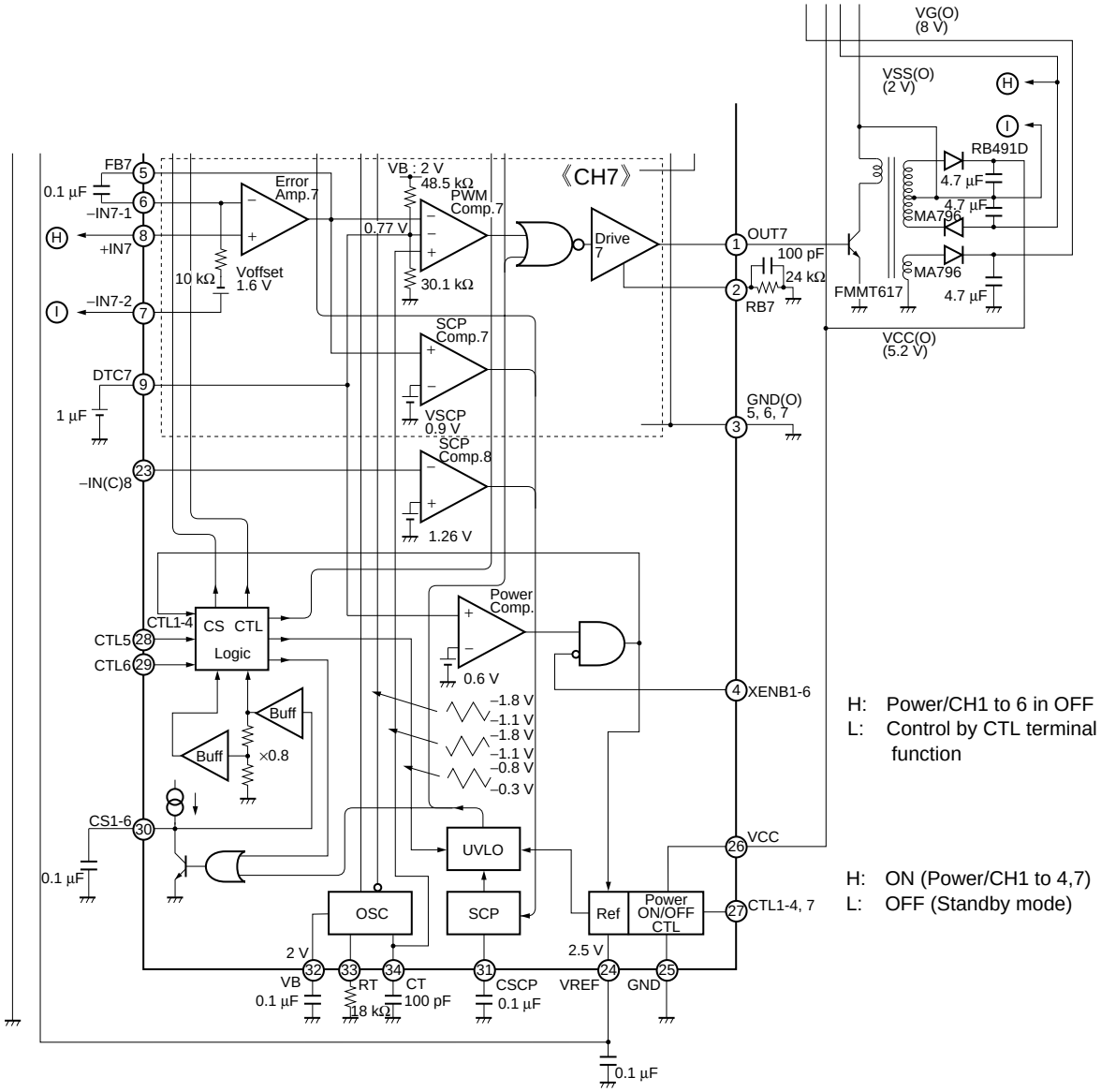
2SD1621: SANYO Electric Co., Ltd.
RB491D: ROHM CO.LTD

- **Enlarged view of B**



FMMT717: ZETEX plc.
FMMT617: ZETEX plc.
CPH3403: SANYO Electric Co., Ltd.
U1FWJ44N: TOSHIBA CORPORATION
MA796: Matsushita Electronic Components Co., Ltd.
2SD1621: SANYO Electric Co., Ltd.
RB491D: ROHM CO.LTD

- **Enlarged view of C**



FMMT717: ZETEX plc.
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MA796: Matsushita Electronic Components Co., Ltd.
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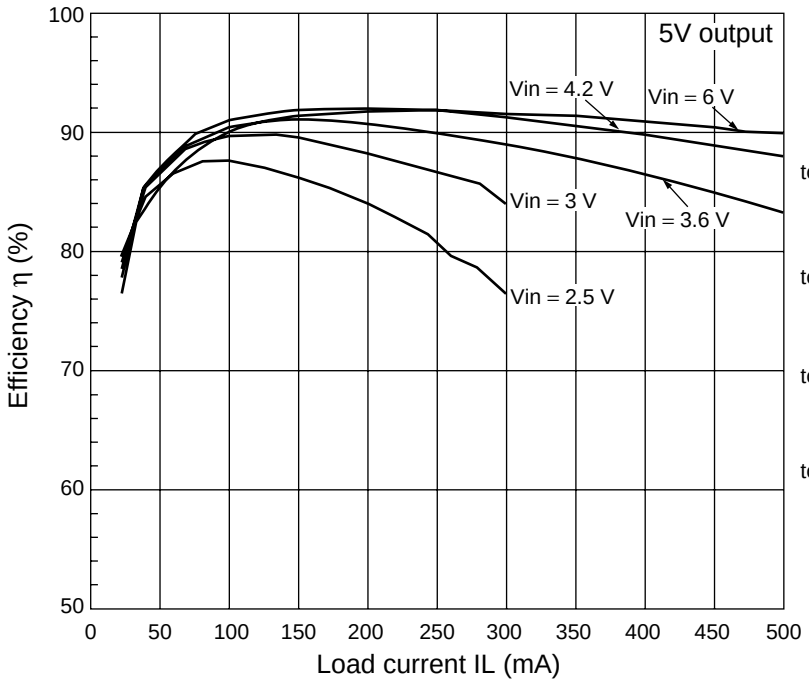
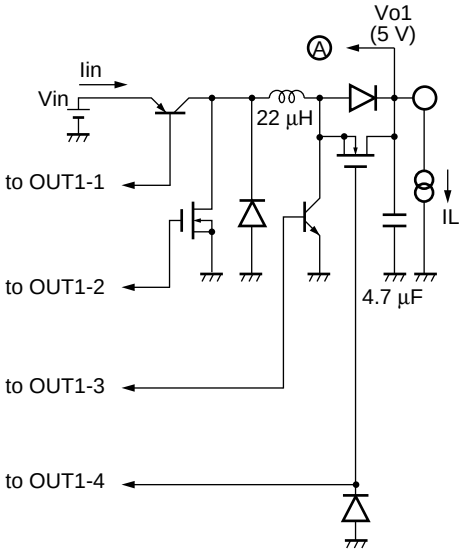
■ REFERENCE DATA

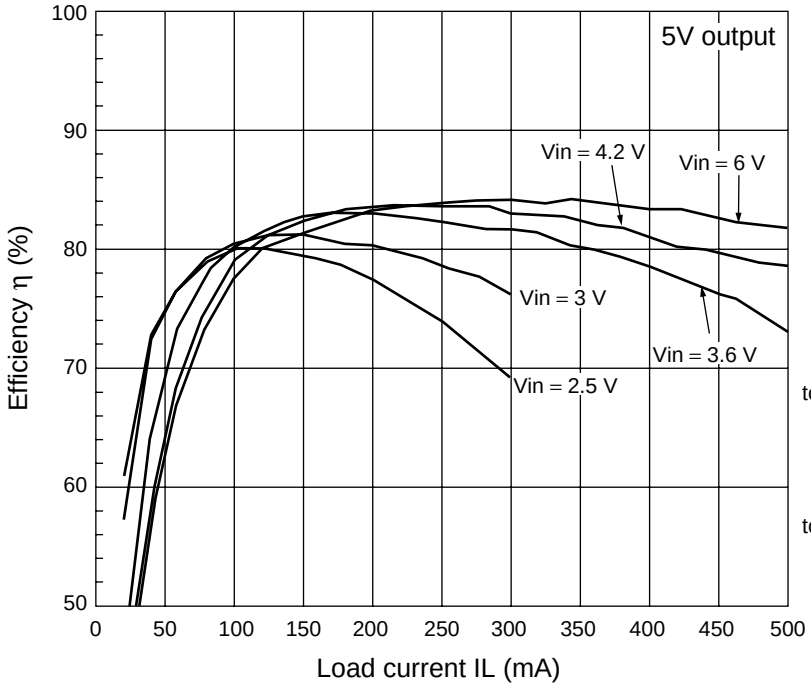
Efficiency vs. load current (ch1, step-up/step-down switching method)

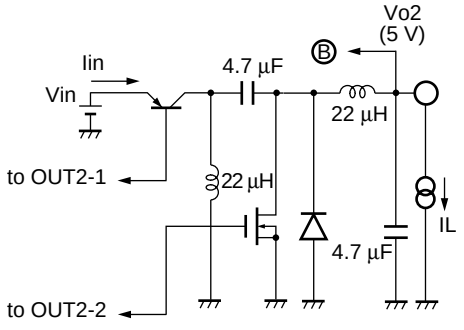




$$\eta = \frac{Vo1 \times IL}{Vin \times Iin} \times 100\ (\%)$$

Efficiency vs. load current (ch2, Zeta Method with Synchronous Rectification)





$$\eta = \frac{Vo2 \times IL}{Vin \times Iin} \times 100\ (\%)$$

■ USAGE PRECAUTIONS

1. Never use settings exceeding maximum rated conditions.

Exceeding maximum rated conditions may cause permanent damage to the LSI.
Also, it is recommended that recommended operating conditions be observed in normal use.
Exceeding recommended operating conditions may adversely affect LSI reliability.

2. Use this device within recommended operating conditions.

Recommended operating conditions are values within which normal LSI operation is warranted. Standard electrical characteristics are warranted within the range of recommended operating conditions and within the listed conditions for each parameter.

3. Printed circuit board ground lines should be set up with consideration for common impedance.

4. Take appropriate static electricity measures.

- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 mΩ between body and ground.

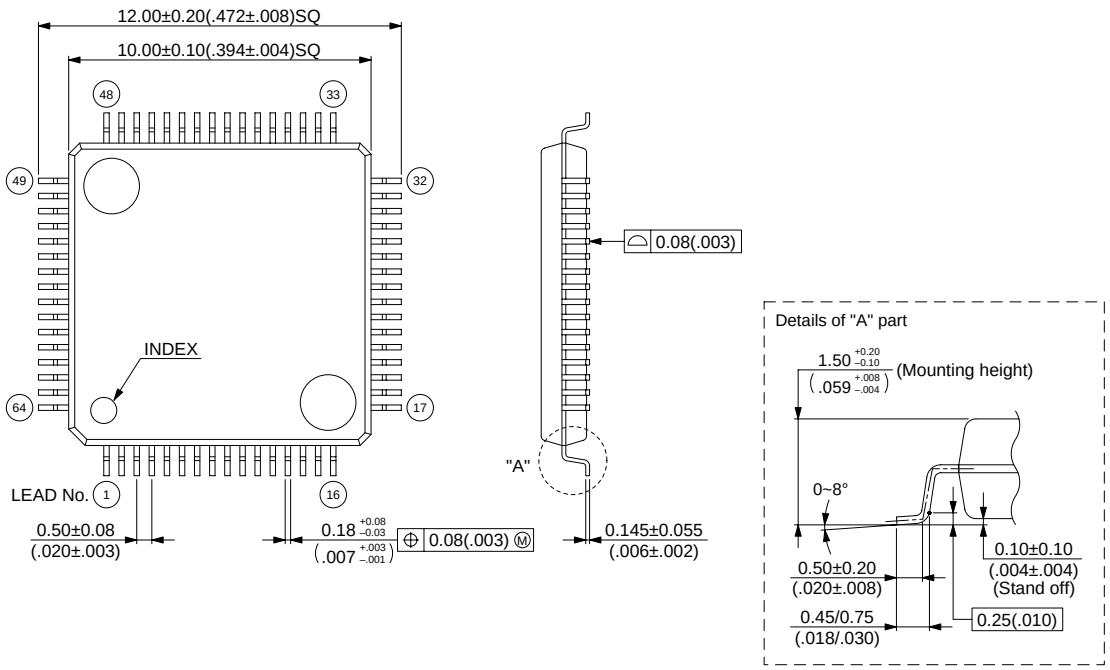
■ ORDERING INFORMATION

Part number	Package	Remarks
MB3827PFV	64-pin plastic LQFP (FPT-64P-M03)	

■ PACKAGE DIMENSION

64-pin Plastic LQFP
(FPT-64P-M03)

*Pins width and pins thickness include plating thickness.



Dimensions in: mm (inches)

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