

## 74VCX16722

### Low Voltage 22-Bit Register with 3.6V Tolerant Inputs and Outputs

#### General Description

The VCX16722 low voltage 22-bit register contains twenty-two non-inverting D-type flip-flops with 3-STATE outputs and is intended for bus oriented applications. The design has been optimized for use with JEDEC compliant 200 pin DIMM modules.

The 74VCX16722 is designed for low voltage (1.65V to 3.6V)  $V_{CC}$  applications with I/O capability up to 3.6V.

The 74VCX16722 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

#### Features

- 1.65V–3.6V  $V_{CC}$  specifications provided
- 3.6V tolerant inputs and outputs
- $t_{PD}$  (CLK to  $O_n$ )
  - 3.6ns max for 3.0V to 3.6V  $V_{CC}$
  - 4.6ns max for 2.3V to 2.7V  $V_{CC}$
  - 9.2ns max for 1.65V to 1.95V  $V_{CC}$
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- Meets JEDEC registered module specifications
- Static Drive ( $I_{OH}/I_{OL}$ )
  - ±24mA @ 3.0V
  - ±18mA @ 2.3V
  - ±6mA @ 1.65V
- Latchup performance exceeds 300 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model >200V

**Note 1:** To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current sourcing capability of the driver.

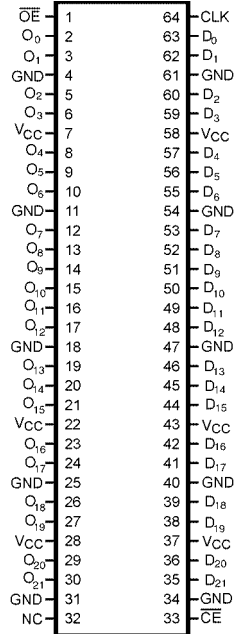
#### Ordering Code:

Order Number	Package Number	Package Description
74VCX16722MTD	MTD64	64-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

74VCX16722 Low Voltage 22-Bit Register with 3.6V Tolerant Inputs and Outputs

### Connection Diagram



### Pin Descriptions

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
$\overline{CE}$	Clock Enable Input (Active Low)
CLK	Clock Input
$D_1 - D_{21}$	Data Inputs
$O_1 - O_{21}$	3-STATE Outputs

### Truth Table

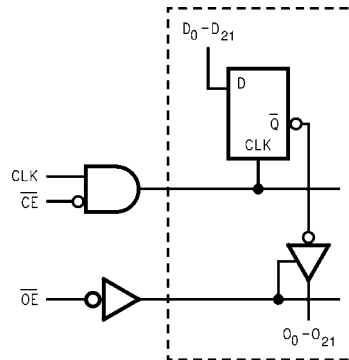
CLK	$\overline{CE}$	$\overline{OE}$	$D_0 - D_{21}$	$O_0 - O_{21}$
X	X	H	X	Z
X	H	L	X	$O_0$
↗	L	L	L	L
↗	L	L	H	H
L or H	L	L	X	$O_0$

H = HIGH Voltage Level  
 L = LOW Level Voltage  
 X = Immaterial (HIGH or LOW, Inputs may not float)  
 Z = High Impedance  
 $O_0$  = Previous  $O_0$  before LOW-to-HIGH transition of Clock  
 ↗ = LOW-to-HIGH transition

### Functional Description

The VCX16722 contains twenty-two D-type flip-flops with 3-STATE standard outputs. The twenty-two flip-flops will store the state of their individual D-type inputs that meet the setup and hold time requirements on the LOW-HIGH Clock (CLK) transition, when the Clock-Enable ( $\overline{CE}$ ) is LOW. The 3-STATE standard outputs are controlled by the Output-Enable ( $\overline{OE}$ ). When  $\overline{OE}$  is HIGH, the standard outputs are in high impedance mode but this does not interfere with entering new data into the flip-flops.

### Logic Diagram



**Absolute Maximum Ratings** (Note 2)

Supply Voltage ( $V_{CC}$ )	-0.5V to +4.6V
DC Input Voltage ( $V_I$ )	-0.5V to +4.6V
Output Voltage ( $V_O$ )	
Outputs 3-STATE	-0.5V to +4.6V
Outputs Active (Note 3)	-0.5 to $V_{CC} + 0.5V$
DC Input Diode Current ( $I_{IK}$ ) $V_I < 0V$	-50 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O < 0V$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Supply Pin ( $I_{CC}$ or Ground)	$\pm 100$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C

**Recommended Operating Conditions** (Note 4)

Power Supply	
Operating	1.65V to 3.6V
Data Retention Only	1.2V to 3.6V
Input Voltage	-0.3V to 3.6V
Output Voltage ( $V_O$ )	
Output in Active States	0V to $V_{CC}$
Output in 3-STATE	0.0V to 3.6V
Output Current in $I_{OH}/I_{OL}$	
$V_{CC} = 3.0V$ to 3.6V	$\pm 24$ mA
$V_{CC} = 2.3V$ to 2.7V	$\pm 18$ mA
$V_{CC} = 1.65V$ to 2.3V	$\pm 6$ mA
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

**Note 2:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The Recommended Operating Conditions tables will define the conditions for actual device operation.

**Note 3:**  $I_O$  Absolute Maximum Rating must be observed.

**Note 4:** Floating or unused pin (inputs or I/O's) must be held HIGH or LOW.

**DC Electrical Characteristics (2.7V <  $V_{CC}$  ≤ 3.6V)**

Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min	Max	Units
$V_{IH}$	HIGH Level Input Voltage		2.7-3.6	2.0		V
$V_{IL}$	LOW Level Input Voltage		2.7-3.6		0.8	V
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -18 \text{ mA}$ $I_{OH} = -24 \text{ mA}$	2.7-3.6 2.7 3.0 3.0	$V_{CC} - 0.2$ 2.2 2.4 2.2		V
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 18 \text{ mA}$ $I_{OL} = 24 \text{ mA}$	2.7-3.6 2.7 3.0 3.0		0.2 0.4 0.4 0.55	V
$I_I$	Input Leakage Current	$0V \leq V_I \leq 3.6V$	2.7-3.6		$\pm 5.0$	$\mu A$
$I_{OZ}$	3-STATE Output Leakage	$0V \leq V_O \leq 3.6V$ $V_I = V_{IH}$ or $V_{IL}$	2.7-3.6		$\pm 10$	$\mu A$
$I_{OFF}$	Power Off Leakage Current	$0V \leq (V_I, V_O) \leq 3.6V$	0		10	$\mu A$
$I_{CC}$	Quiescent Supply Current	$V_I = V_{CC}$ or GND $V_{CC} \leq (V_I, V_O) \leq 3.6V$ (Note 5)	2.7-3.6 2.7-3.6		20 $\pm 20$	$\mu A$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	$V_{IH} = V_{CC} - 0.6V$	2.7-3.6		750	$\mu A$

**Note 5:** Outputs disabled or 3-STATE only.

### DC Electrical Characteristics ( $2.3V \leq V_{CC} \leq 2.7V$ )

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	Min	Max	Units
V <sub>IH</sub>	HIGH Level Input Voltage		2.3-2.7	1.6		V
V <sub>IL</sub>	LOW Level Input Voltage		2.3-2.7		0.7	V
V <sub>OH</sub>	HIGH Level Output Voltage	I <sub>OH</sub> = -100 μA I <sub>OH</sub> = -6 mA I <sub>OH</sub> = -12 mA I <sub>OH</sub> = -18 mA	2.3-2.7 2.3 2.3 2.3	V <sub>CC</sub> - 0.2 2.0 1.8 1.7		V
V <sub>OL</sub>	LOW Level Output Voltage	I <sub>OL</sub> = 100 μA I <sub>OL</sub> = 12mA I <sub>OL</sub> = 18 mA	2.3-2.7 2.3 2.3		0.2 0.4 0.6	V
I <sub>I</sub>	Input Leakage Current	0 ≤ V <sub>I</sub> ≤ 3.6V	2.3-2.7		±5.0	μA
I <sub>OZ</sub>	3-STATE Output Leakage	0 ≤ V <sub>O</sub> ≤ 3.6V V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.3-2.7		±10	μA
I <sub>OFF</sub>	Power Off Leakage Current	0 ≤ (V <sub>I</sub> , V <sub>O</sub> ) ≤ 3.6V	0		10	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND V <sub>CC</sub> ≤ (V <sub>I</sub> , V <sub>O</sub> ) ≤ 3.6V (Note 6)	2.3-2.7 2.3-2.7		20 ±20	μA

Note 6: Outputs disabled or 3-STATE only.

### DC Electrical Characteristics ( $1.65V \leq V_{CC} < 2.3V$ )

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	Min	Max	Units
V <sub>IH</sub>	HIGH Level Input Voltage		1.65 - 2.3	0.65 × V <sub>CC</sub>		V
V <sub>IL</sub>	LOW Level Input Voltage		1.65 - 2.3		0.35 × V <sub>CC</sub>	V
V <sub>OH</sub>	HIGH Level Output Voltage	I <sub>OH</sub> = -100 μA I <sub>OH</sub> = -6 mA	1.65 - 2.3 1.65	V <sub>CC</sub> - 0.2 1.25		V
V <sub>OL</sub>	LOW Level Output Voltage	I <sub>OL</sub> = 100 μA I <sub>OL</sub> = 6mA	1.65 - 2.3 1.65		0.2 0.3	V
I <sub>I</sub>	Input Leakage Current	0 ≤ V <sub>I</sub> ≤ 3.6V	1.65 - 2.3		±5.0	μA
I <sub>OZ</sub>	3-STATE Output Leakage	0 ≤ V <sub>O</sub> ≤ 3.6V V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	1.65 - 2.3		±10	μA
I <sub>OFF</sub>	Power Off Leakage Current	0 ≤ (V <sub>I</sub> , V <sub>O</sub> ) ≤ 3.6V	0		10	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND V <sub>CC</sub> ≤ (V <sub>I</sub> , V <sub>O</sub> ) ≤ 3.6V (Note 7)	1.65 - 2.3 1.65 - 2.3		20 ±20	μA

Note 7: Outputs disabled or 3-STATE only.

AC Electrical Characteristics (Note 8)								
Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}, C_L = 30 \text{ pF}, R_L = 500\Omega$						Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.5 \pm 0.2V$		$V_{CC} = 1.8 \pm 0.15V$		
		Min	Max	Min	Max	Min	Max	
$f_{MAX}$	Maximum Clock Frequency	250		200		100		MHz
$t_{PHL}, t_{PLH}$	Propagation Delay Clock to Bus	1.3	3.6	1.5	4.6	2.0	9.2	ns
$t_{PZL}, t_{PZH}$	Output Enable Time	0.6	3.5	0.8	4.5	1.5	9.0	ns
$t_{PLZ}, t_{PHZ}$	Output Disable Time	0.6	3.2	0.8	4.2	1.5	7.6	ns
$t_S$	Setup Time	2.0		2.0		3.0		ns
$t_H$	Hold Time	0.0		0.0		0.5		ns
$t_W$	Pulse Width	1.5		1.5		4.0		ns
$t_{OSHL}$	Output to Output Skew		0.5		0.5		0.75	ns
$t_{OSLH}$	(Note 9)							
<p><b>Note 8:</b> For <math>C_L = 50 \text{ pF}</math>, add approximately 300 ps to the AC maximum specification.</p> <p><b>Note 9:</b> Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (<math>t_{OSHL}</math>) or LOW-to-HIGH (<math>t_{OSLH}</math>).</p>								
AC Electrical Characteristics Over Load (Note 10)								
Symbol	Parameter	$T_A = -0^\circ\text{C to } +70^\circ\text{C}, R_L = 500\Omega, V_{CC} = 3.3V \pm 0.3V$				Units		
		$C_L = 0 \text{ pF}$		$C_L = 50 \text{ pF}$				
		Min	Max	Min	Max			
$t_{PHL}, t_{PLH}$	Prop Delay Clock to Bus	1.1	2.5	1.9	3.9	ns		
$t_{PZL}, t_{PZH}$	Output Enable Time	0.7	2.4	1.0	3.8	ns		
$t_{PLZ}, t_{PHZ}$	Output Disable Time	0.7	2.1	1.0	3.5	ns		
$t_S$	Setup Time	2.0		2.0		ns		
$t_H$	Hold Time	0.0		0.0		ns		
$t_W$	Pulse Width	1.5		1.5		ns		
<p><b>Note 10:</b> This parameter is guaranteed by characterization but not tested.</p>								
Dynamic Switching Characteristics								
Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$		Units		
				Typical				
$V_{OLP}$	Quiet Output Dynamic Peak $V_{OL}$	$C_L = 30 \text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0V$	1.8	0.25		V		
			2.5	0.6				
			3.3	0.8				
$V_{OLV}$	Quiet Output Dynamic Valley $V_{OL}$	$C_L = 30 \text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0V$	1.8	-0.25		V		
			2.5	-0.6				
			3.3	-0.8				
$V_{OHV}$	Quiet Output Dynamic Valley $V_{OH}$	$C_L = 30 \text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0V$	1.8	1.5		V		
			2.5	1.9				
			3.3	2.2				

## Capacitance

Symbol	Parameter	Conditions	T <sub>A</sub> = +25°C		Units
			Typical		
C <sub>IN</sub>	Input Capacitance	V <sub>I</sub> = 0V or V <sub>CC</sub> , V <sub>CC</sub> = 1.8V, 2.5V, or 3.3V,	3.5		pF
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>I</sub> = 0V, or V <sub>CC</sub> , V <sub>CC</sub> = 1.8V, 2.5V or 3.3V	5.5		pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>I</sub> = 0V or V <sub>CC</sub> , f = 10 MHz, V <sub>CC</sub> = 1.8V, 2.5V or 3.3V	13		pF

## I<sub>OUT</sub> - V<sub>OUT</sub> Characteristics

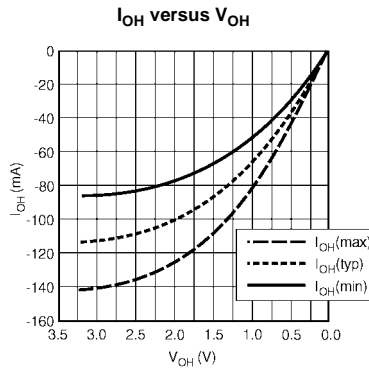


FIGURE 1. Characteristics for Output - Pull Up Driver

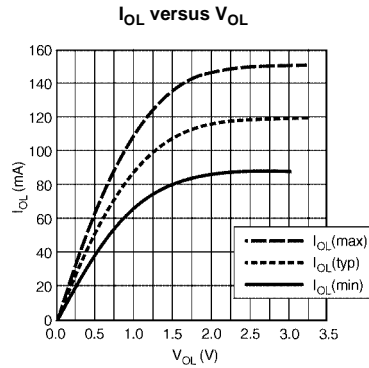


FIGURE 2. Characteristics for Output - Pull Down Driver

### AC Loading and Waveforms

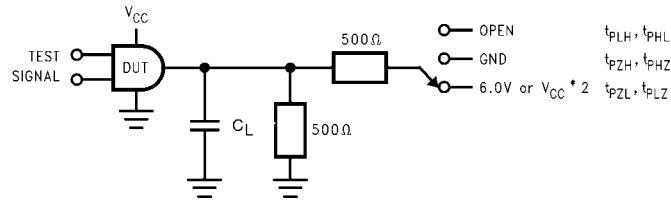


FIGURE 3. AC Test Circuit

TEST	SWITCH
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	6V at $V_{CC} = 3.3 \pm 0.3V$ ; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$ ; 1.8V to $\pm 0.15V$
$t_{PZH}, t_{PHZ}$	GND

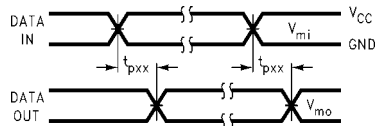


FIGURE 4. Waveform for Inverting and Non-inverting Functions  
 $t_r = t_f \leq 2.0ns, 10\% \text{ to } 90\%$

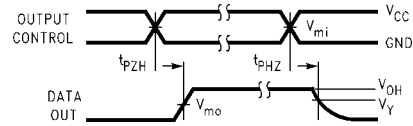


FIGURE 5. 3-STATE Output High Enable and Disable Times for Low Voltage Logic  
 $t_r = t_f \leq 2.0ns, 10\% \text{ to } 90\%$

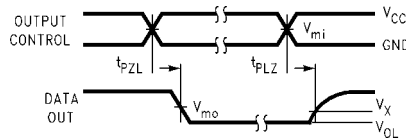
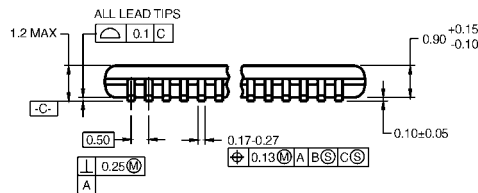
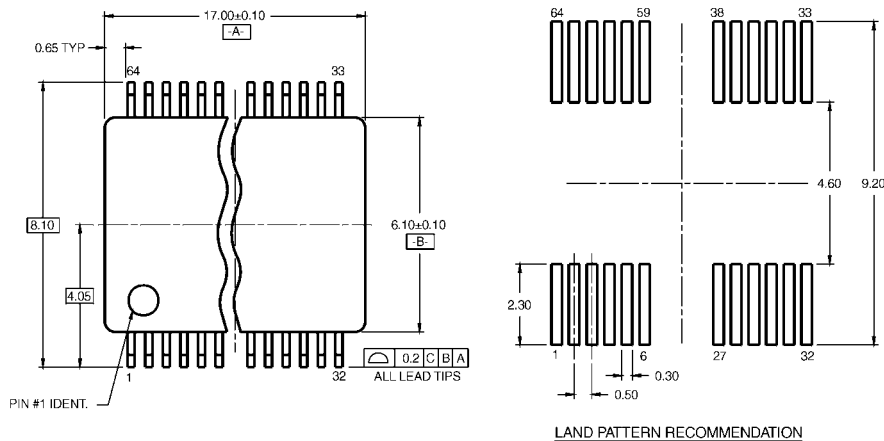


FIGURE 6. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic  
 $t_r = t_f \leq 2.0ns, 10\% \text{ to } 90\%$

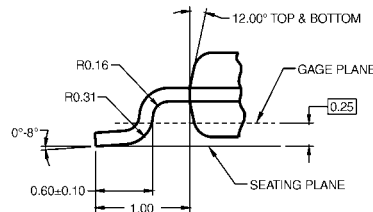
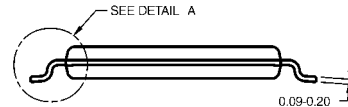
Symbol	$V_{CC}$		
	$3.3V \pm 0.3V$	$2.5V \pm 0.2V$	$1.8 \pm 0.15V$
$V_{mi}$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_{mo}$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_x$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
$V_y$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

**Physical Dimensions** inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION EF, REF NOTE 6, DATE 7/93.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
  - D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.



DETAIL A

MTD64REV B

**64-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD64**

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