| FAIRCHILD |  |  | January 1990 |  |
| :---: | :---: | :---: | :---: | :---: |
| SEMICロNDபСTロRтм |  |  |  |  |
| $74 \mathrm{ACQ646}$-74ACTQ646 |  |  |  |  |
| Quiet Se with 3-S? | ries ${ }^{\text {TM }}$ Oct | with 3-STATE Outputs |  |  |
| General De | scription |  | Features |  |
| The ACQ/ACTQ6 circuits, with outpu providing multiplex input bus or from the A or B bus will be the LOW-to-HIGH (CPAB or CPBA). available are illust Figure 4. <br> The ACQ/ACTQ ogy to guarantee dynamic threshold tures GTOTM outp addition to a split | 46 consist of registe <br> ts, D-type flip-flops, <br> ed transmission of he internal storage re loaded into the res transition of the ap The four fundamenta ated in Figure 1, Fig <br> tilizes Fairchild Qui quiet output switc performance. FACT ut control and und round bus for superi | ered bus transceiver , and control circuitry data directly from the registers. Data on the spective registers on appropriate clock pin tal handling functions Figure 2, Figure 3 and <br> uiet Series ${ }^{\text {TM }}$ technolching and improved T Quiet Series ${ }^{\text {TM }}$ feadershoot corrector in rior performance. | Guaranteed sim dynamic thresh <br> Guaranteed pin <br> - Independent reg <br> ■ Multiplexed real <br> - 300 mil slim dua <br> Outputs source <br> - Faster prop del | aneous switching noise level and performance <br> in skew AC performance <br> rs for $A$ and $B$ busses <br> and stored data transfers <br> line package <br> 24 mA <br> han the standard AC/ACT646 |
| Ordering Code: |  |  |  |  |
| Order Number | Package Number |  | Package | ription |
| 74ACQ646SC | M24B | 24-Lead Small Outlin | Integrated Circuit ( | ), JEDEC MS-013, 0.300 Wide |
| 74ACQ464ASPC | N24C | 24-Lead Plastic Dua | -Line Package (PD | JEDEC MS-001, 0.300 Wide |
| 74ACTQ646SC | M24B | 24-Lead Small Outl | Integrated Circuit ( | ), JEDEC MS-013, 0.300 Wide |
| 74ACTQ464ASPC | N24C | 24-Lead Plastic Dua | -Line Package (PD | JEDEC MS-001, 0.300 Wide |
| Device also available in Tape and Reel. Specify by appending suffix letter " X " to the ordering code. <br> Connection Diagram <br> Pin Descriptions |  |  |  |  |
|  |  | $-\mathrm{v}_{\mathrm{cc}}$ <br> - CPBA <br> -sba <br> - $\bar{G}$ <br> $-B_{0}$ <br> - $_{1}$ <br> $-B_{2}$ <br> $-\mathrm{B}_{3}$ <br> $-B_{4}$ <br> $-B_{5}$ <br> - ${ }^{8}$ <br> - ${ }^{\theta_{7}}$ | Pin Names <br> $A_{0}-A_{7}$ <br> $B_{0}-B_{7}$ <br> CPAB, CPBA <br> SAB, SBA <br> $\bar{G}$ <br> DIR | Descriptions <br> Data Register A Inputs <br> Data Register A Outputs <br> Data Register B Inputs <br> Data Register B Outputs <br> Clock Pulse Inputs <br> Transmit/Receive Inputs <br> Output Enable Input <br> Direction Control Input |

## Logic Symbols



Function Table



| Absolute Maximum Ratings（Note 2） |  |
| :---: | :---: |
| Supply Voltage（ $\mathrm{V}_{\mathrm{CC}}$ ） | -0.5 V to +7.0 V |
| DC Input Diode Current（ $\mathrm{I}_{\mathrm{K}}$ ） |  |
| $V_{1}=-0.5 \mathrm{~V}$ | －20 mA |
| $\mathrm{V}_{1}=\mathrm{V}_{C C}+0.5 \mathrm{~V}$ | ＋20 mA |
| DC Input Voltage（ $\mathrm{V}_{\mathrm{l}}$ ） | -0.5 V to $\mathrm{V}_{C C}+0.5 \mathrm{~V}$ |
| DC Output Diode Current（ $\mathrm{l}_{\mathrm{OK}}$ ） |  |
| $\mathrm{V}_{\mathrm{O}}=-0.5 \mathrm{~V}$ | －20 mA |
| $\mathrm{V}_{\mathrm{O}}=\mathrm{V}_{\mathrm{CC}}+0.5 \mathrm{~V}$ | ＋20 mA |
| DC Output Voltage（ $\mathrm{V}_{\mathrm{O}}$ ） | -0.5 V to $\mathrm{V}_{\mathrm{CC}}+0.5 \mathrm{~V}$ |
| DC Output Source or Sink Current（ $\mathrm{l}_{\mathrm{O}}$ ） | $\pm 50 \mathrm{~mA}$ |
| DC $\mathrm{V}_{\mathrm{CC}}$ or Ground Current per Output Pin（ $\mathrm{I}_{\mathrm{CC}}$ or $\mathrm{I}_{\mathrm{GND}}$ ） | $\pm 50 \mathrm{~mA}$ |
| Storage Temperature（ $\mathrm{T}_{\text {STG }}$ ） | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| DC Latch－Up Source or Sink Current | $\pm 300 \mathrm{~mA}$ |
| Junction Temperature（ $\mathrm{T}_{\mathrm{J}}$ ） |  |
| PDIP | $140^{\circ} \mathrm{C}$ |

## Recommended Operating Conditions

| Supply Voltage $\left(\mathrm{V}_{\mathrm{CC}}\right)$ | 2.0 V to 6.0 V |
| :--- | ---: |
| ACQ | 4.5 V to 5.5 V |
| ACTQ | 0 V to $\mathrm{V}_{\mathrm{CC}}$ |
| Input Voltage $\left(\mathrm{V}_{\mathrm{I}}\right)$ | 0 V to $\mathrm{V}_{\mathrm{CC}}$ |
| Output Voltage $\left(\mathrm{V}_{\mathrm{O}}\right)$ | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |
| Operating Temperature $\left(\mathrm{T}_{\mathrm{A}}\right)$ |  |
| Minimum Input Edge Rate $\Delta \mathrm{V} / \Delta \mathrm{t}$ |  |
| ACQ Devices |  |
| $\mathrm{V}_{\text {IN }}$ from $30 \%$ to $70 \%$ of $\mathrm{V}_{\mathrm{CC}}$ | $125 \mathrm{mV} / \mathrm{ns}$ |
| $\mathrm{V}_{\mathrm{CC}} @ 3.0 \mathrm{~V}, 4.5 \mathrm{~V}, 5.5 \mathrm{~V}$ |  |
| Minimum Input Edge Rate $\Delta \mathrm{V} / \Delta \mathrm{t}$ |  |
| ACTQ Devices |  |
| $\mathrm{V}_{\text {IN }}$ from 0.8 V to 2.0 V | $125 \mathrm{mV} / \mathrm{ns}$ |
| $\mathrm{V}_{\mathrm{CC}} @ 4.5 \mathrm{~V}, 5.5 \mathrm{~V}$ |  |

Note 2：Absolute maximum ratings are those values beyond which damage to the device may occur．The databook specifications should be met，with out exception，to ensure that the system design is reliable over its power supply，temperature，and output／input loading variables．Fairchild does no recommend operation of FACT $^{\text {M }}$ circuits outside databook specifications．

## DC Electrical Characteristics for ACQ

| Symbol | Parameter | $\mathrm{V}_{\mathrm{cc}}$ <br> （V） | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | Units | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Typ | Guaranteed Limits |  |  |  |
| $\overline{\mathrm{V}_{\mathrm{IH}}}$ | Minimum HIGH Level Input Voltage | $\begin{aligned} & 3.0 \\ & 4.5 \\ & 5.5 \end{aligned}$ | $\begin{gathered} \hline 1.5 \\ 2.25 \\ 2.75 \\ \hline \end{gathered}$ | $\begin{gathered} \hline 2.1 \\ 3.15 \\ 3.85 \\ \hline \end{gathered}$ | $\begin{gathered} \hline 2.1 \\ 3.15 \\ 3.85 \\ \hline \end{gathered}$ | V | $\begin{aligned} & \mathrm{V}_{\text {OUT }}=0.1 \mathrm{~V} \\ & \text { or } \mathrm{V}_{\mathrm{CC}}-0.1 \mathrm{~V} \end{aligned}$ |
| $\mathrm{V}_{\mathrm{IL}}$ | Maximum LOW Level Input Voltage | $\begin{aligned} & \hline 3.0 \\ & 4.5 \\ & 5.5 \\ & \hline \end{aligned}$ | $\begin{gathered} \hline 1.5 \\ 2.25 \\ 2.75 \\ \hline \end{gathered}$ | $\begin{gathered} \hline 0.9 \\ 1.35 \\ 1.65 \\ \hline \end{gathered}$ | $\begin{gathered} \hline 0.9 \\ 1.35 \\ 1.65 \\ \hline \end{gathered}$ | V | $\begin{aligned} & \mathrm{V}_{\text {OUT }}=0.1 \mathrm{~V} \\ & \text { or } \mathrm{V}_{\mathrm{CC}}-0.1 \mathrm{~V} \end{aligned}$ |
| $\mathrm{V}_{\mathrm{OH}}$ | Minimum HIGH Level Output Voltage | $\begin{aligned} & \hline 3.0 \\ & 4.5 \\ & 5.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline 2.99 \\ & 4.49 \\ & 5.49 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline 2.9 \\ & 4.4 \\ & 5.4 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline 2.9 \\ & 4.4 \\ & 5.4 \end{aligned}$ | V | l OUt $=-50 \mu \mathrm{~A}$ |
|  |  | $\begin{aligned} & 3.0 \\ & 4.5 \\ & 5.5 \end{aligned}$ |  | $\begin{aligned} & 2.56 \\ & 3.86 \\ & 4.85 \end{aligned}$ | $\begin{aligned} & 2.46 \\ & 3.76 \\ & 4.76 \end{aligned}$ | V | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IL}} \text { or } \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{I}_{\mathrm{OH}}=-12 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{OH}}=-24 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{OH}}=-24 \mathrm{~mA}(\text { Note } 3) \end{aligned}$ |
| $\mathrm{V}_{\text {OL }}$ | Maximum LOW Level Output Voltage | $\begin{aligned} & \hline 3.0 \\ & 4.5 \\ & 5.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline 0.002 \\ & 0.001 \\ & 0.001 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline 0.1 \\ & 0.1 \\ & 0.1 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.1 \\ & 0.1 \\ & 0.1 \end{aligned}$ | V | lout $=50 \mu \mathrm{~A}$ |
|  |  | $\begin{aligned} & 3.0 \\ & 4.5 \\ & 5.5 \end{aligned}$ |  | $\begin{aligned} & 0.36 \\ & 0.36 \\ & 0.36 \end{aligned}$ | $\begin{aligned} & 0.44 \\ & 0.44 \\ & 0.44 \end{aligned}$ | V | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IL}} \text { or } \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{l}_{\mathrm{OL}}=12 \mathrm{~mA} \\ & \mathrm{l}_{\mathrm{OL}}=24 \mathrm{~mA} \\ & \mathrm{l}_{\mathrm{OL}}=24 \mathrm{~mA} \text { (Note 3) } \end{aligned}$ |
| $\overline{I_{\text {N }}(\text { Note 5）}}$ | Maximum Input Leakage Current | 5.5 |  | $\pm 0.1$ | $\pm 1.0$ | $\mu \mathrm{A}$ | $\mathrm{V}_{\mathrm{I}}=\mathrm{V}_{\text {CC }}$ ，GND |
| IoLD | Minimum Dynamic Output Current（Note 4） | 5.5 |  |  | 75 | mA | $\mathrm{V}_{\text {OLD }}=1.65 \mathrm{~V}$ Max |
| IOHD |  | 5.5 |  |  | －75 | mA | $\mathrm{V}_{\text {OHD }}=3.85 \mathrm{~V}$ Min |
| $\mathrm{I}_{\mathrm{Cc}}$ <br> （Note 5） | Maximum Quiescent Supply Current | 5.5 |  | 8.0 | 80.0 | $\mu \mathrm{A}$ | $\mathrm{V}_{\text {IN }}=\mathrm{V}_{\text {CC }}$ or GND |
| Iozt | Maximum I／O <br> Leakage Current <br> （ $\mathrm{A}_{\mathrm{n}}, \mathrm{B}_{\mathrm{n}}$ Inputs） | 5.5 |  | $\pm 0.6$ | $\pm 6.0$ | $\mu \mathrm{A}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{I}}(\mathrm{OE})=\mathrm{V}_{\mathrm{IL}}, \mathrm{~V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{CC}}, \mathrm{GND} \\ & \mathrm{~V}_{\mathrm{O}}=\mathrm{V}_{\mathrm{CC}}, \mathrm{GND} \end{aligned}$ |
| $\mathrm{V}_{\text {OLP }}$ | Quiet Output <br> Maximum Dynamic $\mathrm{V}_{\mathrm{OL}}$ | 5.0 | 1.1 | 1.5 |  | V | Figures 5， 6 <br> （Note 6）（Note 7） |


| DC Electrical Characteristics for ACQ（Continued） |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Symbol | Parameter | $\mathrm{V}_{\mathrm{cc}}$ <br> （V） | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | Units | Conditions |
|  |  |  | Typ | Guaranteed Limits |  |  |  |
| $\mathrm{V}_{\text {OLV }}$ | Quiet Output <br> Minimum Dynamic $\mathrm{V}_{\mathrm{OL}}$ | 5.0 | －0．6 | －1．2 |  | V | Figures 5， 6 （Note 6）（Note 7） |
| $\mathrm{V}_{\text {IHD }}$ | Minimum HIGH Level Dynamic Input Voltage | 5.0 | 3.1 | 3.5 |  | V | （Note 6）（Note 8） |
| $\mathrm{V}_{\text {ILD }}$ | Maximum LOW Level Dynamic Input Voltage | 5.0 | 1.9 | 1.5 |  | V | （Note 6）（Note 8） |

Note 4：Maximum test duration 2.0 ms ，one output loaded at a time．
Note 6：Plastic DIP package．
Note 7：Max number of outputs defined as（ n ）．Data inputs are driven OV to 5 V ．One output＠GND．
Note 8：Max number of Data Inputs（ $n$ ）switching．（ $n-1$ ）inputs switching 0 V to 5 V （ACQ）．Input－under－test switching 5 V to threshold（ $\mathrm{V}_{\mathrm{ILD}}$ ）， OV to threshold $\left(\mathrm{V}_{\mathrm{IHD}}\right) \mathrm{f}=1 \mathrm{MHz}$ ．

## DC Electrical Characteristics for ACTQ

| Symbol | Parameter | $\begin{aligned} & \hline \mathrm{V}_{\mathrm{cc}} \\ & (\mathrm{~V}) \end{aligned}$ | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | Units | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Typ | Guaranteed Limits |  |  |  |
| $\overline{\mathrm{V}_{\mathrm{IH}}}$ | Minimum HIGH Level Input Voltage | $\begin{aligned} & \hline 4.5 \\ & 5.5 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & \hline 2.0 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 2.0 \end{aligned}$ | V | $\begin{aligned} & \mathrm{V}_{\text {OUT }}=0.1 \mathrm{~V} \\ & \text { or } \mathrm{V}_{\mathrm{CC}}-0.1 \mathrm{~V} \end{aligned}$ |
| $\mathrm{V}_{\text {IL }}$ | Maximum LOW Level Input Voltage | $\begin{aligned} & 4.5 \\ & 5.5 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & 0.8 \\ & 0.8 \end{aligned}$ | $\begin{aligned} & \hline 0.8 \\ & 0.8 \end{aligned}$ | V | $\begin{aligned} & \mathrm{V}_{\text {OUT }}=0.1 \mathrm{~V} \\ & \text { or } \mathrm{V}_{\mathrm{CC}}-0.1 \mathrm{~V} \end{aligned}$ |
| $\overline{\mathrm{V}_{\mathrm{OH}}}$ | Minimum HIGH Level Output Voltage | $\begin{aligned} & 4.5 \\ & 5.5 \end{aligned}$ | $\begin{aligned} & 4.49 \\ & 5.49 \end{aligned}$ | $\begin{aligned} & 4.4 \\ & 5.4 \end{aligned}$ | $\begin{aligned} & \hline 4.4 \\ & 5.4 \end{aligned}$ | V | lout $=-50 \mu \mathrm{~A}$ |
|  |  | $\begin{aligned} & 4.5 \\ & 5.5 \end{aligned}$ |  | $\begin{aligned} & 3.86 \\ & 4.86 \end{aligned}$ | $\begin{aligned} & 3.76 \\ & 4.76 \end{aligned}$ | V | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IL}} \text { or } \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{I}_{\mathrm{OH}}=-24 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{OH}}=-24 \mathrm{~mA}(\text { Note } 9) \end{aligned}$ |
| $\mathrm{V}_{\mathrm{OL}}$ | Maximum LOW Level Output Voltage | $\begin{aligned} & 4.5 \\ & 5.5 \end{aligned}$ | $\begin{aligned} & \hline 0.001 \\ & 0.001 \end{aligned}$ | $\begin{aligned} & 0.1 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & \hline 0.1 \\ & 0.1 \end{aligned}$ | V | $\mathrm{l}_{\text {OUT }}=50 \mu \mathrm{~A}$ |
|  |  | $\begin{aligned} & 4.5 \\ & 5.5 \end{aligned}$ |  | $\begin{aligned} & 0.36 \\ & 0.36 \end{aligned}$ | $\begin{aligned} & 0.44 \\ & 0.44 \end{aligned}$ | V | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IL}} \text { or } \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{I}_{\mathrm{OL}}=24 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{OL}}=24 \mathrm{~mA}(\text { Note } 9) \end{aligned}$ |
| $\mathrm{I}_{\mathrm{N}}$ | Maximum Input Leakage Current | 5.5 |  | $\pm 0.1$ | $\pm 1.0$ | $\mu \mathrm{A}$ | $\mathrm{V}_{1}=\mathrm{V}_{\text {CC }}, \mathrm{GND}$ |
| Iozt | Maximum I／O Leakage Current （ $A_{n}, B_{n}$ Inputs） | 5.5 |  | $\pm 0.6$ | $\pm 6.0$ | $\mu \mathrm{A}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{I}}=\mathrm{V}_{\mathrm{IL}}, \mathrm{~V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{O}}=\mathrm{V}_{\mathrm{CC}}, \mathrm{GND} \end{aligned}$ |
| ${ }^{\text {CCT }}$ | Maximum I ${ }_{\text {cC }} /$ Input | 5.5 | 0.6 |  | 1.5 | mA | $\mathrm{V}_{1}=\mathrm{V}_{\mathrm{cc}}-2.1 \mathrm{~V}$ |
| lold | Minimum Dynamic Output Current（Note 10） | 5.5 |  |  | 75 | mA | $\mathrm{V}_{\text {OLD }}=1.65 \mathrm{~V}$ Max |
| ІОНD |  | 5.5 |  |  | －75 | mA | $\mathrm{V}_{\text {OHD }}=3.85 \mathrm{~V}$ Min |
| ${ }_{\text {ICC }}$ | Maximum Quiescent Supply Current | 5.5 |  | 8.0 | 80.0 | $\mu \mathrm{A}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{CC}} \\ & \text { or GND } \end{aligned}$ |
| $\mathrm{V}_{\text {OLP }}$ | Quiet Output <br> Maximum Dynamic $\mathrm{V}_{\mathrm{OL}}$ | 5.0 | 1.1 | 1.5 |  | V | Figures 5， 6 <br> （Note 11）（Note 12） |
| $\mathrm{V}_{\text {OLV }}$ | Quiet Output Minimum Dynamic $\mathrm{V}_{\mathrm{OL}}$ | 5.0 | －0．6 | －1．2 |  | V | Figures 5， 6 （Note 11）（Note 12） |
| $\mathrm{V}_{\text {IHD }}$ | Minimum HIGH Level Dynamic Input Voltage | 5.0 | 1.7 | 2.0 |  | V | （Note 11）（Note 13） |
| $\mathrm{V}_{\text {ILD }}$ | Maximum LOW Level Dynamic Input Voltage | 5.0 | 1.2 | 0.8 |  | V | （Note 11）（Note 13） |
| Note 9：All outputs loaded；thresholds on input associated with output under test． <br> Note 10：Maximum test duration 2.0 ms ，one output loaded at a time． <br> Note 11：Plastic DIP Package． <br> Note 12：Max number of outputs defined as（ n ）．Data inputs are driven 0 V to 3 V ．One output＠GND． <br> Note 13：Max number of data inputs（ $n$ ）switching．（ $n-1$ ）inputs switching $0 V$ to $3 V(A C T Q)$ ．Input－under－test switching： 3 V to threshold（ $\mathrm{V}_{\text {ILD }}$ ）， OV to threshold（ $\mathrm{V}_{\mathrm{IHD}}$ ）， $\mathrm{f}=1 \mathrm{MHz}$ ． |  |  |  |  |  |  |  |


| Symbol | Parameter | $\mathrm{V}_{\mathrm{Cc}}$ <br> (V) <br> (Note 14) | $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \end{aligned}$ |  |  | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \end{gathered}$ |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max | Min | Max |  |
| $\mathrm{t}_{\text {PLH }}$ | Propagation Delay Bus to Bus | $\begin{aligned} & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 3.5 \\ & 2.5 \end{aligned}$ | $\begin{aligned} & 9.0 \\ & 6.5 \end{aligned}$ | $\begin{gathered} 12.0 \\ 9.0 \end{gathered}$ | $\begin{aligned} & 3.5 \\ & 2.5 \end{aligned}$ | $\begin{gathered} 13.0 \\ 9.5 \end{gathered}$ | ns |
| $\mathrm{t}_{\text {PHL }}$ | Propagation Delay <br> Bus to Bus | $\begin{aligned} & \hline 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 3.5 \\ & 2.5 \end{aligned}$ | $\begin{aligned} & \hline 9.0 \\ & 6.5 \end{aligned}$ | $\begin{gathered} 12.0 \\ 9.0 \end{gathered}$ | $\begin{aligned} & 3.5 \\ & 2.5 \end{aligned}$ | $\begin{gathered} 13.0 \\ 9.5 \end{gathered}$ | ns |
| $\mathrm{t}_{\text {PLH }}$ | Propagation Delay Clock to Bus | $\begin{aligned} & \hline 3.3 \\ & 5.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline 3.5 \\ & 2.5 \end{aligned}$ | $\begin{gathered} 10.0 \\ 7.0 \end{gathered}$ | $\begin{gathered} \hline 13.0 \\ 9.5 \end{gathered}$ | $\begin{aligned} & 3.5 \\ & 2.5 \end{aligned}$ | $\begin{aligned} & 14.0 \\ & 10.5 \end{aligned}$ | ns |
| ${ }_{\text {teHL }}$ | Propagation Delay Clock to Bus | $\begin{aligned} & \hline 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 3.5 \\ & 2.5 \end{aligned}$ | $\begin{gathered} 10.0 \\ 7.0 \end{gathered}$ | $\begin{gathered} 13.0 \\ 9.5 \end{gathered}$ | $\begin{aligned} & 3.5 \\ & 2.5 \end{aligned}$ | $\begin{aligned} & 14.0 \\ & 10.5 \end{aligned}$ | ns |
| $\mathrm{t}_{\text {PLH }}$ | $\begin{aligned} & \text { Propagation Delay } \\ & \text { SBA or SAB to } A_{n} \text { or } B_{n} \\ & \left(w / A_{n} \text { or } B_{n} \text { HIGH or LOW }\right) \end{aligned}$ | $\begin{aligned} & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 3.5 \\ & 2.5 \end{aligned}$ | $\begin{aligned} & 9.5 \\ & 6.5 \end{aligned}$ | $\begin{gathered} 12.5 \\ 9.0 \end{gathered}$ | $\begin{aligned} & \hline 3.5 \\ & 2.5 \end{aligned}$ | $\begin{aligned} & 13.5 \\ & 10.0 \end{aligned}$ | ns |
| $\mathrm{t}_{\text {PHL }}$ | $\begin{aligned} & \text { Propagation Delay } \\ & \text { SBA or SAB to } A_{n} \text { or } B_{n} \\ & \left(w / A_{n} \text { or } B_{n} \text { HIGH or LOW }\right) \end{aligned}$ | $\begin{aligned} & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 3.5 \\ & 2.5 \end{aligned}$ | $\begin{aligned} & 9.5 \\ & 6.5 \end{aligned}$ | $\begin{gathered} 12.5 \\ 9.0 \end{gathered}$ | $\begin{aligned} & 3.5 \\ & 2.5 \end{aligned}$ | $\begin{aligned} & 13.5 \\ & 10.0 \end{aligned}$ | ns |
| $\overline{t_{\text {PZH }}}$ | Enable Time $\bar{G}$ to $A_{n}$ or $B_{n}$ | $\begin{aligned} & \hline 3.3 \\ & 5.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & 3.5 \\ & 2.5 \end{aligned}$ | $\begin{gathered} 10.5 \\ 8.0 \\ \hline \end{gathered}$ | $\begin{aligned} & 14.5 \\ & 10.5 \end{aligned}$ | $\begin{aligned} & 3.5 \\ & 2.5 \end{aligned}$ | $\begin{aligned} & 15.5 \\ & 11.5 \end{aligned}$ | ns |
| $\mathrm{t}_{\text {PZL }}$ | Enable Time $\bar{G}$ to $A_{n}$ or $B_{n}$ | $\begin{aligned} & \hline 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 3.5 \\ & 2.5 \end{aligned}$ | $\begin{gathered} 10.5 \\ 8.0 \end{gathered}$ | $\begin{aligned} & 14.5 \\ & 10.5 \end{aligned}$ | $\begin{aligned} & 3.5 \\ & 2.5 \end{aligned}$ | $\begin{aligned} & 15.5 \\ & 11.5 \end{aligned}$ | ns |
| $\mathrm{t}_{\text {PHZ }}$ | $\begin{aligned} & \text { Disable Time } \\ & \overline{\mathrm{G}} \text { to } \mathrm{A}_{\mathrm{n}} \text { or } \mathrm{B}_{\mathrm{n}} \end{aligned}$ | $\begin{aligned} & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 2.5 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & 8.0 \\ & 5.0 \end{aligned}$ | $\begin{gathered} 11.0 \\ 7.5 \end{gathered}$ | $\begin{aligned} & 2.5 \\ & 1.5 \end{aligned}$ | $\begin{gathered} 12.0 \\ 8.0 \end{gathered}$ | ns |
| $\mathrm{t}_{\text {PLZ }}$ | $\begin{aligned} & \text { Disable Time } \\ & \overline{\mathrm{G}} \text { to } \mathrm{A}_{\mathrm{n}} \text { or } \mathrm{B}_{\mathrm{n}} \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 2.5 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & \hline 8.0 \\ & 5.0 \\ & \hline \end{aligned}$ | $\begin{gathered} \hline 11.0 \\ 7.5 \\ \hline \end{gathered}$ | $\begin{aligned} & 2.5 \\ & 1.5 \end{aligned}$ | $\begin{gathered} \hline 12.0 \\ 8.0 \\ \hline \end{gathered}$ | ns |
| $\overline{t_{\text {PZH }}}$ | Enable Time DIR to $A_{n}$ or $B_{n}$ | $\begin{aligned} & \hline 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & \hline 4.5 \\ & 3.0 \end{aligned}$ | $\begin{gathered} 11.0 \\ 8.5 \end{gathered}$ | $\begin{aligned} & 15.5 \\ & 11.0 \end{aligned}$ | $\begin{aligned} & \hline 4.5 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & \hline 17.0 \\ & 11.5 \end{aligned}$ | ns |
| $\mathrm{t}_{\text {PZL }}$ | Enable Time DIR to $A_{n}$ or $B_{n}$ | $\begin{aligned} & \hline 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 4.5 \\ & 3.0 \end{aligned}$ | $\begin{gathered} 11.0 \\ 8.5 \end{gathered}$ | $\begin{aligned} & 15.5 \\ & 11.0 \end{aligned}$ | $\begin{aligned} & 4.5 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & \hline 17.0 \\ & 11.5 \end{aligned}$ | ns |
| $\mathrm{t}_{\text {PHZ }}$ | Disable Time DIR to $A_{n}$ or $B_{n}$ | $\begin{aligned} & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 8.0 \\ & 5.0 \end{aligned}$ | $\begin{gathered} 11.0 \\ 7.5 \end{gathered}$ | $\begin{aligned} & 1.5 \\ & 1.0 \end{aligned}$ | $\begin{gathered} 12.0 \\ 8.0 \end{gathered}$ | ns |
| $\mathrm{t}_{\text {PLZ }}$ | $\begin{array}{\|l\|} \hline \begin{array}{l} \text { Disable Time } \\ \text { DIR to } A_{n} \text { or } B_{n} \end{array} \\ \hline \end{array}$ | $\begin{aligned} & \hline 3.3 \\ & 5.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & \hline 8.0 \\ & 5.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline 11.0 \\ & 7.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.0 \end{aligned}$ | $\begin{gathered} \hline 12.0 \\ 8.0 \\ \hline \end{gathered}$ | ns |
| tos | Output to Output Skew (Note 15) | $\begin{aligned} & \hline 3.3 \\ & 5.0 \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 0.5 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.0 \end{aligned}$ |  | $\begin{aligned} & \hline 1.5 \\ & 1.0 \end{aligned}$ | ns |
| Note 14: Voltage Range 3.3 is $3.3 \mathrm{~V} \pm 0.3 \mathrm{~V}$. <br> Voltage Range 5.0 is $5.0 \mathrm{~V} \pm 0.5 \mathrm{~V}$ <br> Note 15: Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (toshL) or LOW-to-HIGH (tosLh). Parameter guaranteed by design. Not tested. <br> AC Operating Requirements for ACQ |  |  |  |  |  |  |  |  |
| Symbol | Parameter | $\mathrm{V}_{\mathrm{Cc}}$ <br> (Note 16) |  | $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |  | Units |
| $\mathrm{t}_{\mathrm{s}}$ | Setup Time, HIGH or LOW Bus to Clock | $\begin{aligned} & \hline 3.3 \\ & 5.0 \end{aligned}$ |  |  | $\begin{aligned} & \hline 3.0 \\ & 3.0 \end{aligned}$ |  |  | ns |
| $\mathrm{t}_{\mathrm{H}}$ | Hold Time, HIGH or LOW Bus to Clock |  |  |  | $\begin{aligned} & 1.5 \\ & 1.5 \end{aligned}$ |  |  | ns |
| $\mathrm{t}_{\mathrm{W}}$ | Clock Pulse Width HIGH or LOW |  |  |  | $\begin{aligned} & 4.0 \\ & 4.0 \end{aligned}$ |  |  | ns |
| Note 16: Voltage Range 5.0 is $5.0 \mathrm{~V} \pm 0.5 \mathrm{~V}$ Voltage Range 3.3 is $3.3 \mathrm{~V} \pm 0.3 \mathrm{~V}$ |  |  |  |  |  |  |  |  |



## FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests．The following is a brief description of the setup used to measure the noise characteristics of FACT．
Equipment：
Hewlett Packard Model 8180A Word Generator
PC－163A Test Fixture
Tektronics Model 7854 Oscilloscope
Procedure：
1．Verify Test Fixture Loading：Standard Load 50 pF ， $500 \Omega$ ．
2．Deskew the HFS generator so that no two channels have greater than 150 ps skew between them．This requires that the oscilloscope be deskewed first．It is important to deskew the HFS generator channels before testing．This will ensure that the outputs switch simultaneously．

3．Terminate all inputs and outputs to ensure proper load－ ing of the outputs and that the input levels are at the correct voltage．
4．Set the HFS generator to toggle all but one output at a frequency of 1 MHz ．Greater frequencies will increase DUT heating and effect the results of the measure－ ment

5．Set the HFS generator input levels at OV LOW and 3 V HIGH for ACT devices and OV LOW and 5V HIGH for AC devices．Verify levels with an oscilloscope．


FIGURE 5．Quiet Output Noise Voltage Waveforms Note 20： $\mathrm{V}_{\mathrm{OHV}}$ and $\mathrm{V}_{\text {OLP }}$ are measured with respect to ground reference． Note 21：Input pulses have the following characteristics：$f=1 \mathrm{MHz}$ ， $\mathrm{t}_{\mathrm{r}}=3 \mathrm{~ns}, \mathrm{t}_{\mathrm{f}}=3 \mathrm{~ns}$ ，skew＜ 150 ps ．
$\mathrm{V}_{\mathrm{OLP}} / \mathrm{V}_{\mathrm{OLV}}$ and $\mathrm{V}_{\mathrm{OHP}} / \mathrm{V}_{\mathrm{OHV}}$ ：
－Determine the quiet output pin that demonstrates the greatest noise levels．The worst case pin will usually be the furthest from the ground pin．Monitor the output volt－ ages using a $50 \Omega$ coaxial cable plugged into a standard SMB type connector on the test fixture．Do not use an active FET probe．
－Measure $\mathrm{V}_{\text {OLP }}$ and $\mathrm{V}_{\text {OLV }}$ on the quiet output during the worst case transition for active and enable．Measure $\mathrm{V}_{\mathrm{OHP}}$ and $\mathrm{V}_{\mathrm{OHV}}$ on the quiet output during the worst case active and enable transition．
－Verify that the GND reference recorded on the oscillo－ scope has not drifted to ensure the accuracy and repeat－ ability of the measurements．
$V_{\text {ILD }}$ and $V_{\text {IHD }}$ ：
－Monitor one of the switching outputs using a $50 \Omega$ coaxial cable plugged into a standard SMB type connector on the test fixture．Do not use an active FET probe．
－First increase the input LOW voltage level， $\mathrm{V}_{\mathrm{IL}}$ ，until the output begins to oscillate or steps out a min of 2 ns ． Oscillation is defined as noise on the output LOW level that exceeds $\mathrm{V}_{\text {IL }}$ limits，or on output HIGH levels that exceed $\mathrm{V}_{\mathrm{IH}}$ limits．The input LOW voltage level at which oscillation occurs is defined as $\mathrm{V}_{\text {ILD }}$
－Next decrease the input HIGH voltage level， $\mathrm{V}_{\mathrm{IH}}$ ，until the output begins to oscillate or steps out a min of 2 ns ． Oscillation is defined as noise on the output LOW level that exceeds $\mathrm{V}_{\text {IL }}$ limits，or on output HIGH levels that exceed $\mathrm{V}_{\mathrm{IH}}$ limits．The input HIGH voltage level at which oscillation occurs is defined as $\mathrm{V}_{\mathrm{IHD}}$ ．
－Verify that the GND reference recorded on the oscillo－ scope has not drifted to ensure the accuracy and repeat－ ability of the measurements．


FIGURE 6．Simultaneous Switching Test Circuit
Physical Dimensions inches (millimeters) unless otherwise noted



