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November 2013

FQP50N06L

N-Channel QFET[®] MOSFET 60 V, 52.4 A, 21 m Ω

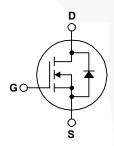
Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- 52.4 A, 60 V, $R_{DS(on)}$ = 21 m Ω (Max.) @ V_{GS} = 10 V, I_D = 26.2 A
- Low Gate Charge (Typ. 24.5 nC)
- Low Crss (Typ. 90 pF)
- · 100% Avalanche Tested
- · 175°C Maximum Junction Temperature Rating





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FQP50N06L	Unit	
V_{DSS}	Drain-Source Voltage		60	V	
I _D	Drain Current - Continuous (T _C = 25°	C)	52.4	А	
	- Continuous (T _C = 100	°C)	37.1	А	
I _{DM}	Drain Current - Pulsed	(Note 1)	210	Α	
V _{GSS}	Gate-Source Voltage		± 20	V	
E _{AS}	Single Pulsed Avalanche Energy	(Note 2)	990	mJ	
I _{AR}	Avalanche Current	(Note 1)	52.4	Α	
E _{AR}	Repetitive Avalanche Energy	(Note 1)	12.1	mJ	
dv/dt	Peak Diode Recovery dv/dt (Note 3)		7.0	V/ns	
P_{D}	Power Dissipation (T _C = 25°C)		121	W	
	- Derate above 25°C		0.81	W/°C	
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +175	°C	
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds		300	°C	

Thermal Characteristics

Symbol	Parameter	FQP50N06L	Unit	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	1.24	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	°C/W	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP50N06L	FQP50N06L	TO-220	Tube	N/A	N/A	50 units

Symbol	Parameter	Parameter Test Conditions		Тур	Max	Unit
Off Cha	aracteristics					
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	60			V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		0.06		V/°C
I _{DSS}	Zoro Coto Voltago Drain Current	V _{DS} = 60 V, V _{GS} = 0 V			1	μΑ
	Zero Gate Voltage Drain Current	V _{DS} = 48 V, T _C = 150°C			10	μΑ
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 20 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -20 V, V _{DS} = 0 V			-100	nA
On Cha	aracteristics					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.0		2.5	V
R _{DS(on)}	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 26.2 \text{ A}$ $V_{GS} = 5 \text{ V}, I_D = 26.2 \text{ A}$		0.017 0.020	0.021 0.025	Ω
9 _{FS}	Forward Transconductance $V_{DS} = 25 \text{ V}, I_D = 26.2 \text{ A}$			40		S
Dvnam	ic Characteristics					
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V,		1250	1630	pF
C _{oss}	Output Capacitance	f = 1.0 MHz		445	580	pF
C _{rss}	Reverse Transfer Capacitance			90	120	pF
Switchi	ing Characteristics					
t _{d(on)}	Turn-On Delay Time	V _{DD} = 30 V, I _D = 26.2 A,		20	50	ns
t _r	Turn-On Rise Time	$V_{DD} = 30 \text{ V}, I_{D} = 20.2 \text{ A},$ $R_{G} = 25 \Omega$		380	770	ns
t _{d(off)}	Turn-Off Delay Time	116 - 20 22		80	170	ns
t _f	Turn-Off Fall Time	(Note 4)	/	145	300	ns
Qg	Total Gate Charge	V _{DS} = 48 V, I _D = 52.4 A,	- 4-	24.5	32	nC
Q _{gs}	Gate-Source Charge	V _{GS} = 5 V	A	6		nC
^	0 / 5 / 0/	- ³⁰				-

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current		 	52.4	Α
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		 	210	Α
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 52.4 A	 	1.5	V
t _{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_{S} = 52.4 \text{ A},$	 65		ns
Q _{rr}	Reverse Recovery Charge	$dI_F / dt = 100 A/\mu s$	 125		nC

 Q_{gd}

- **Notes:** 1. Repetitive Rating : Pulse width limited by maximum junction temperature. 2. L = 300 μ H, I_{AS} = 52.4 A, V_{DD} = 25 V, R_G = 25 Ω , starting T_J = 25°C. 3. I_{SD} \leq 52.4 A, di/dt \leq 300 λ / μ s, V_{DD} \leq BV_{DSS}, starting T_J = 25°C. 4. Essentially independent of operating temperature.

Gate-Drain Charge

nC

14.5

Typical Characteristics

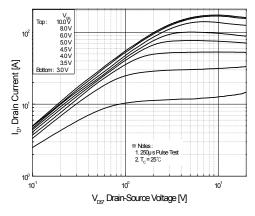


Figure 1. On-Region Characteristics

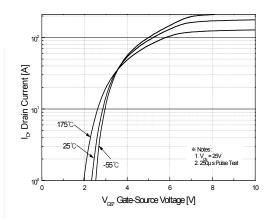


Figure 2. Transfer Characteristics

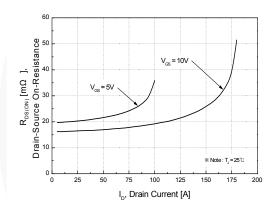


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

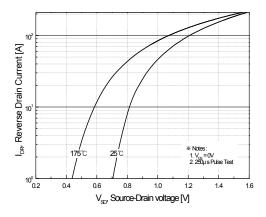


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

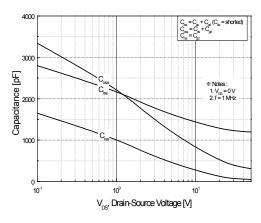


Figure 5. Capacitance Characteristics

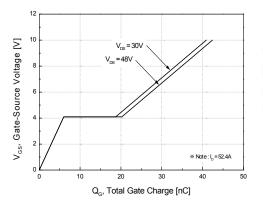


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

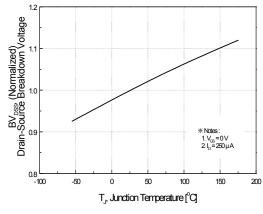


Figure 7. Breakdown Voltage Variation vs. Temperature

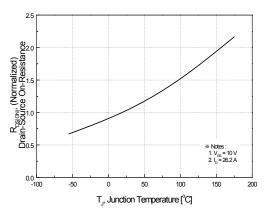


Figure 8. On-Resistance Variation vs. Temperature

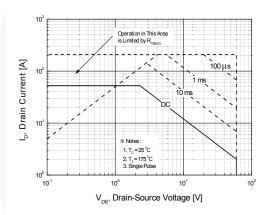


Figure 9. Maximum Safe Operating Area

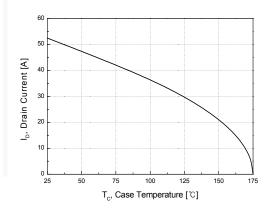


Figure 10. Maximum Drain Current vs. Case Temperature

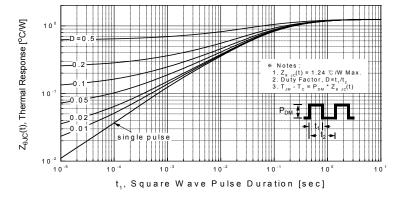


Figure 11. Transient Thermal Response Curve

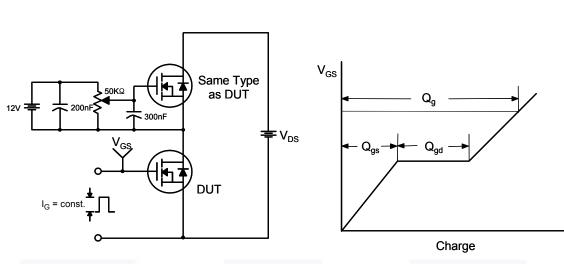


Figure 12. Gate Charge Test Circuit & Waveform

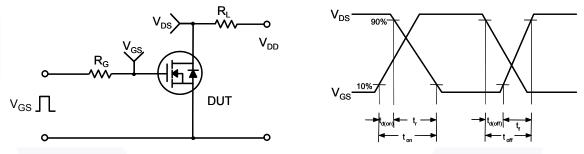


Figure 13. Resistive Switching Test Circuit & Waveforms

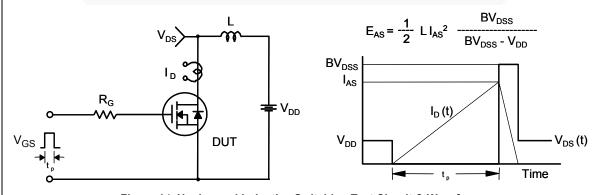
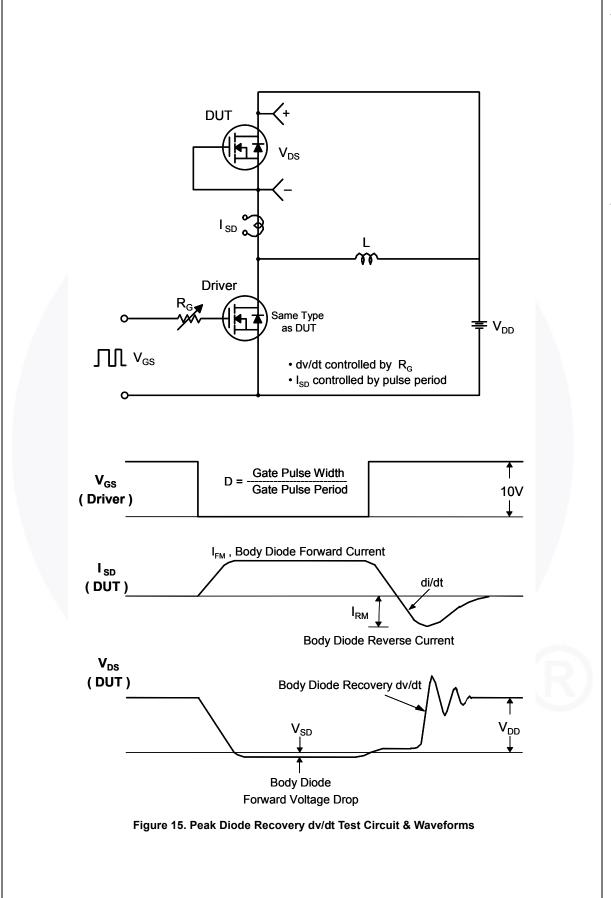


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Mechanical Dimensions

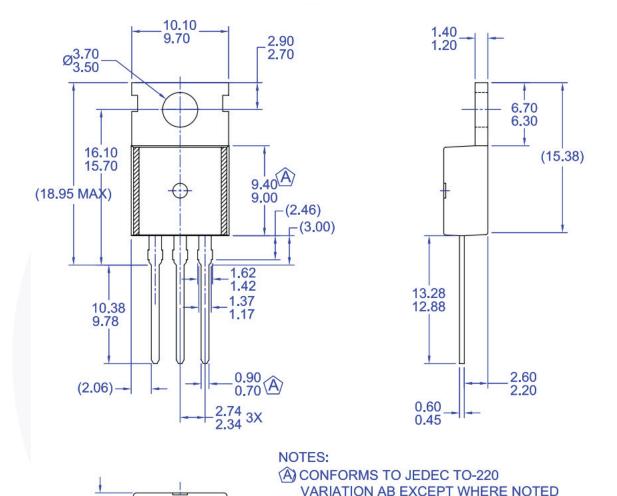


Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D) DRAWING FILE/REVISION: MKT-TO220Y03REV1

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10.20

9.80

4.70

4.30





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