

**32M-WORD BY 72-BIT SYNCHRONOUS DYNAMIC RAM MODULE  
UNBUFFERED TYPE****Description**

The MC-4532CC727XFA is 33,554,432 words by 72 bits synchronous dynamic RAM module on which 18 pieces of 128M SDRAM:  $\mu$ PD45128841 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

**Features**

- 33,554,432 words by 72 bits organization (ECC type)
- Clock frequency and access time from CLK.

| Part number         | /CAS latency | Clock frequency<br>(MAX.) | Access time from CLK<br>(MAX.) |
|---------------------|--------------|---------------------------|--------------------------------|
| MC-4532CC727XFA-A75 | CL = 3       | 133 MHz                   | 5.4 ns                         |
|                     | CL = 2       | 100 MHz                   | 6.0 ns                         |

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Quad internal banks controlled by BA0 and BA1 (Bank Select)
- Programmable burst-length (1, 2, 4, 8 and full page)
- Programmable wrap sequence (Sequential / Interleave)
- Programmable /CAS latency (2, 3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- All DQs have  $10\ \Omega \pm 10\%$  of series resistor
- Single 3.3 V  $\pm 0.3$  V power supply
- LVTTTL compatible
- 4,096 refresh cycles/64 ms
- Burst termination by Burst Stop command and Precharge command
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Unbuffered type
- Serial PD

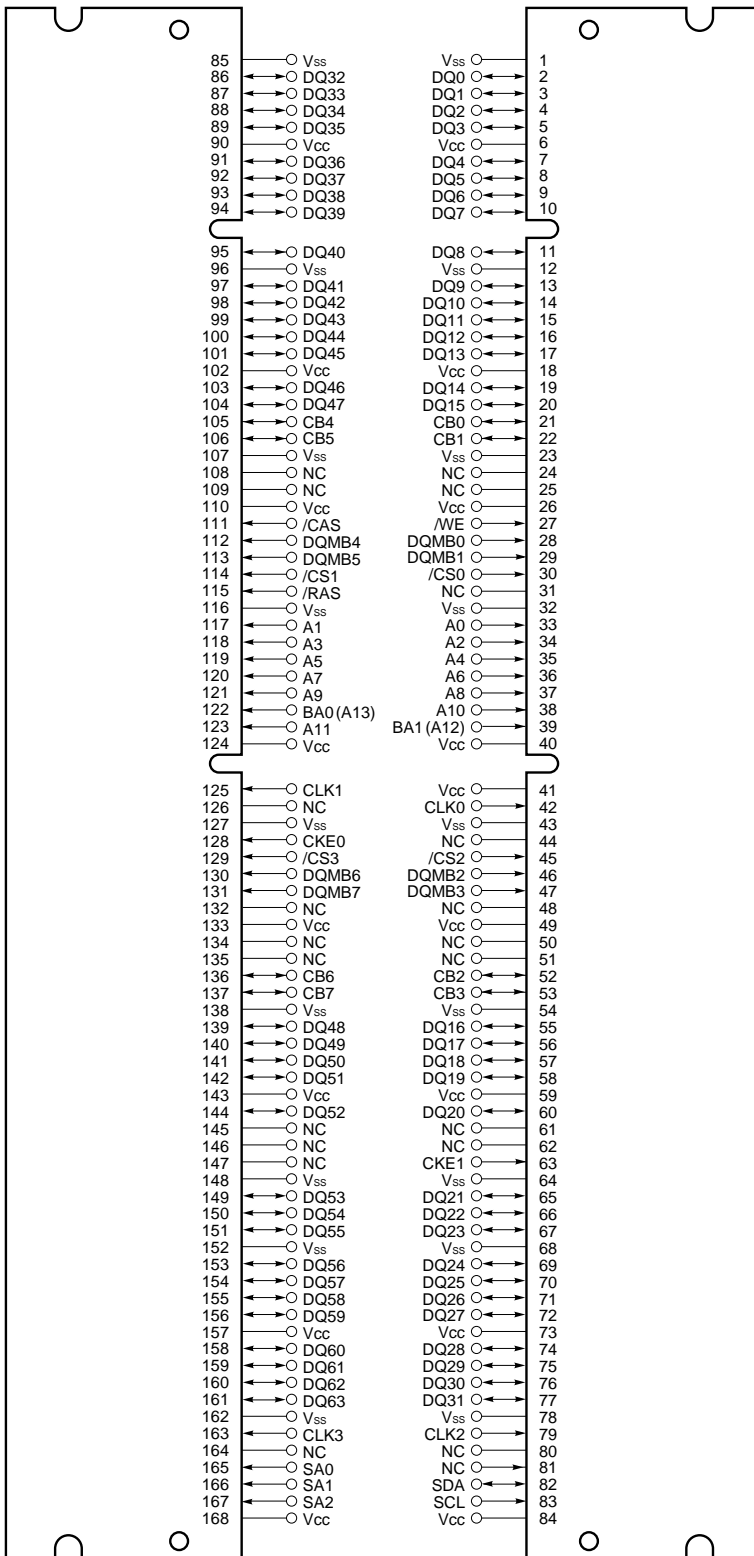
**The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.  
Not all devices/types available in every country. Please check with local Elpida Memory, Inc. for availability and additional information.**

## Ordering Information

| Part number         | Clock frequency<br>(MAX.) | Package  | Mounted devices  |
|---------------------|---------------------------|--|--|
| MC-4532CC727XFA-A75 | 133 MHz                   | 168-pin Dual In-line Memory Module<br>(Socket Type)<br>Edge connector : Gold plated<br>34.93 mm height | 18 pieces of $\mu$ PD45128841G5 (Rev. X)<br>(10.16 mm (400) TSOP (II)) |

Pin Configuration

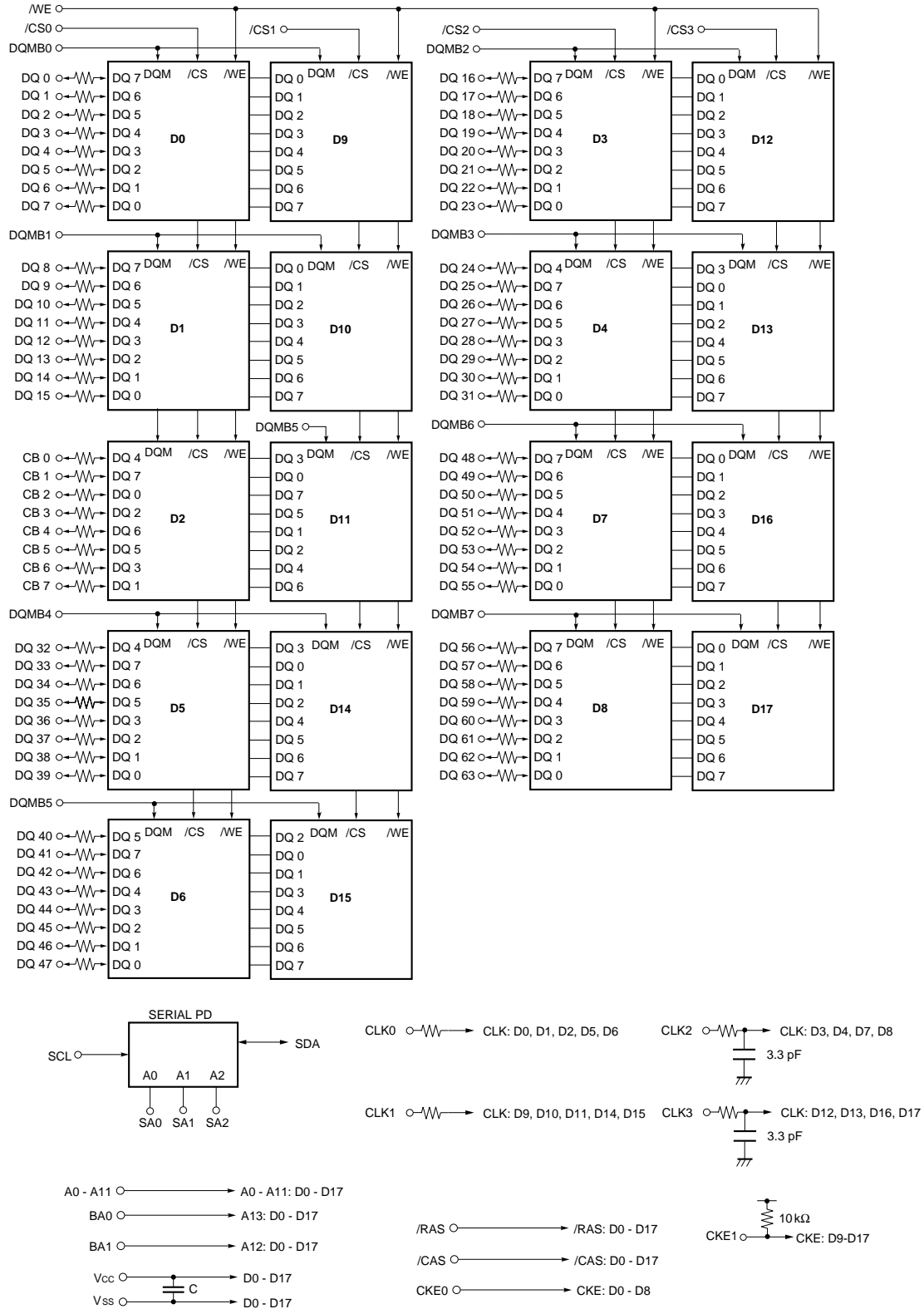
168-pin Dual In-line Memory Module Socket Type (Edge connector: Gold plated)



/xxx indicates active low signal.

- A0 - A11 : Address Inputs
- [Row: A0 - A11, Column: A0 - A9]
- BA0 (A13), BA1 (A12) : SDRAM Bank Select
- DQ0 - DQ63, CB0 - CB7 : Data Inputs/Outputs
- CLK0 - CLK3 : Clock Input
- CKE0, CKE1 : Clock Enable Input
- /CS0 - /CS3 : Chip Select Input
- /RAS : Row Address Strobe
- /CAS : Column Address Strobe
- /WE : Write Enable
- DQMB0 - DQMB7 : DQ Mask Enable
- SA0 - SA2 : Address Input for EEPROM
- SDA : Serial Data I/O for PD
- SCL : Clock Input for PD
- Vcc : Power Supply
- Vss : Ground
- NC : No Connection

Block Diagram



- Remarks**
- The value of all resistors is 10 Ω except CKE1.
  - D0 - D17:  $\mu$ PD45128841 (4M words  $\times$  8 bits  $\times$  4 banks)

### Electrical Specifications

- All voltages are referenced to  $V_{SS}$  (GND).
- After power up, wait more than 100  $\mu s$  and then, execute power on sequence and CBR (Auto) refresh before proper device operation is achieved.

### Absolute Maximum Ratings

| Parameter                                   | Symbol    | Condition | Rating       | Unit |
|---|-----------|-----------|--------------|------|
| Voltage on power supply pin relative to GND | $V_{CC}$  |           | -0.5 to +4.6 | V    |
| Voltage on input pin relative to GND        | $V_T$     |           | -0.5 to +4.6 | V    |
| Short circuit output current                | $I_O$     |           | 50           | mA   |
| Power dissipation                           | $P_D$     |           | 18           | W    |
| Operating ambient temperature               | $T_A$     |           | 0 to 70      | °C   |
| Storage temperature                         | $T_{stg}$ |           | -55 to +125  | °C   |

**Caution** Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

### Recommended Operating Conditions

| Parameter                     | Symbol   | Condition | MIN. | TYP. | MAX.           | Unit |
|-------------------------------|----------|-----------|------|------|----------------|------|
| Supply voltage                | $V_{CC}$ |           | 3.0  | 3.3  | 3.6            | V    |
| High level input voltage      | $V_{IH}$ |           | 2.0  |      | $V_{CC} + 0.3$ | V    |
| Low level input voltage       | $V_{IL}$ |           | -0.3 |      | +0.8           | V    |
| Operating ambient temperature | $T_A$    |           | 0    |      | 70             | °C   |

### Capacitance ( $T_A = 25\text{ °C}$ , $f = 1\text{ MHz}$ )

| Parameter                     | Symbol    | Test condition                                  | MIN. | TYP. | MAX. | Unit |
|-------------------------------|-----------|---|------|------|------|------|
| Input capacitance             | $C_{I1}$  | A0 - A11, BA0 (A13), BA1 (A12), /RAS, /CAS, /WE | 40   |      | 80   | pF   |
|                               | $C_{I2}$  | CLK0 - CLK3                                     | 20   |      | 40   |      |
|                               | $C_{I3}$  | CKE0, CKE1                                      | 30   |      | 56   |      |
|                               | $C_{I4}$  | /CS0 - /CS3                                     | 15   |      | 33   |      |
|                               | $C_{I5}$  | DQMB0 - DQMB7                                   | 5    |      | 21   |      |
| Data input/output capacitance | $C_{I/O}$ | DQ0 - DQ63, CB0 - CB7                           | 7    |      | 19   | pF   |

## DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

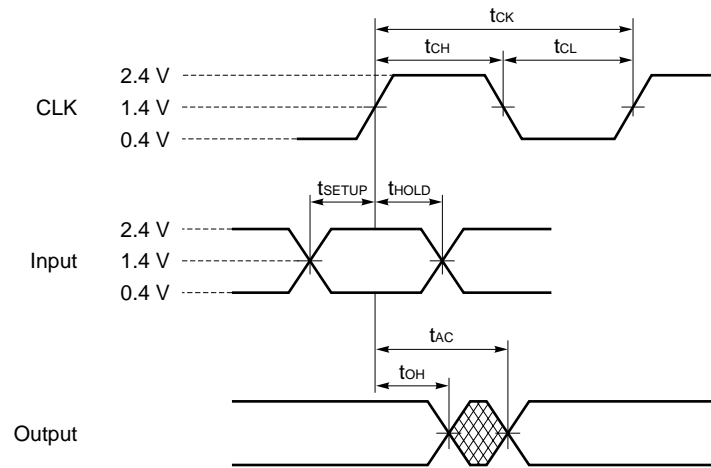
| Parameter  | Symbol             | Test condition   | -A75             |       | Unit | Notes |
|--|--------------------|--|------------------|-------|------|-------|
|  |                    |  | MIN.             | MAX.  |      |       |
| Operating current                                | I <sub>CC1</sub>   | Burst length = 1<br>t <sub>RC</sub> ≥ t <sub>RC(MIN.)</sub> , I <sub>O</sub> = 0 mA  | /CAS latency = 2 | 1,170 | mA   | 1     |
|  |                    |  | /CAS latency = 3 | 1,215 |      |       |
| Precharge standby current in power down mode     | I <sub>CC2P</sub>  | CKE ≤ V <sub>IL(MAX.)</sub> , t <sub>CK</sub> = 15 ns  |                  | 18    | mA   |       |
|  | I <sub>CC2PS</sub> | CKE ≤ V <sub>IL(MAX.)</sub> , t <sub>CK</sub> = ∞  |                  | 18    |      |       |
| Precharge standby current in non power down mode | I <sub>CC2N</sub>  | CKE ≥ V <sub>IH(MIN.)</sub> , t <sub>CK</sub> = 15 ns, /CS ≥ V <sub>IH(MIN.)</sub> ,<br>Input signals are changed one time during 30 ns. |                  | 360   | mA   |       |
|  | I <sub>CC2NS</sub> | CKE ≥ V <sub>IH(MIN.)</sub> , t <sub>CK</sub> = ∞ Input signals are stable.  |                  | 144   |      |       |
| Active standby current in power down mode        | I <sub>CC3P</sub>  | CKE ≤ V <sub>IL(MAX.)</sub> , t <sub>CK</sub> = 15 ns  |                  | 90    | mA   |       |
|  | I <sub>CC3PS</sub> | CKE ≤ V <sub>IL(MAX.)</sub> , t <sub>CK</sub> = ∞  |                  | 72    |      |       |
| Active standby current in non power down mode    | I <sub>CC3N</sub>  | CKE ≥ V <sub>IH(MIN.)</sub> , t <sub>CK</sub> = 15 ns, /CS ≥ V <sub>IH(MIN.)</sub> ,<br>Input signals are changed one time during 30 ns. |                  | 540   | mA   |       |
|  | I <sub>CC3NS</sub> | CKE ≥ V <sub>IH(MIN.)</sub> , t <sub>CK</sub> = ∞, Input signals are stable.   |                  | 360   |      |       |
| Operating current (Burst mode)                   | I <sub>CC4</sub>   | t <sub>CK</sub> ≥ t <sub>CK(MIN.)</sub><br>I <sub>O</sub> = 0 mA   | /CAS latency = 2 | 1,350 | mA   | 2     |
|  |                    |  | /CAS latency = 3 | 1,665 |      |       |
| CBR (Auto) refresh current                       | I <sub>CC5</sub>   | t <sub>RC</sub> ≥ t <sub>RC(MIN.)</sub>  | /CAS latency = 2 | 2,340 | mA   | 3     |
|  |                    |  | /CAS latency = 3 | 2,430 |      |       |
| Self refresh current                             | I <sub>CC6</sub>   | CKE ≤ 0.2 V  |                  | 36    | mA   |       |
| Input leakage current                            | I <sub>I(L)</sub>  | V <sub>I</sub> = 0 to 3.6 V, All other pins not under test = 0 V   |                  | -18   | +18  | μA    |
|  |                    |  | CKE1             | -500  |      |       |
| Output leakage current                           | I <sub>O(L)</sub>  | D <sub>OUT</sub> is disabled, V <sub>O</sub> = 0 to 3.6 V  |                  | -3    | +3   | μA    |
| High level output voltage                        | V <sub>OH</sub>    | I <sub>O</sub> = -4.0 mA   |                  | 2.4   |      | V     |
| Low level output voltage                         | V <sub>OL</sub>    | I <sub>O</sub> = +4.0 mA   |                  |       | 0.4  | V     |

- Notes**
1. I<sub>CC1</sub> depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I<sub>CC1</sub> is measured on condition that addresses are changed only one time during t<sub>CK(MIN.)</sub>.
  2. I<sub>CC4</sub> depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I<sub>CC4</sub> is measured on condition that addresses are changed only one time during t<sub>CK(MIN.)</sub>.
  3. I<sub>CC5</sub> is measured on condition that addresses are changed only one time during t<sub>CK(MIN.)</sub>.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Test Conditions

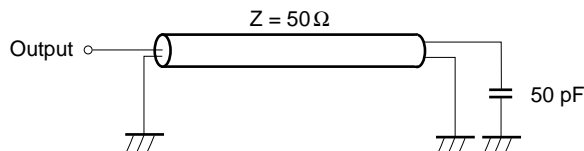
| Parameter   | Value     | Unit |
|---|-----------|------|
| AC high level input voltage / low level input voltage | 2.4 / 0.4 | V    |
| Input timing measurement reference level              | 1.4       | V    |
| Transition time (Input rise and fall time)            | 1         | ns   |
| Output timing measurement reference level             | 1.4       | V    |



Synchronous Characteristics

| Parameter  |                  | Symbol            | -A75 |           | Unit | Note |
|--|------------------|-------------------|------|-----------|------|------|
|  |                  |                   | MIN. | MAX.      |      |      |
| Clock cycle time   | /CAS latency = 3 | t <sub>CK3</sub>  | 7.5  | (133 MHz) | ns   |      |
|  | /CAS latency = 2 | t <sub>CK2</sub>  | 10   | (100 MHz) | ns   |      |
| Access time from CLK   | /CAS latency = 3 | t <sub>AC3</sub>  |      | 5.4       | ns   | 1    |
|  | /CAS latency = 2 | t <sub>AC2</sub>  |      | 6.0       | ns   | 1    |
| CLK high level width   |                  | t <sub>CH</sub>   | 2.5  |           | ns   |      |
| CLK low level width  |                  | t <sub>CL</sub>   | 2.5  |           | ns   |      |
| Data-out hold time   |                  | t <sub>OH</sub>   | 3.0  |           | ns   | 1    |
| Data-out low-impedance time                                      |                  | t <sub>LZ</sub>   | 0    |           | ns   |      |
| Data-out high-impedance time                                     | /CAS latency = 3 | t <sub>HZ3</sub>  | 3.0  | 5.4       | ns   |      |
|  | /CAS latency = 2 | t <sub>HZ2</sub>  | 3.0  | 6.0       | ns   |      |
| Data-in setup time   |                  | t <sub>DS</sub>   | 1.5  |           | ns   |      |
| Data-in hold time  |                  | t <sub>DH</sub>   | 0.8  |           | ns   |      |
| Address setup time   |                  | t <sub>AS</sub>   | 1.5  |           | ns   |      |
| Address hold time  |                  | t <sub>AH</sub>   | 0.8  |           | ns   |      |
| CKE setup time   |                  | t <sub>CKS</sub>  | 1.5  |           | ns   |      |
| CKE hold time  |                  | t <sub>CKH</sub>  | 0.8  |           | ns   |      |
| CKE setup time (Power down exit)                                 |                  | t <sub>CKSP</sub> | 1.5  |           | ns   |      |
| Command (/CS0 - /CS3, /RAS, /CAS, /WE, DQMB0 - DQMB7) setup time |                  | t <sub>CMS</sub>  | 1.5  |           | ns   |      |
| Command (/CS0 - /CS3, /RAS, /CAS, /WE, DQMB0 - DQMB7) hold time  |                  | t <sub>CMH</sub>  | 0.8  |           | ns   |      |

**Note 1.** Output load



**Remark** These specifications are applied to the monolithic device.



## Asynchronous Characteristics

| Parameter   | Symbol           | -A75              |           | Unit | Note |
|---|------------------|-------------------|-----------|------|------|
|   |                  | MIN.              | MAX.      |      |      |
| ACT to REF/ACT command period (operation)           | t <sub>RC</sub>  | 67.5              |           | ns   |      |
| REF to REF/ACT command period (refresh)             | t <sub>RC1</sub> | 67.5              |           | ns   |      |
| ACT to PRE command period                           | t <sub>RAS</sub> | 45                | 120,000   | ns   |      |
| PRE to ACT command period                           | t <sub>RP</sub>  | 20                |           | ns   |      |
| Delay time ACT to READ/WRITE command                | t <sub>RCD</sub> | 20                |           | ns   |      |
| ACT(one) to ACT(another) command period             | t <sub>RRD</sub> | 15                |           | ns   |      |
| Data-in to PRE command period                       | t <sub>DPL</sub> | 8                 |           | ns   |      |
| Data-in to ACT(REF) command period (Auto precharge) | /CAS latency = 3 | t <sub>DAL3</sub> | 1CLK+22.5 | ns   | 1    |
|   | /CAS latency = 2 | t <sub>DAL2</sub> | 1CLK+20   | ns   | 1    |
| Mode register set cycle time                        | t <sub>RSC</sub> | 2                 |           | CLK  |      |
| Transition time                                     | t <sub>r</sub>   | 0.5               | 30        | ns   |      |
| Refresh time (4,096 refresh cycles)                 | t <sub>REF</sub> |                   | 64        | ms   |      |

**Note** This device can satisfy the t<sub>DAL3</sub> spec of 1CLK+20 ns for up to and including 125 MHz operation.

## Serial PD

(1/2)

| Byte No. | Function Described  | Hex | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Notes         |
|----------|---|-----|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| 0        | Defines the number of bytes written into serial PD memory | 80H | 1     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 128 bytes     |
| 1        | Total number of bytes of serial PD memory                 | 08H | 0     | 0     | 0     | 0     | 1     | 0     | 0     | 0     | 256 bytes     |
| 2        | Fundamental memory type                                   | 04H | 0     | 0     | 0     | 0     | 0     | 1     | 0     | 0     | SDRAM         |
| 3        | Number of rows  | 0CH | 0     | 0     | 0     | 0     | 1     | 1     | 0     | 0     | 12 rows       |
| 4        | Number of columns   | 0AH | 0     | 0     | 0     | 0     | 1     | 0     | 1     | 0     | 10 columns    |
| 5        | Number of banks   | 02H | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 0     | 2 banks       |
| 6        | Data width  | 48H | 0     | 1     | 0     | 0     | 1     | 0     | 0     | 0     | 72 bits       |
| 7        | Data width (continued)                                    | 00H | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0             |
| 8        | Voltage interface   | 01H | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1     | LVTTTL        |
| 9        | CL = 3 Cycle time   | 75H | 0     | 1     | 1     | 1     | 0     | 1     | 0     | 1     | 7.5 ns        |
| 10       | CL =3 Access time   | 54H | 0     | 1     | 0     | 1     | 0     | 1     | 0     | 0     | 5.4 ns        |
| 11       | DIMM configuration type                                   | 02H | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 0     | ECC           |
| 12       | Refresh rate/type   | 80H | 1     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | Normal        |
| 13       | SDRAM width   | 08H | 0     | 0     | 0     | 0     | 1     | 0     | 0     | 0     | ×8            |
| 14       | Error checking SDRAM width                                | 08H | 0     | 0     | 0     | 0     | 1     | 0     | 0     | 0     | ×8            |
| 15       | Minimum clock delay                                       | 01H | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1 clock       |
| 16       | Burst length supported                                    | 8FH | 1     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 1, 2, 4, 8, F |
| 17       | Number of banks on each SDRAM                             | 04H | 0     | 0     | 0     | 0     | 0     | 1     | 0     | 0     | 4 banks       |
| 18       | /CAS latency supported                                    | 06H | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0     | 2, 3          |
| 19       | /CS latency supported                                     | 01H | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 0             |
| 20       | /WE latency supported                                     | 01H | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 0             |
| 21       | SDRAM module attributes                                   | 00H | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |               |
| 22       | SDRAM device attributes : General                         | 0EH | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 0     |               |
| 23       | CL = 2 Cycle time   | A0H | 1     | 0     | 1     | 0     | 0     | 0     | 0     | 0     | 10 ns         |
| 24       | CL = 2 Access time  | 60H | 0     | 1     | 1     | 0     | 0     | 0     | 0     | 0     | 6 ns          |
| 25-26    |   | 00H | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |               |
| 27       | t <sub>RP</sub> (MIN.)                                    | 14H | 0     | 0     | 0     | 1     | 0     | 1     | 0     | 0     | 20 ns         |
| 28       | t <sub>RRD</sub> (MIN.)                                   | 0FH | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 15 ns         |
| 29       | t <sub>RCD</sub> (MIN.)                                   | 14H | 0     | 0     | 0     | 1     | 0     | 1     | 0     | 0     | 20 ns         |
| 30       | t <sub>RAS</sub> (MIN.)                                   | 2DH | 0     | 0     | 1     | 0     | 1     | 1     | 0     | 1     | 45 ns         |
| 31       | Module bank density                                       | 20H | 0     | 0     | 1     | 0     | 0     | 0     | 0     | 0     | 128M bytes    |
| 32       | Command and address signal input setup time               | 15H | 0     | 0     | 0     | 1     | 0     | 1     | 0     | 1     | 1.5 ns        |
| 33       | Command and address signal input hold time                | 08H | 0     | 0     | 0     | 0     | 1     | 0     | 0     | 0     | 0.8 ns        |
| 34       | Data signal input setup time                              | 15H | 0     | 0     | 0     | 1     | 0     | 1     | 0     | 1     | 1.5 ns        |
| 35       | Data signal input hold time                               | 08H | 0     | 0     | 0     | 0     | 1     | 0     | 0     | 0     | 0.8 ns        |
| 36-61    |   | 00H | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |               |
| 62       | SPD revision  | 12H | 0     | 0     | 0     | 1     | 0     | 0     | 1     | 0     | 1.2           |
| 63       | Checksum for bytes 0 - 62                                 | C2H | 1     | 1     | 0     | 0     | 0     | 0     | 1     | 0     |               |
| 64       | Manufacture's JEDEC ID code                               | 10H | 0     | 0     | 0     | 1     | 0     | 0     | 0     | 0     | NEC           |

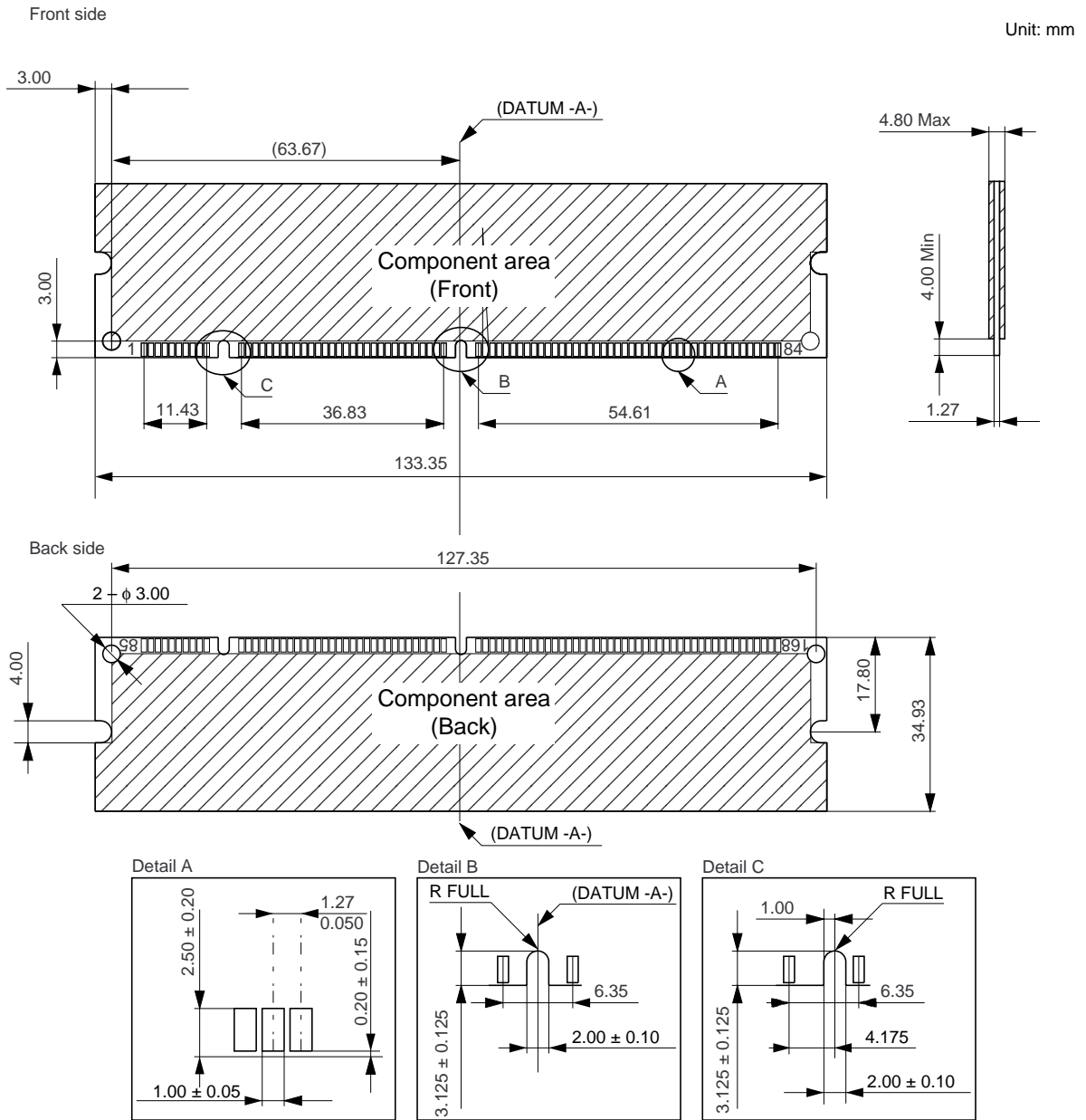
(2/2)

| Byte No. | Function Described                       | Hex | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Notes  |
|----------|--|-----|-------|-------|-------|-------|-------|-------|-------|-------|--------|
| 65-71    | Manufacture's JEDEC ID code              |     |       |       |       |       |       |       |       |       |        |
| 72       | Manufacturing location                   |     |       |       |       |       |       |       |       |       |        |
| 73-90    | Manufacture's P/N                        |     |       |       |       |       |       |       |       |       |        |
| 91-92    | Revision code                            |     |       |       |       |       |       |       |       |       |        |
| 93-94    | Manufacturing date                       |     |       |       |       |       |       |       |       |       |        |
| 95-98    | Assembly serial number                   |     |       |       |       |       |       |       |       |       |        |
| 99-125   | Mfg specific                             |     |       |       |       |       |       |       |       |       |        |
| 126      | Intel specification frequency            | 64H | 0     | 1     | 1     | 0     | 0     | 1     | 0     | 0     | 100MHz |
| 127      | Intel specification /CAS latency support | FFH | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     |        |

**Timing Chart**

Refer to the **μPD45128441, 45128841, 45128163 Data sheet (E0031N)**.

Package Drawing



Note: Tolerance on all dimensions  $\pm$  0.15 unless otherwise specified.

ECA-TS2-0049-01

**CAUTION FOR HANDLING MEMORY MODULES**

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory ICs, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

In particular, do not push module cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

When re-packing memory modules, be sure the modules are not touching each other.

Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

MDE0202

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR MOS DEVICES**

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES**

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

The information in this document is subject to change without notice. Before using this document, confirm that this is the latest version.

No part of this document may be copied or reproduced in any form or by any means without the prior written consent of Elpida Memory, Inc.

Elpida Memory, Inc. does not assume any liability for infringement of any intellectual property rights (including but not limited to patents, copyrights, and circuit layout licenses) of Elpida Memory, Inc. or third parties by or arising from the use of the products or information listed in this document. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of Elpida Memory, Inc. or others.

Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of the customer's equipment shall be done under the full responsibility of the customer. Elpida Memory, Inc. assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.

**[Product applications]**

Elpida Memory, Inc. makes every attempt to ensure that its products are of high quality and reliability. However, users are instructed to contact Elpida Memory's sales office before using the product in aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment, medical equipment for life support, or other such application in which especially high quality and reliability is demanded or where its failure or malfunction may directly threaten human life or cause risk of bodily injury.

**[Product usage]**

Design your application so that the product is used within the ranges and conditions guaranteed by Elpida Memory, Inc., including the maximum ratings, operating supply voltage range, heat radiation characteristics, installation conditions and other related characteristics. Elpida Memory, Inc. bears no responsibility for failure or damage when the product is used beyond the guaranteed ranges and conditions. Even within the guaranteed ranges and conditions, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Elpida Memory, Inc. products does not cause bodily injury, fire or other consequential damage due to the operation of the Elpida Memory, Inc. product.

**[Usage environment]**

This product is not designed to be resistant to electromagnetic waves or radiation. This product must be used in a non-condensing environment.

If you export the products or technology described in this document that are controlled by the Foreign Exchange and Foreign Trade Law of Japan, you must follow the necessary procedures in accordance with the relevant laws and regulations of Japan. Also, if you export products/technology controlled by U.S. export control regulations, or another country's export control laws or regulations, you must follow the necessary procedures in accordance with such laws or regulations.

If these products/technology are sold, leased, or transferred to a third party, or a third party is granted license to use these products, that third party must be made aware that they are responsible for compliance with the relevant laws and regulations.