

## GENERAL DESCRIPTION

OB2273 is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications.

PWM switching frequency at normal operation is internally fixed and is trimmed to tight range. At no load or light load condition, the IC operates in extended 'burst mode' to minimize switching loss. Lower standby power and higher conversion efficiency is thus achieved.

VDD low startup current and low operating current contribute to a reliable power on startup and low standby design with OB2273.

OB2273 offers complete protection coverage with auto-recovery including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), and VDD under voltage lockout (UVLO). It also provides the protections with latched shut down including over temperature protection (OTP), and over voltage (fixed or adjustable) protection (OVP). Excellent EMI performance is achieved with On-Bright proprietary frequency shuffling technique.

The tone energy at below 20KHZ is minimized in the design and audio noise is eliminated during operation.

OB2273 is offered in SOT23-6 and DIP-8 package.

## FEATURES

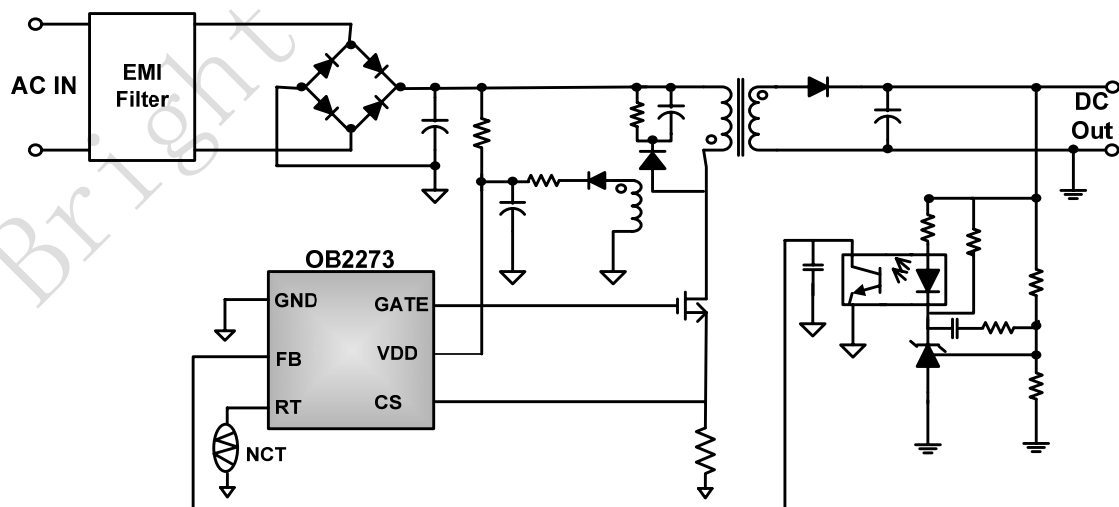
- Power on Soft Start Reducing MOSFET Vds Stress
- Frequency shuffling for EMI
- Extended Burst Mode Control For Improved Efficiency and Minimum Standby Power Design
- Audio Noise Free Operation
- Fixed 65KHZ Switching Frequency
- Comprehensive Protection Coverage
  - VDD Under Voltage Lockout with Hysteresis (UVLO)
  - Cycle-by-cycle over current threshold setting for constant output power limiting over universal input voltage range
  - Overload Protection (OLP) with auto-recovery
  - Over Temperature Protection (OTP) with latch shut down
  - VDD Over voltage Protection(OVP) with latch shut down
  - Adjustable OVP through external Zener

## APPLICATIONS

Offline AC/DC flyback converter for

- Battery Charger
- Power Adapter
- Set-Top Box Power Supplies
- Open-frame SMPS

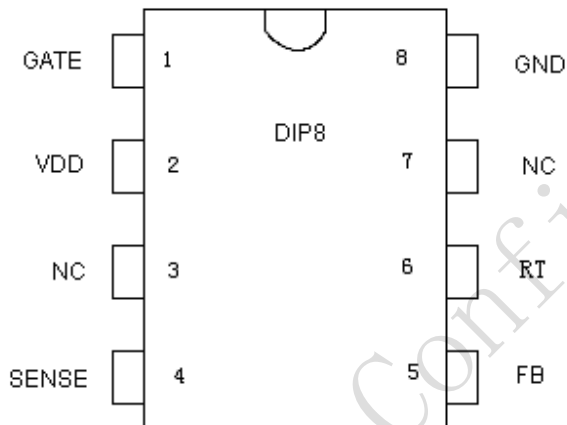
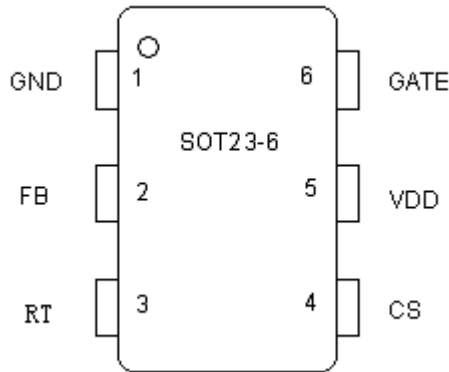
## TYPICAL APPLICATION



### GENERAL INFORMATION

#### Pin Configuration

The OB2273 is offered in SOT23-6 and DIP8 package, shown as below.



#### Ordering Information

Part Number	Description
OB2273MP	SOT23-6, Pb-free in T&R
OB2273AP	DIP8, Pb-free in Tube

#### Package Dissipation Rating

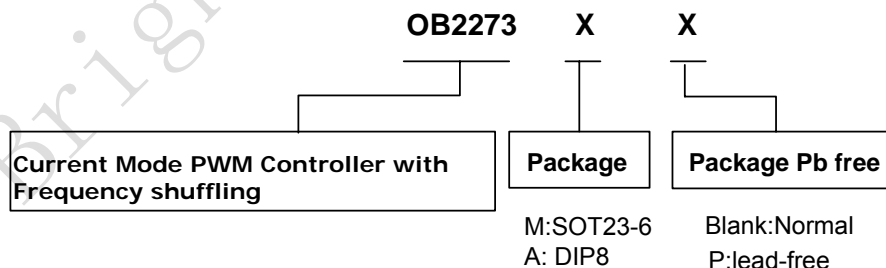
Package	R $\theta$ JA(°C/W)
SOT23-6	200
DIP8	90

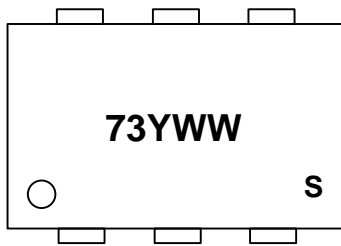
#### Absolute Maximum Ratings

Parameter	Value
VDD DC Supply Voltage	30 V
VDD Zener Clamp Voltage <sup>Note</sup>	VDD_Clamp+0.1V
VDD DC Clamp Current	10 mA
FB Input Voltage	-0.3 to 7V
Sense Input Voltage	-0.3 to 7V
RT Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature T <sub>J</sub>	-40 to 150 °C
Min/Max Storage Temperature T <sub>stg</sub>	-55 to 160 °C
Lead Temperature (Soldering, 10secs)	260 °C

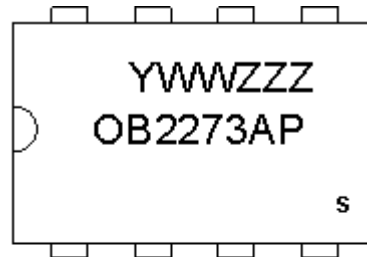
**Note:** VDD\_Clamp has a nominal value of 32V.

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.



**Marking Information**


Y:Year Code  
 WW:Week Code(01-52)  
 S:Internal Code(Optional)



Y:Year Code  
 WW:Week Code(01-52)  
 ZZZ:Lot Code  
 A:DIP8 Package  
 P:Pb-free Package  
 S:Internal Code(Optional)

**TERMINAL ASSIGNMENTS**

Pin Name	I/O	Description
GND	P	Ground
FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at Pin 4.
RT	I	Dual function pin. Either connected through a NTC resistor to ground for over temperature shutdown/latch control or connected through Zener to VDD for adjustable over voltage protection
CS	I	Current sense input
VDD	P	Power Supply
Gate	O	Totem-pole gate driver output for power Mosfet

**RECOMMENDED OPERATING CONDITION**

Symbol	Parameter	Min/Max	Unit
VDD	VDD Supply Voltage	12 to 25	V
T <sub>A</sub>	Operating Ambient Temperature	-40 to 85	°C



**ELECTRICAL CHARACTERISTICS**

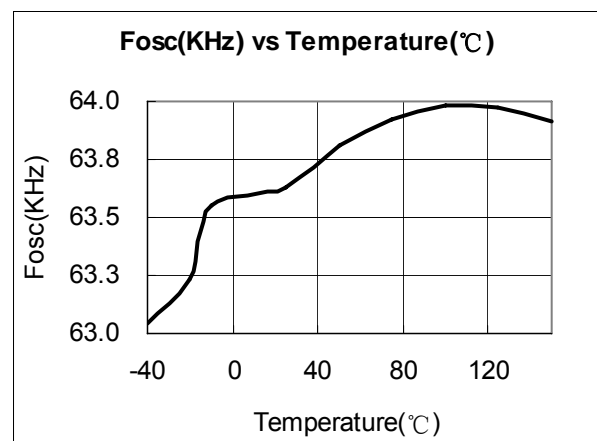
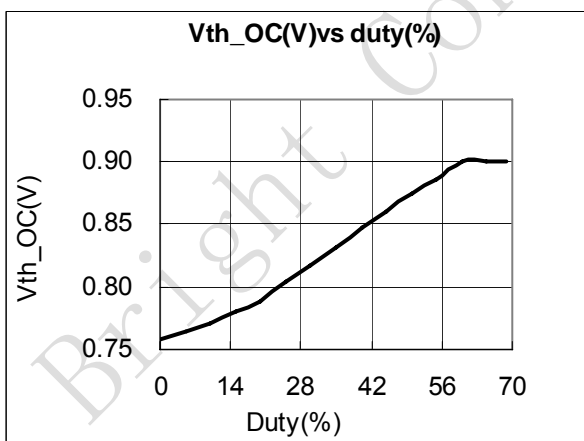
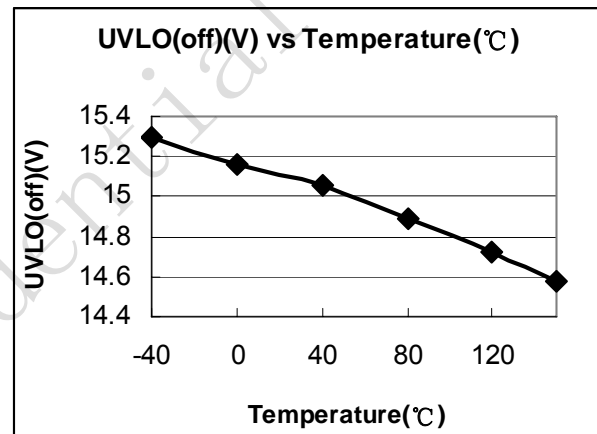
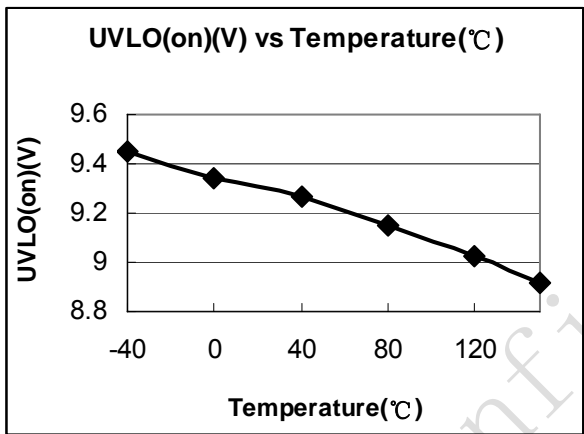
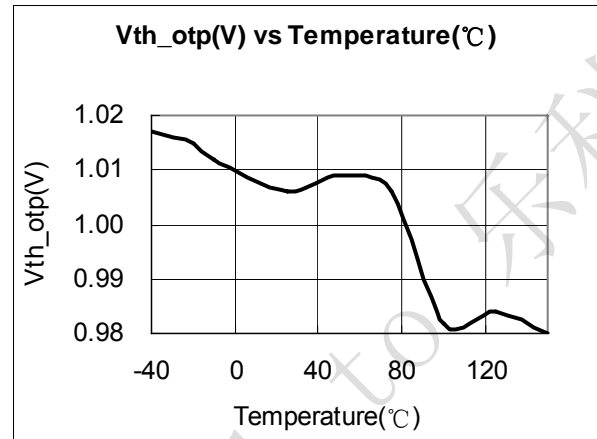
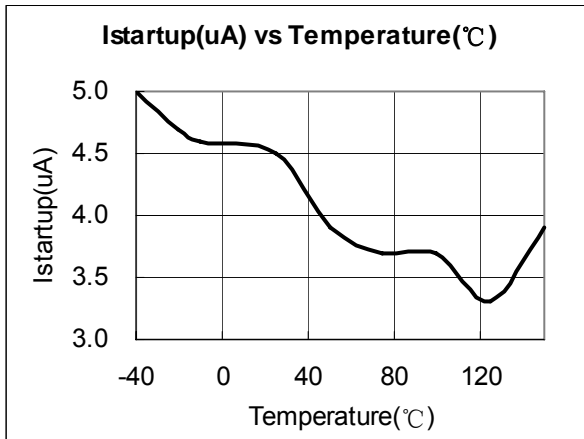
 (T<sub>A</sub> = 25°C, VDD=18V, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Supply Voltage (VDD)</b>						
I <sub>startup</sub>	VDD Start up Current	VDD=UVLO(OFF)-1V, measure leakage current into VDD		5	20	uA
I <sub>VDD_Operation</sub>	Operation Current	VDD=18V, V <sub>FB</sub> =3V, CS=0V, C <sub>gate</sub> =1nF		1.8	2.5	mA
UVLO(ON)	VDD Under Voltage Lockout Enter		8	9	10	V
UVLO(OFF)	VDD Under Voltage Lockout Exit (Recovery)		14.3	15.3	16.3	V
V <sub>pull-up</sub>	Pull-up PMOS active			13		V
V <sub>dd_clamp</sub>		I <sub>vdd</sub> =10mA	30	32	34	V
OVP(ON)	Over voltage protection voltage	CS=0V, FB=3V Ramp up VDD until gate clock is off	26	28	30	V
V <sub>latch_release</sub>	Latch release voltage			5		V
<b>Feedback Input Section(FB Pin)</b>						
V <sub>FB_Open</sub>	V <sub>FB</sub> Open Loop Voltage		3.9	4.2		V
A <sub>vcs</sub>	PWM input gain $\Delta V_{FB}/\Delta V_{CS}$			2		V/V
Maximum duty cycle	Max duty cycle @ VDD=18V, V <sub>FB</sub> =3V, V <sub>CS</sub> =0V		75	80	85	%
V <sub>ref_green</sub>	The threshold enter green mode			2		V
V <sub>ref_burst_H</sub>	The threshold exit burst mode			1.275		V
V <sub>ref_burst_L</sub>	The threshold enter burst mode			1.175		V
I <sub>FB_Short</sub>	FB pin short circuit current	Short FB pin to GND and measure current		0.4		mA
V <sub>TH_PL</sub>	Power Limiting FB Threshold Voltage			3.7		V
T <sub>D_PL</sub>	Power limiting Debounce Time		80	88	96	mSec
Z <sub>FB_IN</sub>	Input Impedance			16		Kohm
<b>Current Sense Input(CS Pin)</b>						
SST	Soft start time			4		ms
T <sub>blanking</sub>	Leading edge blanking time			220		ns
Z <sub>SENSE_IN</sub>	Input Impedance			40		Kohm
T <sub>D_OC</sub>	Over Current Detection and Control Delay	From Over Current Occurs till the Gatedrive output start to turn off		120		nSec
V <sub>TH_OC</sub>	Internal Current Limiting Threshold Voltage with zero duty cycle			0.75		V
V <sub>ocp_clamping</sub>	CS voltage clamber			0.9		V
<b>Oscillator</b>						
F <sub>osc</sub>	Normal Oscillation Frequency	VDD=18V, FB=3V, CS=0V	60	65	70	KHZ
$\Delta f_{OSC}$	Frequency jittering			+/-4		%
F <sub>shuffling</sub>	Shuffling frequency			32		Hz

$\Delta f_{Temp}$	Frequency Temperature Stability			1		%
$\Delta f_{VDD}$	Frequency Voltage Stability			1		%
F_Burst	Burst Mode Switch Frequency			22		KHZ
<b>Gate driver</b>						
VOL	Output low level @ VDD=18V, I <sub>o</sub> =5mA				1	V
VOH	Output high level @ VDD=18V, I <sub>o</sub> =20mA		6			V
V_clamping	Output clamp voltage			12		V
T <sub>r</sub>	Output rising time 1V ~ 12V @ CL=1000pF			175		nS
T <sub>f</sub>	Output falling time 12V ~ 1V @ CL=1000pF			85		nS
<b>Over temperature protection</b>						
IRT	Output current of RT pin		95	100	105	uA
VOTP	Threshold voltage for OTP		0.95	1	1.05	V
Td_OTP	OTP debounce time			32		Cycle
VRT_FL	Float voltage at RT pin			2.3		V
Vth_OVP	External OVP threshold voltage			4		V

**CHARACTERIZATION PLOTS**

VDD = 18V, TA = 25°C condition applies if not otherwise noted.



## OPERATION DESCRIPTION

OB2273 is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications. The 'Extended burst mode' control greatly reduces the standby power consumption and helps the design easily to meet the international power conservation requirements.

- **Startup Current and Start up Control**

Startup current of OB2273 is designed to be very low so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application.

- **Operating Current**

The Operating current of OB2273 is low at 1.8mA. Good efficiency is achieved with OB2273 low operating current together with the 'Extended burst mode' control features.

- **Soft Start**

OB2273 features an internal 4ms soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VDD reaches UVLO(OFF), the CS peak voltage is gradually increased from 0.05V to the maximum level. Every restart up is followed by a soft start.

- **Frequency shuffling for EMI improvement**

The frequency Shuffling (switching frequency modulation) is implemented in OB2273. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

- **Extended Burst Mode Operation**

At light load or zero load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.

The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below

Vref\_burst\_L (the threshold enter burst mode) and device enters Burst Mode control. The Gate drive output switches when FB input rises back to Vref\_burst\_H (the threshold exit burst mode). Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.

The switching frequency control also eliminates the audio noise at any loading conditions.

- **Oscillator Operation**

The switching frequency is internally fixed at 65KHZ. No external frequency setting components are required for PCB design simplification.

- **Current Sensing and Leading Edge Blanking**

Cycle-by-Cycle current limiting is offered in OB2273 current mode PWM control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of power MOSFET. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

- **Internal Synchronized Slope Compensation**

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

- **Drive**

The power MOSFET is driven by a dedicated gate driver for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive results the compromise of EMI.

A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

- **Protection Controls**

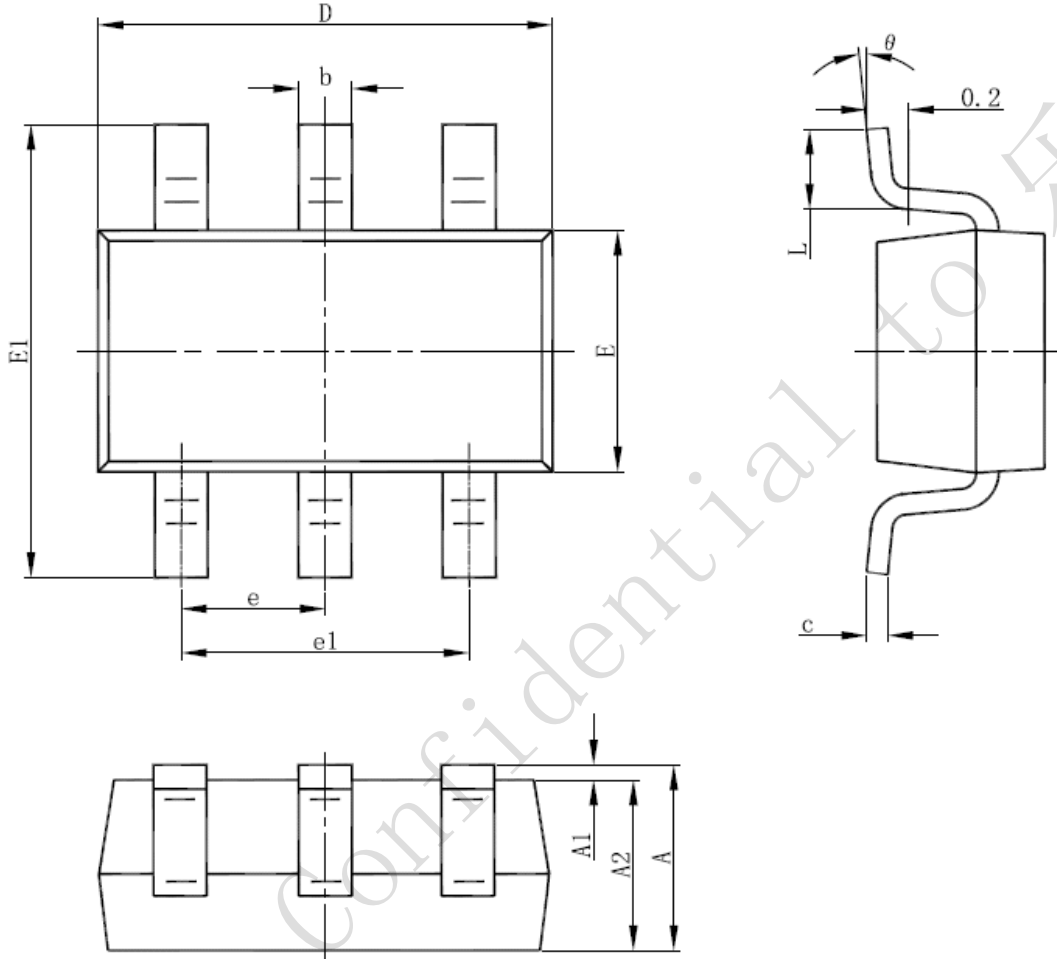


Good power supply system reliability is achieved with auto-recovery protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP), and Under Voltage Lockout on VDD (UVLO), and latch shutdown features including over temperature protection (OTP), fixed or adjustable VDD over voltage protection (OVP). With On-Bright Proprietary technology, the OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range.

At overload condition when FB input voltage exceeds power limit threshold value for more than TD\_PL, control circuit reacts to shut down the converter. It restarts when VDD voltage drops below UVLO limit. For protection with latch shut down mode, control circuit shutdowns (latch) the power MOSFET when an Over Temperature condition or Over Voltage condition is detected until VDD drops below 5V (Latch release voltage), and device enters power on restart-up sequence thereafter.

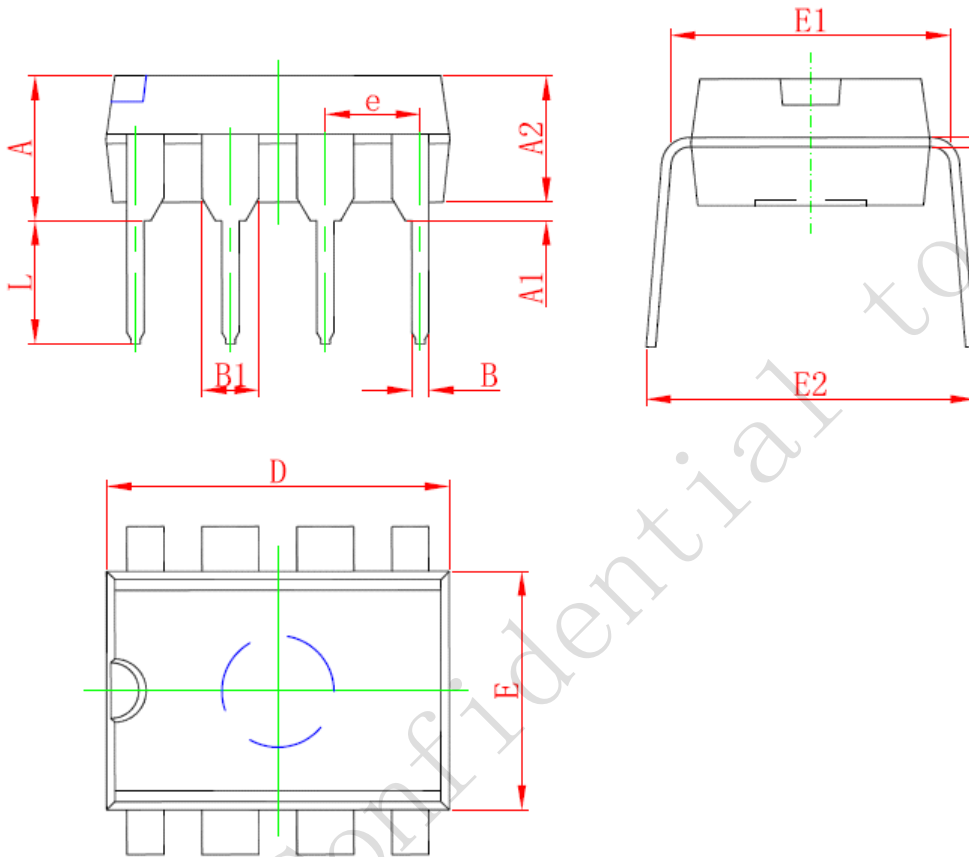
**PACKAGE MECHANICAL DATA**

**SOT-23-6L PACKAGE OUTLINE DIMENSIONS**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.300	0.039	0.051
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.800	3.020	0.110	0.119
E	1.500	1.700	0.059	0.067
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
theta	0°	8°	0°	8°

**DIP8 PACKAGE OUTLINE DIMENSIONS**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	5.334	0.146	0.210
A1	0.381		0.015	
A2	2.921	4.953	0.115	0.195
B	0.350	0.650	0.014	0.026
B1	1.524 (BSC)		0.06 (BSC)	
C	0.200	0.360	0.008	0.014
D	9.000	10.160	0.354	0.400
E	6.096	7.112	0.240	0.280
E1	7.320	8.255	0.288	0.325
e	2.540 (BSC)		0.1 (BSC)	
L	2.921	3.810	0.115	0.150
E2	7.620	10.920	0.300	0.430

## IMPORTANT NOTICE

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