## FEATURES

Complete monolithic resolver-to-digital converter $\mathbf{3 1 2 5}$ rps maximum tracking rate (10-bit resolution) $\pm 2.5$ arc minutes of accuracy
10-/12-/14-/16-bit resolution, set by user
Parallel and serial 10-bit to 16-bit data ports
Absolute position and velocity outputs
System fault detection
Programmable fault detection thresholds
Differential inputs
Incremental encoder emulation
Programmable sinusoidal oscillator on board
Compatible with DSP and SPI interface standards
5 V supply with 2.3 V to 5 V logic interface
Support defense and aerospace applications (AQEC)
Military temperature range ( $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ )
Controlled manufacturing baseline
One assembly/test site
One fabrication site
Enhanced product change notification
Qualification data available upon request

## APPLICATIONS

DC and ac servo motor control
Encoder emulation
Electric power steering
Electric vehicles
Integrated starter generators/alternators
Automotive motion sensing and control

## GENERAL DESCRIPTION

The AD2S1210-EP is a complete 10-bit to 16-bit resolution tracking resolver-to-digital converter, integrating an on-board programmable sinusoidal oscillator that provides sine wave excitation for resolvers.
The converter accepts $3.15 \mathrm{~V} \mathrm{p}-\mathrm{p} \pm 27 \%$ input signals, in the range of 2 kHz to 20 kHz on the sine and cosine inputs. A Type II servo loop is employed to track the inputs and convert the input sine and cosine information into a digital representation of the input angle and velocity. The maximum tracking rate is 3125 rps .
Full details about this enhanced product, including theory of operation, registers details, and applications information, are available in the AD2S1210 data sheet, which should be concluded in conjunction with this data sheet.

## Rev. 0

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Figure 1.

## PRODUCT HIGHLIGHTS

1. Ratiometric tracking conversion. The Type II tracking loop provides continuous output position data without conversion delay. It also provides noise immunity and tolerance of harmonic distortion on the reference and input signals.
2. System fault detection. A fault detection circuit can sense loss of resolver signals, out-of-range input signals, input signal mismatch, or loss of position tracking. The fault detection threshold levels can be individually programmed by the user for optimization within a particular application.
3. Input signal range. The sine and cosine inputs can accept differential input voltages of $3.15 \mathrm{~V} p-\mathrm{p} \pm 27 \%$.
4. Programmable excitation frequency. Excitation frequency is easily programmable to a number of standard frequencies between 2 kHz and 20 kHz .
5. Triple format position data. Absolute 10 -bit to 16 -bit angular position data is accessed via either a 16 -bit parallel port or a 4 -wire serial interface. Incremental encoder emulation is in standard A-quad-B format with direction output available.
6. Digital velocity output. 10-bit to 16 -bit signed digital velocity accessed via either a 16-bit parallel port or a 4 -wire serial interface.

## AD2S1210-EP

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## REVISION HISTORY

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## SPECIFICATIONS

$\mathrm{AV}_{\mathrm{DD}}=\mathrm{DV}_{\mathrm{DD}}=5.0 \mathrm{~V} \pm 5 \%, \mathrm{CLKIN}=8.192 \mathrm{MHz} \pm 25 \%$, $\mathrm{EXC}, \mathrm{EXC}$ frequency $=10 \mathrm{kHz}$ to 20 kHz (10-bit); 6 kHz to 20 kHz (12-bit); 3 kHz to 12 kHz (14-bit); 2 kHz to 10 kHz (16-bit); $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\mathrm{MAX}}$; unless otherwise noted. ${ }^{1}$

Table 1.

| Parameter | Min | Typ | Max | Unit | Conditions/Comments |
| :---: | :---: | :---: | :---: | :---: | :---: |
| SINE, COSINE INPUTS ${ }^{2}$ |  |  |  |  |  |
| Voltage Amplitude | 2.3 | 3.15 | 4.0 | $V \mathrm{p}-\mathrm{p}$ | Sinusoidal waveforms, differential SIN to SINLO, COS to COSLO |
| Input Bias Current |  |  | 8.25 | $\mu \mathrm{A}$ | $\mathrm{V}_{\mathrm{IN}}=4.0 \mathrm{~V}$ p-p, CLKIN $=8.192 \mathrm{MHz}$ |
| Input Impedance | 485 |  |  | $k \Omega$ | $\mathrm{V}_{\mathrm{IN}}=4.0 \mathrm{~V}$ p-p, CLKIN $=8.192 \mathrm{MHz}$ |
| Phase Lock Range | -44 |  | +44 | Degrees | Sine/cosine vs. EXC output, Control Register D3 $=0$ |
| Common-Mode Rejection | $\pm 20$ |  |  | arc sec/V | 10 Hz to 1 MHz , Control Register D4 $=0$ |
| ANGULAR ACCURACY ${ }^{3}$ |  |  |  |  |  |
| Angular Accuracy |  | $\pm 2.5+1 \text { LSB }$ | $\pm 7+1$ LSB | arc min | No missing codes |
| Resolution |  | $10,12,14,16$ |  | Bits |  |
| Linearity INL |  |  |  |  |  |  |
| 10-bit |  |  | $\pm 1$ | LSB |  |
| 12-bit |  |  | $\pm 2$ | LSB |  |
| 14-bit |  |  | $\pm 4$ | LSB |  |
| 16-bit |  |  | $\pm 16$ | LSB |  |
| Linearity DNL |  |  | $\pm 0.9$ | LSB |  |
| Repeatability |  | $\pm 1$ |  | LSB |  |
| VELOCITY OUTPUT |  |  |  |  |  |
| Velocity Accuracy ${ }^{4}$ |  |  |  |  |  |
| 10-bit |  |  | $\pm 2$ | LSB | Zero acceleration |
| 12-bit |  |  | $\pm 2$ | LSB | Zero acceleration |
| 14-bit |  |  | $\pm 4$ | LSB | Zero acceleration |
| 16-bit |  |  | $\pm 16$ | LSB | Zero acceleration |
| Resolution ${ }^{5}$ |  | 9, 11, 13, 15 |  | Bits |  |
| DYNAMNIC PERFORMANCE |  |  |  |  |  |
| Bandwidth |  |  |  |  |  |
| 10-bit | 2000 |  | 6600 | Hz |  |
|  | 2900 |  | 5400 | Hz | CLKIN $=$ 8.192 MHz |
| 12-bit | 900 |  | 2800 | Hz |  |
|  | 1200 |  | 2200 | Hz | CLKIN $=8.192 \mathrm{MHz}$ |
| 14-bit | 400 |  | 1500 | Hz |  |
|  | 600 |  | 1200 | Hz | CLKIN $=8.192 \mathrm{MHz}$ |
| 16-bit | 100 |  | 350 | Hz |  |
|  | 125 |  | 275 | Hz | CLKIN $=8.192 \mathrm{MHz}$ |
|  |  |  |  |  |  |  |
| 10-bit |  |  | 3125 | rps | $\text { CLKIN }=10.24 \mathrm{MHz}$ |
|  |  |  | 2500 |  | CLKIN $=8.192 \mathrm{MHz}$ |
| 12-bit |  |  | 1250 | rps | CLKIN $=10.24 \mathrm{MHz}$ |
|  |  |  | 1000 |  | CLKIN $=8.192 \mathrm{MHz}$ |
| 14-bit |  |  | 625 | rps | CLKIN $=10.24 \mathrm{MHz}$ |
|  |  |  | 500 |  | CLKIN $=8.192 \mathrm{MHz}$ |
| 16-bit |  |  | 156.25 | rps | $\begin{aligned} & \text { CLKIN }=10.24 \mathrm{MHz} \\ & \text { CLKIN }=8.192 \mathrm{MHz} \end{aligned}$ |
|  |  |  |  |  |  | 125 |
| Acceleration Error |  |  |  |  |  |
| 10-bit |  | 30 |  | arc min | At $50,000 \mathrm{rps},{ }^{2} \mathrm{CLKIN}=8.192 \mathrm{MHz}$ |
| 12-bit |  | 30 |  | arc min | At 10,000 rps, ${ }^{2}$ CLKIN $=8.192 \mathrm{MHz}$ |
| 14-bit |  | 30 |  | arc min | At $2500 \mathrm{rps},{ }^{2} \mathrm{CLKIN}=8.192 \mathrm{MHz}$ |
| 16-bit |  | 30 |  | arc min | At $125 \mathrm{rps},{ }^{2} \mathrm{CLKIN}=8.192 \mathrm{MHz}$ |

## AD2S1210-EP

\begin{tabular}{|c|c|c|c|c|c|}
\hline Parameter \& Min \& Tур \& Max \& Unit \& Conditions/Comments \\
\hline \begin{tabular}{l}
Settling Time \(10^{\circ}\) Step Input 10-bit \\
12-bit \\
14-bit \\
16-bit \\
Settling Time \(179^{\circ}\) Step Input \\
10-bit \\
12-bit \\
14-bit \\
16-bit
\end{tabular} \& \& \[
\begin{aligned}
\& 0.6 \\
\& 2.2 \\
\& 6.5 \\
\& 27.5 \\
\& \\
\& 1.5 \\
\& 4.75 \\
\& 10.5 \\
\& 45
\end{aligned}
\] \& \[
\begin{aligned}
\& 0.9 \\
\& 3.3 \\
\& 9.8 \\
\& 48 \\
\& \\
\& 2.4 \\
\& 6.1 \\
\& 15.2 \\
\& 68
\end{aligned}
\] \& \begin{tabular}{l}
ms \\
ms \\
ms \\
ms \\
ms \\
ms \\
ms \\
ms
\end{tabular} \& \begin{tabular}{l}
To settle to within \(\pm 2\) LSB, CLKIN \(=8.192 \mathrm{MHz}\) \\
To settle to within \(\pm 2\) LSB, CLKIN \(=8.192 \mathrm{MHz}\) \\
To settle to within \(\pm 2\) LSB, CLKIN \(=8.192 \mathrm{MHz}\) \\
To settle to within \(\pm 2\) LSB, CLKIN \(=8.192 \mathrm{MHz}\) \\
To settle to within \(\pm 2\) LSB, CLKIN \(=8.192 \mathrm{MHz}\) \\
To settle to within \(\pm 2\) LSB, CLKIN \(=8.192 \mathrm{MHz}\) \\
To settle to within \(\pm 2\) LSB, CLKIN \(=8.192 \mathrm{MHz}\) \\
To settle to within \(\pm 2\) LSB, CLKIN \(=8.192 \mathrm{MHz}\)
\end{tabular} \\
\hline \begin{tabular}{l}
EXC, \(\overline{\text { EXC OUTPUTS }}\) \\
Voltage \\
Center Voltage \\
Frequency \\
EXC/EXC DC Mismatch \\
EXC/ \(\overline{E X C}\) AC Mismatch THD
\end{tabular} \& \[
\begin{aligned}
\& 3.2 \\
\& 2.40 \\
\& 2
\end{aligned}
\] \& 3.6
\[
2.47
\]
\[
-58
\] \& \begin{tabular}{l}
4.0 \\
2.53 \\
20 \\
30 \\
132
\end{tabular} \& \begin{tabular}{l}
V p-p \\
V \\
kHz \\
mV \\
mV \\
dB
\end{tabular} \& \begin{tabular}{l}
Load \(\pm 100 \mu \mathrm{~A}\), typical differential output \((\mathrm{EXC}\) to \(\overline{\mathrm{EXC}})=7.2 \mathrm{~V}\) p-p \\
First five harmonics
\end{tabular} \\
\hline \begin{tabular}{l}
VOLTAGE REFERENCE REFOUT \\
Drift PSRR
\end{tabular} \& 2.40 \& \[
\begin{aligned}
\& 2.47 \\
\& 100 \\
\& -60
\end{aligned}
\] \& 2.53 \& \[
\begin{aligned}
\& \mathrm{V} \\
\& \mathrm{ppm} /{ }^{\circ} \mathrm{C} \\
\& \mathrm{~dB}
\end{aligned}
\] \& \(\pm \mathrm{l}_{\text {OUT }}=100 \mu \mathrm{~A}\) \\
\hline \begin{tabular}{l}
CLKIN, XTALOUT \({ }^{6}\) \\
\(V_{\text {IL }}\) Voltage Input Low \\
\(\mathrm{V}_{\mathrm{IH}}\) Voltage Input High
\end{tabular} \& 2.0 \& \& 0.8 \& \[
\begin{aligned}
\& \mathrm{V} \\
\& \mathrm{~V}
\end{aligned}
\] \& \\
\hline ```
LOGIC INPUTS
VILL Voltage Input Low
V IH Voltage Input High
I|L
Pull-Up)
I|L
IHH
``` \& \begin{tabular}{l}
2.0 \\
1.7
\[
-10
\]
\end{tabular} \& \& \[
\begin{aligned}
\& 0.8 \\
\& 0.7 \\
\& 10 \\
\& 80
\end{aligned}
\] \& \begin{tabular}{l}
V \\
V \\
V \\
V \\
\(\mu \mathrm{A}\) \\
\(\mu \mathrm{A}\) \\
\(\mu \mathrm{A}\)
\end{tabular} \& \begin{tabular}{l}
\[
\begin{aligned}
\& \mathrm{V}_{\text {DRVE }}=2.7 \mathrm{~V} \text { to } 5.25 \mathrm{~V} \\
\& \mathrm{~V}_{\text {DRIVE }}=2.3 \mathrm{~V} \text { to } 2.7 \mathrm{~V} \\
\& \mathrm{~V}_{\text {DRIVE }}=2.7 \mathrm{~V} \text { to } 5.25 \mathrm{~V} \\
\& \mathrm{~V}_{\text {DRIVE }}=2.3 \mathrm{~V} \text { to } 2.7 \mathrm{~V}
\end{aligned}
\] \\
RESO, RES1, \(\overline{\mathrm{RD}}, \overline{\mathrm{WR}} / \overline{\mathrm{FSYNC}}, \mathrm{A} 0, \mathrm{~A} 1\), and \(\overline{\mathrm{RESET}}\) pins
\end{tabular} \\
\hline \begin{tabular}{l}
LOGIC OUTPUTS \\
\(\mathrm{V}_{\mathrm{oL}}\) Voltage Output Low \\
\(\mathrm{V}_{\text {OH }}\) Voltage Output High \\
\(\mathrm{I}_{\text {ozH }}\) High Level Three-State Leakage I ozL Low Level Three-State Leakage
\end{tabular} \& \[
\begin{aligned}
\& 2.4 \\
\& 2.0 \\
\& -10
\end{aligned}
\] \& \& 0.4

10 \& | V |
| :--- |
| V |
| V |
| $\mu \mathrm{A}$ |
| $\mu \mathrm{A}$ | \& \[

$$
\begin{aligned}
& \mathrm{V}_{\text {DRIVE }}=2.3 \mathrm{~V} \text { to } 5.25 \mathrm{~V} \\
& \mathrm{~V}_{\text {DRIVE }}=2.7 \mathrm{~V} \text { to } 5.25 \mathrm{~V} \\
& \mathrm{~V}_{\text {DRIVE }}=2.3 \mathrm{~V} \text { to } 2.7 \mathrm{~V}
\end{aligned}
$$
\] <br>

\hline | POWER REQUIREMENTS $\mathrm{AV}_{\mathrm{DD}}$ $\mathrm{DV}_{\mathrm{DD}}$ |
| :--- |
| $V_{\text {DRIVE }}$ | \& \[

$$
\begin{aligned}
& 4.75 \\
& 4.75 \\
& 2.3 \\
& \hline
\end{aligned}
$$

\] \& \& \[

$$
\begin{aligned}
& 5.25 \\
& 5.25 \\
& 5.25
\end{aligned}
$$

\] \& \[

$$
\begin{aligned}
& \mathrm{V} \\
& \mathrm{~V} \\
& \mathrm{~V}
\end{aligned}
$$
\] \& <br>

\hline | POWER SUPPLY |
| :--- |
| $I_{\text {AvDD }}$ |
| $I_{\text {DVDD }}$ |
| $I_{\text {OVDD }}$ | \& \& \& \[

$$
\begin{aligned}
& 12 \\
& 35 \\
& 2
\end{aligned}
$$

\] \& | mA |
| :--- |
| mA |
| mA | \& <br>

\hline
\end{tabular}

[^0]
## TIMING SPECIFICATIONS

$A V_{D D}=D V_{D D}=5.0 \mathrm{~V} \pm 5 \%, T_{A}=T_{M I N}$ to $T_{M A X}$, unless otherwise noted. ${ }^{1}$
Table 2.

| Parameter | Description | Limit at $\mathrm{T}_{\text {MIN }}, \mathrm{T}_{\text {MAX }}$ | Unit |
| :---: | :---: | :---: | :---: |
| $\mathrm{f}_{\text {CLKIN }}$ | Frequency of clock input | 6.144 | MHz min |
|  |  | 10.24 | MHz max |
| $\mathrm{t}_{\mathrm{CK}}$ | Clock period ( $\left.\mathrm{t}_{\mathrm{CK}}=1 / \mathrm{f}_{\text {CLKIN }}\right)$ | 98 | $n s$ min |
|  |  | 163 | ns max |
| $\mathrm{t}_{1}$ | A 0 and A 1 setup time before $\overline{\mathrm{RD}} / \overline{\mathrm{CS}}$ low | 2 | $n s$ min |
| $\mathrm{t}_{2}$ | Delay $\overline{\mathrm{CS}}$ falling edge to $\overline{\mathrm{WR}} / \overline{\mathrm{FSYNC}}$ rising edge | 22 | $n \mathrm{nmin}$ |
| $\mathrm{t}_{3}$ | Address/data setup time during a write cycle | 3 | ns min |
| $\mathrm{t}_{4}$ | Address/data hold time during a write cycle | 2 | ns min |
| $\mathrm{t}_{5}$ | Delay $\overline{\mathrm{WR}} / \overline{\text { FSYNC }}$ rising edge to $\overline{\mathrm{CS}}$ rising edge | 2 | $n \mathrm{nsmin}$ |
| $\mathrm{t}_{6}$ | Delay $\overline{\mathrm{CS}}$ rising edge to $\overline{\mathrm{CS}}$ falling edge | 10 | ns min |
| $\mathrm{t}_{7}$ | Delay between writing address and writing data | $2 \times \mathrm{t}_{\mathrm{ck}}+20$ | $n \mathrm{nsmin}$ |
| $\mathrm{t}_{8}$ | A0 and A1 hold time after $\overline{W R} / \overline{F S Y N C}$ rising edge | 2 | $n \mathrm{nsmin}$ |
| $\mathrm{t}_{9}$ | Delay between successive write cycles | $6 \times \mathrm{t}_{\mathrm{ck}}+20$ | $n \mathrm{nsmin}$ |
| $\mathrm{t}_{10}$ | Delay between rising edge of $\overline{\mathrm{WR}} / \overline{\mathrm{FSYNC}}$ and falling edge of $\overline{\mathrm{RD}}$ | 2 | $n s$ min |
| $t_{11}$ | Delay $\overline{\mathrm{CS}}$ falling edge to $\overline{\mathrm{RD}}$ falling edge | 2 | $n \mathrm{n}$ min |
| $\mathrm{t}_{12}$ | Enable delay $\overline{\mathrm{RD}}$ low to data valid in configuration mode |  |  |
|  | $\mathrm{V}_{\text {DRIVE }}=4.5 \mathrm{~V}$ to 5.25 V | 37 | ns min |
|  | $\mathrm{V}_{\text {DRIVE }}=2.7 \mathrm{~V}$ to 3.6 V | 25 | ns min |
|  | $\mathrm{V}_{\text {DRIVE }}=2.3 \mathrm{~V}$ to 2.7 V | 30 | ns min |
| $\mathrm{t}_{13}$ | $\overline{\mathrm{RD}}$ rising edge to $\overline{\mathrm{CS}}$ rising edge | 2 | $n \mathrm{nsmin}$ |
| $\mathrm{t}_{14 \mathrm{~A}}$ | Disable delay $\overline{\mathrm{RD}}$ high to data high-Z | 16 | $n \mathrm{nmin}$ |
| $\mathrm{t}_{14 \mathrm{~B}}$ | Disable delay $\overline{C S}$ high to data high-Z | 16 | ns min |
| $\mathrm{t}_{15}$ | Delay between rising edge of $\overline{\mathrm{RD}}$ and falling edge of $\overline{\mathrm{WR}} / \overline{\mathrm{FSYNC}}$ | 2 | $n \mathrm{nsmin}$ |
| $\mathrm{t}_{16}$ | $\overline{\text { SAMPLE }}$ pulse width | $2 \times \mathrm{t}_{\mathrm{CK}}+20$ | ns min |
| $\mathrm{t}_{17}$ | Delay from $\overline{\text { SAMPLE }}$ before $\overline{\mathrm{RD}} / \overline{\mathrm{CS}}$ low | $6 \times \mathrm{t}_{\mathrm{CK}}+20$ | $n \mathrm{nmin}$ |
| $\mathrm{t}_{18}$ | Hold time $\overline{\mathrm{RD}}$ before $\overline{\mathrm{RD}}$ low | 2 | $n \mathrm{nmin}$ |
| $\mathrm{t}_{19}$ | Enable delay $\overline{\mathrm{RD}} / \overline{\mathrm{CS}}$ low to data valid |  |  |
|  | $\mathrm{V}_{\text {DRIVE }}=4.5 \mathrm{~V}$ to 5.25 V | 17 | $n \mathrm{nmin}$ |
|  | $\mathrm{V}_{\text {DRIVE }}=2.7 \mathrm{~V}$ to 3.6 V | 21 | ns min |
|  | $\mathrm{V}_{\text {DRIVE }}=2.3 \mathrm{~V}$ to 2.7 V | 33 | $n \mathrm{nmin}$ |
| $\mathrm{t}_{20}$ | $\overline{\mathrm{RD}}$ pulse width | 6 | $n \mathrm{nmin}$ |
| $\mathrm{t}_{21}$ | A 0 and A 1 set time to data valid when $\overline{\mathrm{RD}} / \overline{\mathrm{CS}}$ low |  |  |
|  | $\mathrm{V}_{\text {DRIVE }}=4.5 \mathrm{~V}$ to 5.25 V | 36 | $n s$ min |
|  | $\mathrm{V}_{\text {DRIVE }}=2.7 \mathrm{~V}$ to 3.6 V | 37 | $n s$ min |
|  | $\mathrm{V}_{\text {DRIVE }}=2.3 \mathrm{~V}$ to 2.7 V | 29 | ns min |
| $\mathrm{t}_{22}$ | Delay $\overline{W R} / \overline{\text { FSYNC }}$ falling edge to SCLK rising edge | 3 | $n \mathrm{nmin}$ |
| $\mathrm{t}_{23}$ | Delay $\overline{\mathrm{WR}} / \overline{\text { FSYNC }}$ falling edge to SDO release from high-Z |  |  |
|  | $\mathrm{V}_{\text {DRIVE }}=4.5 \mathrm{~V}$ to 5.25 V | 16 | $n s$ min |
|  | $\mathrm{V}_{\text {DRIVE }}=2.7 \mathrm{~V}$ to 3.6 V | 26 | ns min |
|  | $\mathrm{V}_{\text {DRIVE }}=2.3 \mathrm{~V}$ to 2.7 V | 29 | ns min |
| $\mathrm{t}_{24}$ | Delay SCLK rising edge to DBx valid |  |  |
|  | $\mathrm{V}_{\text {DRIVE }}=4.5 \mathrm{~V}$ to 5.25 V | 24 | $n \mathrm{nmin}$ |
|  | $\mathrm{V}_{\text {DRIVE }}=2.7 \mathrm{~V}$ to 3.6 V | 18 | ns min |
|  | $\mathrm{V}_{\text {DRIVE }}=2.3 \mathrm{~V}$ to 2.7 V | 32 | ns min |
| $\mathrm{t}_{25}$ | SCLK high time | $0.4 \times \mathrm{t}_{\text {scLk }}$ | ns min |
| $\mathrm{t}_{26}$ | SCLK low time | $0.4 \times \mathrm{t}_{\text {scLk }}$ | $n \mathrm{nmin}$ |
| $\mathrm{t}_{27}$ | SDI setup time prior to SCLK falling edge | 3 | $n \mathrm{~ns}$ min |
| $\mathrm{t}_{28}$ | SDI hold time after SCLK falling edge | 2 | $n \mathrm{nmin}$ |

## AD2S1210-EP

| Parameter | Description | Limit at $\mathrm{T}_{\text {MIN }}, \mathrm{T}_{\text {MAX }}$ | Unit |
| :---: | :---: | :---: | :---: |
| $\mathrm{t}_{29}$ | Delay $\overline{\mathrm{WR}} / \overline{\text { FSYNC rising edge to SDO high-Z }}$ | 15 | ns min |
| $\mathrm{t}_{30}$ | Delay from $\overline{\text { SAMPLE }}$ before $\overline{W R} / \overline{\text { FSYNC }}$ falling edge | $6 \times \mathrm{t}_{\mathrm{ck}}+20 \mathrm{~ns}$ | ns min |
| $\mathrm{t}_{31}$ | Delay $\overline{\mathrm{CS}}$ falling edge to $\overline{\mathrm{WR}} / \overline{\mathrm{FSYNC}}$ falling edge in normal mode | 2 | ns min |
| $\mathrm{t}_{32}$ | A 0 and A 1 setup time before $\overline{\mathrm{WR}} / \overline{\mathrm{FSYNC}}$ falling edge | 2 | $n \mathrm{nmin}$ |
| $\mathrm{t}_{33}$ | A0 and A1 hold time after $\overline{W R} / \overline{\text { FSYNC falling edge }{ }^{2}}$ |  |  |
|  | In normal mode, A0 $=0, A 1=0 / 1$ | $24 \times \mathrm{t}_{\mathrm{CK}}+5 \mathrm{~ns}$ | $n s$ min |
|  | In configuration mode, $\mathrm{A} 0=1, \mathrm{~A} 1=1$ | $8 \times \mathrm{t}_{\mathrm{CK}}+5 \mathrm{~ns}$ | $n \mathrm{~ns}$ min |
| $\mathrm{t}_{34}$ | Delay $\overline{\mathrm{WR}} / \overline{\mathrm{FSYNC}}$ rising edge to $\overline{\mathrm{WR}} / \overline{\mathrm{FSYNC}}$ falling edge | 10 | $n \mathrm{~ns}$ min |
| $\mathrm{f}_{\text {sclk }}$ | Frequency of SCLK input |  |  |
|  | $\mathrm{V}_{\text {DRIVE }}=4.5 \mathrm{~V}$ to 5.25 V | 20 | MHz |
|  | $\mathrm{V}_{\text {DRIVE }}=2.7 \mathrm{~V}$ to 3.6 V | 25 | MHz |
|  | $\mathrm{V}_{\text {DRIVE }}=2.3 \mathrm{~V}$ to 2.7 V | 15 | MHz |

[^1]
## ABSOLUTE MAXIMUM RATINGS

Table 3.

| Parameter | Rating |
| :---: | :---: |
| $\mathrm{AV}_{\mathrm{DD}}$ to AGND, DGND | -0.3 V to +7.0 V |
| DV ${ }_{\text {DD }}$ to AGND, DGND | -0.3 V to +7.0 V |
| $\mathrm{V}_{\text {DRIVE }}$ to AGND, DGND | -0.3 V to $\mathrm{AV}_{\mathrm{DD}}$ |
| $A V_{D D}$ to $\mathrm{DV}_{\text {DD }}$ | -0.3 V to +0.3 V |
| AGND to DGND | -0.3 V to +0.3 V |
| Analog Input Voltage to AGND | -0.3 V to $\mathrm{AV}_{\mathrm{DD}}+0.3 \mathrm{~V}$ |
| Digital Input Voltage to DGND | -0.3 V to $\mathrm{V}_{\text {DRIVE }}+0.3 \mathrm{~V}$ |
| Digital Output Voltage to DGND | -0.3 V to $\mathrm{V}_{\text {DRIVE }}+0.3 \mathrm{~V}$ |
| Analog Output Voltage Swing | -0.3 V to AV $\mathrm{DD}+0.3 \mathrm{~V}$ |
| Input Current to Any Pin Except Supplies ${ }^{1}$ | $\pm 10 \mathrm{~mA}$ |
| Operating Temperature Range (Ambient) |  |
| EP Grade | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| $\theta_{\mathrm{JA}}$ Thermal Impedance ${ }^{2}$ | $54^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\theta_{\text {jc }}$ Thermal Impedance ${ }^{2}$ | $15^{\circ} \mathrm{C} / \mathrm{W}$ |
| RoHS-Compliant Temperature, Soldering Reflow | $260(-5 /+0)^{\circ} \mathrm{C}$ |
| ESD | 2 kV HBM |

[^2]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

## AD2S1210-EP

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



Figure 2. Pin Configuration
Table 4. Pin Function Descriptions

| $\begin{aligned} & \text { Pin } \\ & \text { No. } \end{aligned}$ | Mnemonic | Description |
| :---: | :---: | :---: |
| 1 | RES1 | Resolution Select 1. Logic input. RES1 in conjunction with RES0 allows the resolution of the AD2S1210-EP to be programmed. |
| 2 | $\overline{C S}$ | Chip Select. Active low logic input. The device is enabled when $\overline{\mathrm{CS}}$ is held low. |
| 3 | $\overline{\mathrm{RD}}$ | Edge-Triggered Logic Input. When the $\overline{S O E}$ pin is high, this pin acts as a frame synchronization signal and output enable for the parallel data outputs, DB15 to DB0. The output buffer is enabled when $\overline{\mathrm{CS}}$ and $\overline{\mathrm{RD}}$ are held low. When the $\overline{\mathrm{SOE}}$ pin is low, the $\overline{\mathrm{RD}}$ pin should be held high. |
| 4 | $\overline{\text { WR } / \overline{\text { FSYNC }}}$ | Edge-Triggered Logic Input. When the $\overline{S O E}$ pin is high, this pin acts as a frame synchronization signal and input enable for the parallel data inputs, DB7 to DB0. The input buffer is enabled when $\overline{\mathrm{CS}}$ and $\overline{\mathrm{WR}} / \overline{\mathrm{FSYNC}}$ are held low. When the $\overline{\text { SOE }}$ pin is low, the $\overline{W R} / \overline{F S Y N C}$ pin acts as a frame synchronization signal and enable for the serial data bus. |
| 5,19 | DGND | Digital Ground. These pins are ground reference points for digital circuitry on the AD2S1210-EP. Refer all digital input signals to this DGND voltage. Both of these pins can be connected to the AGND plane of a system. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. |
| 6 | DV DD | Digital Supply Voltage, 4.75 V to 5.25 V . This is the supply voltage for all digital circuitry on the AD2S1210-EP. The AV ${ }_{D D}$ and $\mathrm{DV}_{\mathrm{DD}}$ voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. |
| 7 | CLKIN | Clock Input. A crystal or oscillator can be used at the CLKIN and XTALOUT pins to supply the required clock frequency of the AD2S1210-EP. Alternatively, a single-ended clock can be applied to the CLKIN pin. The input frequency of the AD2S1210-EP is specified from 6.144 MHz to 10.24 MHz . |
| 8 | XTALOUT | Crystal Output. When using a crystal or oscillator to supply the clock frequency to the AD2S1210-EP, apply the crystal across the CLKIN and XTALOUT pins. When using a single-ended clock source, the XTALOUT pin should be considered a no connect pin. |
| 9 | $\overline{\text { SOE }}$ | Serial Output Enable. Logic input. This pin enables either the parallel or serial interface. The serial interface is selected by holding the $\overline{\text { SOE }}$ pin low, and the parallel interface is selected by holding the $\overline{\text { SOE }}$ pin high. |
| 10 | $\overline{\text { SAMPLE }}$ | Sample Result. Logic input. Data is transferred from the position and velocity integrators to the position and velocity registers after a high-to-low transition on the SAMPLE signal. The fault register is also updated after a high-to-low transition on the SAMPLE signal. |
| 11 | DB15/SDO | Data Bit 15/Serial Data Output Bus. When the $\overline{\text { SOE }}$ pin is high, this pin acts as DB15, a three-state data output pin controlled by $\overline{\mathrm{CS}}$ and $\overline{\mathrm{RD}}$. When the $\overline{\mathrm{SOE}}$ pin is low, this pin acts as SDO, the serial data output bus controlled by $\overline{\mathrm{CS}}$ and $\overline{\mathrm{WR}} / \overline{\mathrm{FSYNC}}$. The bits are clocked out on the rising edge of SCLK. |
| 12 | DB14/SDI | Data Bit 14/Serial Data Input Bus. When the $\overline{S O E}$ pin is high, this pin acts as DB14, a three-state data output pin controlled by $\overline{\mathrm{CS}}$ and $\overline{\mathrm{RD}}$. When the $\overline{\text { SOE }}$ pin is low, this pin acts as SDI, the serial data input bus controlled by $\overline{\mathrm{CS}}$ and $\overline{\mathrm{WR}} / \overline{\mathrm{FSYNC}}$. The bits are clocked in on the falling edge of SCLK. |


| $\begin{aligned} & \hline \text { Pin } \\ & \text { No } \end{aligned}$ | Mnemonic | Description |
| :---: | :---: | :---: |
| 13 | DB13/SCLK | Data Bit 13/Serial Clock. In parallel mode, this pin acts as DB13, a three-state data output pin controlled by $\overline{\mathrm{CS}}$ and $\overline{\mathrm{RD}}$. In serial mode, this pin acts as the serial clock input. |
| $\begin{aligned} & 14 \text { to } \\ & 17 \end{aligned}$ | $\begin{aligned} & \text { DB12 to } \\ & \text { DB9 } \end{aligned}$ | Data Bit 12 to Data Bit 9. Three-state data output pins controlled by $\overline{\mathrm{CS}}$ and $\overline{\mathrm{RD}}$. |
| 18 | $\mathrm{V}_{\text {DRIVE }}$ | Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface operates. Decouple this pin to DGND. The voltage range on this pin is 2.3 V to 5.25 V and may be different from the voltage range at $A V_{D D}$ and $D V_{D D}$ but should never exceed either by more than 0.3 V . |
| 20 | DB8 | Data Bit 8. Three-state data output pin controlled by $\overline{\mathrm{CS}}$ and $\overline{\mathrm{RD}}$. |
| $\begin{aligned} & 21 \text { to } \\ & 28 \end{aligned}$ | DB7 to DB0 | Data Bit 7 to Data Bit 0. Three-state data input/output pins controlled by $\overline{\mathrm{CS}}, \overline{\mathrm{RD}}$, and $\overline{\mathrm{WR}} / \overline{\mathrm{FSYNC}}$. |
| 29 | A | Incremental Encoder Emulation Output A. Logic output. This output is free running and is valid if the resolver format input signals applied to the converter are valid. |
| 30 | B | Incremental Encoder Emulation Output B. Logic output. This output is free running and is valid if the resolver format input signals applied to the converter are valid. |
| 31 | NM | North Marker Incremental Encoder Emulation Output. Logic output. This output is free running and is valid if the resolver format input signals applied to the converter are valid. |
| 32 | DIR | Direction. Logic output. This output is used in conjunction with the incremental encoder emulation outputs. The DIR output indicates the direction of the input rotation and is high for increasing angular rotation. |
| 33 | $\overline{\text { RESET }}$ | Reset. Logic input. The AD2S1210-EP requires an external reset signal to hold the $\overline{\operatorname{RESET}}$ input low until $\mathrm{V}_{\mathrm{DD}}$ is within the specified operating range of 4.75 V to 5.25 V . |
| 34 | LOT | Loss of Tracking. Logic output. Loss of tracking (LOT) is indicated by a logic low on the LOT pin and is not latched. |
| 35 | DOS | Degradation of Signal. Logic output. Degradation of signal (DOS) is detected when either resolver input (sine or cosine) exceeds the specified DOS sine/cosine threshold or when an amplitude mismatch occurs between the sine and cosine input voltages. DOS is indicated by a logic low on the DOS pin. |
| 36 | A1 | Mode Select 1. Logic input. A1 in conjunction with A0 allows the mode of the AD2S1210-EP to be selected. |
| 37 | A0 | Mode Select 0. Logic input. A0 in conjunction with A1 allows the mode of the AD2S1210-EP to be selected. |
| 38 | EXC | Excitation Frequency. Analog output. An on-board oscillator provides the sinusoidal excitation signal (EXC) and its complement signal ( $\overline{\mathrm{EXC}})$ to the resolver. The frequency of this reference signal is programmable via the excitation frequency register. |
| 39 | $\overline{\text { EXC }}$ | Excitation Frequency Complement. Analog output. An on-board oscillator provides the sinusoidal excitation signal (EXC) and its complement signal ( $\overline{\mathrm{EXC}}$ ) to the resolver. The frequency of this reference signal is programmable via the excitation frequency register. |
| 40 | AGND | Analog Ground. This pin is the ground reference points for analog circuitry on the AD2S1210-EP. Refer all analog input signals and any external reference signal to this AGND voltage. Connect the AGND pin to the AGND plane of a system. The AGND and DGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. |
| 41 | SIN | Positive Analog Input of Differential SIN/SINLO Pair. The input range is 2.3 V p-p to 4.0 V p-p. |
| 42 | SINLO | Negative Analog Input of Differential SIN/SINLO Pair. The input range is 2.3 V p-p to 4.0 V p-p. |
| 43 | $\mathrm{AV}_{\mathrm{DD}}$ | Analog Supply Voltage, 4.75 V to 5.25 V . This pin is the supply voltage for all analog circuitry on the AD2S1210-EP. The $A V_{D D}$ and $D V_{D D}$ voltages ideally should be at the same potential and must not be more than 0.3 V apart, even on a transient basis. |
| 44 | COSLO | Negative Analog Input of Differential COS/COSLO Pair. The input range is $2.3 \mathrm{Vp-p} \mathrm{to} 4.0 \mathrm{~V}$ p-p. |
| 45 | cos | Positive Analog Input of Differential COS/COSLO Pair. The input range is $2.3 \mathrm{Vp-p} \mathrm{to} 4.0 \mathrm{Vp-p}$. |
| 46 | REFBYP | Reference Bypass. Connect reference decoupling capacitors at this pin. Typical recommended values are $10 \mu \mathrm{~F}$ and $0.01 \mu \mathrm{~F}$. |
| 47 | REFOUT | Voltage Reference Output. |
| 48 | RESO | Resolution Select 0 . Logic input. RES0 in conjunction with RES1 allows the resolution of the AD2S1210-EP to be programmed. |

## AD2S1210-EP

## TYPICAL PERFORMANCE CHARACTERISTICS

$\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{AV}_{\mathrm{DD}}=\mathrm{DV}_{\mathrm{DD}}=\mathrm{V}_{\mathrm{DRIVE}}=5 \mathrm{~V}, \mathrm{SIN} / \mathrm{SINLO}=3.15 \mathrm{~V}$ p-p, COS/COSLO $=3.15 \mathrm{~V}$ p-p, CLKIN $=8.192 \mathrm{MHz}$, unless otherwise noted.


Figure 3. Typical 16-Bit Angular Accuracy Histogram Of Codes, 10,000 Samples


Figure 4. Typical 14-Bit Angular Accuracy Histogram of Codes, 10,000 Samples, Hysteresis Disabled


Figure 5. Typical 14-Bit Angular Accuracy Histogram of Codes, 10,000 Samples, Hysteresis Enabled


Figure 6. Typical 12-Bit Angular Accuracy Histogram of Codes, 10,000 Samples, Hysteresis Disabled


Figure 7. Typical 12-Bit Angular Accuracy Histogram of Codes, 10,000 Samples, Hysteresis Enabled


Figure 8. Typical 10-Bit Angular Accuracy Histogram of Codes, 10,000 Samples, Hysteresis Disabled


Figure 9. Typical 10-Bit Angular Accuracy Histogram of Codes, 10,000 Samples, Hysteresis Enabled


Figure 10. Typical 16-Bit $10^{\circ}$ Step Response


Figure 11. Typical 14-Bit $10^{\circ}$ Step Response


Figure 12. Typical 12-Bit $10^{\circ}$ Step Response


Figure 13. Typical 10-Bit $10^{\circ}$ Step Response


Figure 14. Typical 16-Bit $179^{\circ}$ Step Response

## AD2S1210-EP



Figure 15. Typical 14-Bit $179^{\circ}$ Step Response


Figure 16. Typical 12-Bit $179^{\circ}$ Step Response


Figure 17. Typical 10-Bit $179^{\circ}$ Step Response


Figure 18. Typical System Magnitude Response


Figure 19. Typical System Phase Response


Figure 20. Typical 16-Bit Tracking Error vs. Acceleration


Figure 21. Typical 14-Bit Tracking Error vs. Acceleration


Figure 22. Typical 12-Bit Tracking Error vs. Acceleration


Figure 23. Typical 10-Bit Tracking Error vs. Acceleration

## AD2S1210-EP

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BBC

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Figure 24. 48-Lead Low Profile Quad Flat Package [LQFP] (ST-48)
Dimensions shown in millimeters

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
| :--- | :--- | :--- | :--- |
| AD2S1210SST-EP-RL7 | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | 48 -Lead LQFP | ST-48 |

NOTES

## AD2S1210-EP

## NOTES


[^0]:    ${ }^{1}$ Temperature range is as follows: $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$.
    ${ }^{2}$ The voltages SIN, SINLO, COS, and COSLO, relative to AGND, must always be between 0.15 V and $A V_{D D}-0.2 \mathrm{~V}$.
    ${ }^{3}$ All specifications within the angular accuracy parameter are tested at constant velocity, that is, zero acceleration.
    ${ }^{4}$ The velocity accuracy specification includes velocity offset and dynamic ripple.
    ${ }^{5}$ For example, when RESO $=0$ and RES1 $=1$, the position output has a resolution of 12 bits. The velocity output has a resolution of 11 bits with the MSB indicating the direction of rotation. In this example, with a CLKIN frequency of 8.192 MHz , the velocity LSB is 0.488 rps , that is, $1000 \mathrm{rps} /\left(2^{11}\right)$.
    ${ }^{6}$ The clock frequency of the AD2S1210-EP can be supplied with a crystal, an oscillator, or directly from a DSP/microprocessor digital output. When using a single-ended clock signal directly from the DSP/microprocessor, the XTALOUT pin should remain open circuit and the logic levels outlined under the logic inputs parameter in Table 1 apply.

[^1]:    ${ }^{1}$ Temperature range is as follows: $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$.
    ${ }^{2}$ A0 and A1 should remain constant for the duration of the serial readback. This may require 24 clock periods to read back the 8 -bit fault information in addition to the 16 bits of position/velocity data. If the fault information is not required, $A 0 / \mathrm{A} 1$ may be released after 16 clock cycles.

[^2]:    ${ }^{1}$ Transient currents of up to 100 mA do not cause latch-up.
    ${ }^{2}$ JEDEC 2S2P standard board.

