FEATURES<br>Monolithic 10-Bit/ 60 MSPS Converter TTL Outputs

Bipolar ( $\pm 1.75$ V) Analog Input
56 dB SNR @ 2.3 MHz Input
Low (45 pF) Input Capacitance
MIL-STD-883 Compliant Versions Available
APPLICATIONS
Digital Oscilloscopes
Medical Imaging
Professional Video
Radar Warning/ Guidance Systems
Infrared Systems

## GENERAL DESCRIPTION

The AD 9020 A/D converter is a 10-bit monolithic converter capable of word rates of 60 M SPS and above. Innovative architecture using 512 input comparators instead of the traditional 1024 required by other flash converters reduces input capacitance and improves linearity.

Encode and outputs are T T L-compatible, making the AD 9020 an ideal candidate for use in low power systems. An overflow bit is provided to indicate analog input signals greater than $+\mathrm{V}_{\text {SEnSE }}$.
V oltage sense lines are provided to insure accurate driving of the $\pm \mathrm{V}_{\text {REF }}$ Voltages applied to the units. Quarter-point taps on the resistor ladder help optimize the integral linearity of the unit.
Either 68-pin ceramic leaded (gull wing) packages or ceramic LCC s are available and are specifically designed for low thermal impedances. T wo performance grades for temperatures of both $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ and $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ ranges are offered to allow the user to select the linearity best suited for each application. Dynamic performance is fully characterized and production tested at $+25^{\circ} \mathrm{C}$. M IL-ST D-883 units are available.
The AD 9020 A/D Converter is available in versions compliant with M IL-STD-883. Refer to the Analog D evices M ilitary Products D atabook or current AD 9020/883B data sheet for detailed specifications.

REV. A

[^0]FUNCTIONAL BLOCK DIAGRAM


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## AD9020- SPECIFICATIONS

| ABSOLUTE MAXIMUM RATINGS ${ }^{\mathbf{1}}$ |  | 3/4 Ref, $1 / 2_{\text {ReF }}, 1 / 4_{\text {ReF }}$ Current | $\pm 10 \mathrm{~mA}$ |
| :---: | :---: | :---: | :---: |
| $+\mathrm{V}_{\text {S }}$ | +6 V | Digital Output Current | 20 mA |
| - $\mathrm{V}_{\text {S }}$ | .-6 V | Operating T emperature |  |
| ANALOG IN | -2 V to +2 V | AD 9020JE/K E/JZ/K Z | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |
| $+\mathrm{V}_{\text {REF }},-\mathrm{V}_{\text {REF }}, 3 / 4_{\text {REF }}, 1 / 2_{\text {REF }}, 1 / 4_{\text {REF }}$ | -2V to +2 V | Storage T emperature | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| + $\mathrm{V}_{\text {REF }}$ to $-\mathrm{V}_{\text {REF }}$ | . . . 4.0 V | M aximum Junction T emperature ${ }^{2}$ | $+175^{\circ} \mathrm{C}$ |
| DIGITAL INPUTS | -0.5 V to +V V | L ead Soldering Temp (10 sec) | $+300^{\circ} \mathrm{C}$ |

## ELECTRICAL CHARACTERIST|CS $\left( \pm V_{S}= \pm 5 \mathrm{~V}_{;} \pm \mathrm{V}_{\text {SENSE }}= \pm 1.75 \mathrm{~V}\right.$; ENCODE $=40 \mathrm{MSPS}$ unless otherwise noted $)$

| Parameter (Conditions) | Temp | Test Level | AD9020jE/JZ |  |  | AD9020KE/KZ |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max | Min | Typ | Max |  |
| RESOLUTION |  |  | 10 |  |  | 10 |  |  | Bits |
| DC ACCURACY ${ }^{3}$ <br> Differential $N$ onlinearity <br> Integral N onlinearity <br> No M issing Codes | $\begin{aligned} & +25^{\circ} \mathrm{C} \\ & \text { Full } \\ & +25^{\circ} \mathrm{C} \\ & \text { Full } \\ & \text { Full } \end{aligned}$ | $\begin{aligned} & \mathrm{I} \\ & \mathrm{VI} \\ & \mathrm{I} \\ & \mathrm{VI} \\ & \mathrm{VI} \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 1.25 \end{aligned}$ | $\begin{aligned} & 1.25 \\ & 1.5 \\ & 2.0 \\ & 2.5 \end{aligned}$ |  | $\begin{aligned} & 0.75 \\ & 1.0 \\ & \text { Guara } \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 1.25 \\ & 1.5 \\ & 2.0 \\ & \text { eed } \end{aligned}$ | $\begin{aligned} & \text { LSB } \\ & \text { LSB } \\ & \text { LSB } \\ & \text { LSB } \end{aligned}$ |
| ANALOG INPUT Input Bias Current ${ }^{4}$ <br> Input Resistance Input C apacitance ${ }^{4}$ Analog Bandwidth | $\begin{aligned} & +25^{\circ} \mathrm{C} \\ & \text { F ull } \\ & +25^{\circ} \mathrm{C} \\ & +25^{\circ} \mathrm{C} \\ & +25^{\circ} \mathrm{C} \end{aligned}$ | $\begin{aligned} & \mathrm{I} \\ & \mathrm{VI} \\ & \mathrm{I} \\ & \mathrm{~V} \\ & \mathrm{~V} \end{aligned}$ | 2.0 | $\begin{aligned} & 0.4 \\ & 7.0 \\ & 45 \\ & 175 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 2.0 \end{aligned}$ | 2.0 | $\begin{aligned} & 0.4 \\ & 7.0 \\ & 45 \\ & 175 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 2.0 \end{aligned}$ | mA <br> mA <br> k $\Omega$ <br> pF <br> M Hz |
| REFERENCE INPUT <br> Reference L adder Resistance <br> L adder T empco <br> Reference L adder Offset T op of L adder <br> Bottom of Ladder <br> Offset Drift C oefficient | $\begin{aligned} & +25^{\circ} \mathrm{C} \\ & \text { Full } \\ & \text { Full } \\ & +25^{\circ} \mathrm{C} \\ & \text { Full } \\ & +25^{\circ} \mathrm{C} \\ & \text { Full } \\ & \text { Full } \end{aligned}$ | $\begin{aligned} & \mathrm{I} \\ & \mathrm{VI} \\ & \mathrm{~V} \\ & \\ & \mathrm{I} \\ & \mathrm{VI} \\ & \mathrm{I} \\ & \mathrm{VI} \\ & \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 22 \\ & 14 \end{aligned}$ | 37 <br> 0.1 <br> 45 <br> 45 <br> 50 | $\begin{aligned} & 56 \\ & 66 \\ & \\ & 90 \\ & 90 \\ & 90 \\ & 90 \end{aligned}$ | $\begin{aligned} & 22 \\ & 14 \end{aligned}$ | 37 <br> 0.1 <br> 45 <br> 45 <br> 50 | $\begin{aligned} & 56 \\ & 66 \\ & \\ & 90 \\ & 90 \\ & 90 \\ & 90 \end{aligned}$ | $\Omega$ <br> $\Omega$ <br> $\Omega /{ }^{\circ} \mathrm{C}$ <br> mV <br> mV <br> mV <br> mV <br> $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| SWITCHING PERFORMANCE <br> Conversion Rate <br> A perture D elay ( $\mathrm{t}_{\mathrm{A}}$ ) <br> A perture U ncertainty (Jitter) <br> Output Delay $\left(\mathrm{t}_{\mathrm{OD}}\right)^{5}$ <br> Output T ime Skew ${ }^{5}$ | $\begin{aligned} & +25^{\circ} \mathrm{C} \\ & +25^{\circ} \mathrm{C} \\ & +25^{\circ} \mathrm{C} \\ & +25^{\circ} \mathrm{C} \\ & +25^{\circ} \mathrm{C} \end{aligned}$ | $\begin{aligned} & \text { I } \\ & \text { V } \\ & \text { V } \\ & \text { I } \\ & \text { I } \end{aligned}$ | 60 6 | $\begin{aligned} & 1 \\ & 5 \\ & 10 \\ & 3 \end{aligned}$ | $\begin{aligned} & 13 \\ & 5 \end{aligned}$ | 60 6 | $\begin{aligned} & 1 \\ & 5 \\ & 10 \\ & 3 \end{aligned}$ | $\begin{aligned} & 13 \\ & 5 \end{aligned}$ | M SPS <br> ns <br> ps, rms <br> ns <br> ns |
| DYNAMIC PERFORMANCE <br> Transient Response Overvoltage Recovery Time Effective Number of Bits (ENOB) $\mathrm{f}_{\mathrm{IN}}=2.3 \mathrm{M} \mathrm{~Hz}$ $\mathrm{f}_{\mathrm{IN}}=10.3 \mathrm{M} \mathrm{~Hz}$ $\mathrm{f}_{\mathrm{IN}}=15.3 \mathrm{M} \mathrm{~Hz}$ <br> Signal-to-N oise Ratio ${ }^{6}$ $\begin{aligned} & f_{\text {fN }}=2.3 \mathrm{M} \mathrm{~Hz} \\ & f_{\text {fN }}=10.3 \mathrm{M} \mathrm{~Hz} \\ & \mathrm{f}_{\mathrm{IN}}=15.3 \mathrm{M} \mathrm{~Hz} \end{aligned}$ <br> Signal-to-N oise Ratio ${ }^{6}$ (Without H armonics) $\begin{aligned} & f_{f_{I N}}=2.3 \mathrm{M} \mathrm{~Hz} \\ & \mathrm{f}_{\text {IN }}=10.3 \mathrm{M} \mathrm{~Hz} \\ & \mathrm{f}_{\mathrm{IN}}=15.3 \mathrm{M} \mathrm{~Hz} \end{aligned}$ | $\begin{aligned} & +25^{\circ} \mathrm{C} \\ & +25^{\circ} \mathrm{C} \\ & +25^{\circ} \mathrm{C} \\ & +25^{\circ} \mathrm{C} \\ & +25^{\circ} \mathrm{C} \\ & +25^{\circ} \mathrm{C} \\ & +25^{\circ} \mathrm{C} \\ & +25^{\circ} \mathrm{C} \\ & \\ & +25^{\circ} \mathrm{C} \\ & +25^{\circ} \mathrm{C} \\ & +25^{\circ} \mathrm{C} \end{aligned}$ | V <br> V <br> I <br> IV <br> IV <br> I <br> I <br> I <br> I <br> I <br> I | $\begin{aligned} & 8.6 \\ & 8.0 \\ & 7.5 \\ & 54 \\ & 50 \\ & 47 \\ & \\ & \\ & 54 \\ & 51 \\ & 48 \end{aligned}$ | 10 10 <br> 9.0 <br> 8.4 <br> 8.0 <br> 56 <br> 53 <br> 50 <br> 56 <br> 54 <br> 52 |  | $\begin{aligned} & 8.6 \\ & 8.0 \\ & 7.5 \\ & 54 \\ & 50 \\ & 47 \\ & \\ & \\ & 54 \\ & 51 \\ & 48 \\ & \hline \end{aligned}$ | 10 10 <br> 9.0 <br> 8.4 <br> 8.0 <br> 56 <br> 53 <br> 50 <br> 56 <br> 54 <br> 52 |  | ns ns <br> Bits <br> Bits <br> Bits <br> dB <br> dB <br> dB <br> dB <br> dB <br> dB |


| Parameter (Conditions) | Temp | Test Level | AD9020]E/J |  |  | AD9020KE/KZ |  |  | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max | Min | Typ | Max |  |
| DYN AMIC PERFORM ANCE (continued) |  |  |  |  |  |  |  |  |  |
| H armonic Distortion |  |  |  |  |  |  |  |  |  |
| $\mathrm{f}_{\mathrm{IN}}=2.3 \mathrm{M} \mathrm{Hz}$ | $+25^{\circ} \mathrm{C}$ | I | 61 | 67 |  | 61 | 67 |  | dBc |
| $\mathrm{f}_{\mathrm{IN}}=10.3 \mathrm{M} \mathrm{Hz}$ | $+25^{\circ} \mathrm{C}$ | I | 55 | 59 |  | 55 | 59 |  | dBc |
| $\mathrm{f}_{\mathrm{IN}}=15.3 \mathrm{M} \mathrm{Hz}$ | $+25^{\circ} \mathrm{C}$ | I | 49 | 53 |  | 49 | 53 |  | dBC |
| T wo-T one Intermodulation |  |  |  |  |  |  |  |  |  |
| Distortion Rejection ${ }^{7}$ | $+25^{\circ} \mathrm{C}$ | v |  | 70 |  |  | 70 |  | dBc |
| D ifferential Phase | $+25^{\circ} \mathrm{C}$ | V |  | 0.5 |  |  | 0.5 |  | D egree |
| D ifferential G ain | $+25^{\circ} \mathrm{C}$ | V |  | 1 |  |  | 1 |  | \% |
| ENCODEINPUT |  |  |  |  |  |  |  |  |  |
| Logic " ${ }^{\text {" V Voltage }}$ | Full | VI | 2.0 |  |  | 2.0 |  |  | v |
| Logic "0" Voltage | Full | VI |  |  | 0.8 |  |  | 0.8 | V |
| Logic "1" C urrent | Full | VI |  |  | 20 |  |  | 20 | $\mu \mathrm{A}$ |
| Logic "0" C urrent | Full | VI |  |  | 800 |  |  | 800 | $\mu \mathrm{A}$ |
| Input Capacitance | $+25^{\circ} \mathrm{C}$ | V |  | 5 |  |  | 5 |  | pF |
| Pulse Width (High) | $+25^{\circ} \mathrm{C}$ | 1 | 6 |  |  | 6 |  |  | ns |
| Pulse Width (Low) | $+25^{\circ} \mathrm{C}$ | I | 6 |  |  | 6 |  |  | ns |
| DIGITAL OUTPUTS |  |  |  |  |  |  |  |  |  |
| Logic " 1 " Voltage ( $\mathrm{I}_{\text {OH }}=2 \mathrm{~mA}$ ) | Full | VI | 2.4 |  |  | 2.4 |  |  | V |
| Logic "0" Voltage ( $\mathrm{l}_{\mathrm{oL}}=6 \mathrm{~mA}$ ) | Full | VI |  |  | 0.4 |  |  |  | V |
| POWER SUPPLY |  |  |  |  |  |  |  |  |  |
| + $\mathrm{V}_{\text {S }}$ Supply Current | $+25^{\circ} \mathrm{C}$ | 1 |  | 440 | 530 |  | 440 | 530 | mA |
|  | Full | VI |  |  | 542 |  |  | 542 | mA |
| - $\mathrm{V}_{\text {S }}$ Supply Current | $+25^{\circ} \mathrm{C}$ | I |  | 140 | 170 |  | 140 | 170 | mA |
|  | Full | VI |  |  | 177 |  |  | 177 | mA |
| Power Dissipation | $+25^{\circ} \mathrm{C}$ | I |  | 2.8 | 3.3 |  | 2.8 | 3.3 | W |
|  | Full | VI |  |  | 3.4 |  |  | 3.4 | W |
| Power Supply Rejection Ratio (PSRR) ${ }^{8}$ | Full | VI |  | 6 | 10 |  | 6 | 10 | mV/V |

NOTES
${ }^{1}$ A bsolute maximum ratings are limiting values to be applied individually, and beyond which the service ability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
${ }^{2} \mathrm{~T}$ ypical thermal impedances (part soldered onto board): 68-pin leaded ceramic chip carrier: $\theta_{\mathrm{JC}}=1^{\circ} \mathrm{C} / \mathrm{W} ; \theta_{\mathrm{JA}}=17^{\circ} \mathrm{C} / \mathrm{W}$ (no air flow); $\theta_{\mathrm{JA}}=15^{\circ} \mathrm{C} / \mathrm{W}$
(air flow $=500 \mathrm{LFM}$ ). 68-pin ceramic LCC: $\theta_{\mathrm{J}}=2.6^{\circ} \mathrm{C} / \mathrm{W} ; \theta_{\mathrm{JA}}=15^{\circ} \mathrm{C} / \mathrm{W}$ (no air flow); $\theta_{\mathrm{JA}}=13^{\circ} \mathrm{C} / \mathrm{W}$ (air flow $=500 \mathrm{LFM}$ ).
${ }^{3} 3 / 4_{\mathrm{REF}}, 1 / 2_{\mathrm{REF}}$, and $1 / 4_{\mathrm{REF}}$ reference ladder taps are driven from dc sources at $+0.875 \mathrm{~V}, 0 \mathrm{~V}$, and -0.875 V , respectively. Accuracy of the overflow comparator is not tested and not included in linearity specifications.
${ }^{4} \mathrm{M}$ easured with ANALOG IN $=+\mathrm{V}_{\text {SENSE }}$.
${ }^{5}$ O utput delay measured as worst-case time from $50 \%$ point of the rising edge of ENCODE to $50 \%$ point of the slowest rising or falling edge of $D_{0}-D_{g}$. Output skew measured as worst-case difference in output delay among $D_{0}-D_{9}$.
${ }^{6}$ RM S signal to rms noise with analog input signal 1 dB below full scale at specified frequency.
${ }^{7}$ Intermodulation measured with analog input frequencies of 2.3 M Hz and 3.0 M Hz at 7 dB below full scale.
${ }^{8} \mathrm{M}$ easured as the ratio of the worst-case change in transition voltage of a single comparator for a $5 \%$ change in $+\mathrm{V}_{\mathrm{S}}$ or $-\mathrm{V}_{\mathrm{S}}$.
Specifications subject to change without notice.

## EXPLANATION OF TEST LEVELS

T est Level
| - 100\% production tested.
II - $100 \%$ production tested at $+25^{\circ} \mathrm{C}$, and sample tested at specified temperatures.
III - Sample tested only.
IV - Parameter is guaranteed by design and characterization testing.
V - Parameter is a typical value only.
VI - All devices are $100 \%$ production tested at $+25^{\circ} \mathrm{C} .100 \%$ production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

DIE LAYOUT AND MECHANICAL INFORMATION

| Die Dimensions | $206 \times 140 \times 15( \pm 2)$ mils |
| :---: | :---: |
| Pad Dimensions | . . . . . . . . . $4 \times 4$ mils |
| M etalization | G old |
| Backing | N one |
| Substrate Potential | -V |
| Passivation | N itride |



ORDERING GUIDE

| Device | Temperature Range | Description | Package Option* |
| :---: | :---: | :---: | :---: |
| AD 9020JZ | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 68-Pin Leaded Ceramic | Z-68 |
| AD 9020JE | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 68-T erminal Ceramic LCC | E-68A |
| AD 9020K Z | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 68-Pin Leaded Ceramic | Z-68 |
| AD 9020K E | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | 68-T erminal C eramic LCC | E-68A |
| AD 9020SZ/883 | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | 68-Pin Leaded Ceramic | Z-68 |
| AD 9020SE/883 | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | 68-T erminal C eramic LCC | E-68A |
| AD 9020T Z/883 | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | 68-Pin Leaded Ceramic | Z-68 |
| AD 9020TE/883 | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | 68-T erminal Ceramic LCC | E-68A |
| AD 9020/PC B | $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ | Evaluation Board |  |

*E = C eramic Leadless C hip C arrier; Z = Ceramic Leaded Chip C arrier.


AD9020 Burn-In Circuit


## AD9020 PIN FUNCTION DESCRIPTIONS

| Pin No. | Name | Function |
| :---: | :---: | :---: |
| 1 | $1 / 2_{\text {REF }}$ | M idpoint of internal reference ladder. |
| $\begin{aligned} & 2,16,28,29,35,41,42, \\ & 54,64 \end{aligned}$ | - $\mathrm{V}_{\text {S }}$ | N egative supply voltage; nominally $-5.0 \mathrm{~V} \pm 5 \%$. |
| $\begin{aligned} & 3,6,15,18,25,30,33,34 \\ & 37,40,45,52,55,65,68 \end{aligned}$ | $+\mathrm{V}_{5}$ | Positive supply voltage; nominally $+5 \mathrm{~V} \pm 5 \%$. |
| $\begin{aligned} & 4,5,13,17,27,31,32 \\ & 36,38,39,43,53,66,67 \end{aligned}$ | GROUND | All ground pins should be connected together and to low impedance ground plane. |
| 7 | $3 / 4_{\text {REF }}$ | T hree-quarter point of internal reference ladder. |
| 8, 9 | ANALOG IN | Analog input; nominally between $\pm 1.75 \mathrm{~V}$. |
| 11 | $+\mathrm{V}_{\text {SENSE }}$ | Voltage sense line to most positive point on internal resistor ladder. N ormally +1.75 V . |
| 12 | $+\mathrm{V}_{\text {REF }}$ | Voltage force connection for top of internal reference ladder. N ormally driven to provide +1.75 V at $+\mathrm{V}_{\text {SENSE }}$. |
| 14 | ENCODE | TTL-compatible convert command used to begin digitizing process. |
| 19-23, 46-50 | $\mathrm{D}_{0}-\mathrm{D}_{9}$ | T TL-compatible digital output data. |
| 51 | OVERFLOW | TTL-compatible output indicating ANALOG IN $>+\mathrm{V}_{\text {SENSE }}$. |
| 56 | - $\mathrm{V}_{\text {REF }}$ | Voltage force connection for bottom of internal reference ladder. N ormally driven to provide -1.75 V at $-\mathrm{V}_{\text {SENSE }}$. |
| 57 | $-\mathrm{V}_{\text {SENSE }}$ | Voltage sense line to most negative point on internal resistor ladder. N ormally -1.75 V . |
| 59 | LSBs INVERT | $N$ ormally grounded. When connected to $+V_{5}$, lower order bits $\left(D_{0}-D_{8}\right)$ are inverted. |
| 61 | M SB INVERT | $N$ ormally grounded. When connected to $+V_{5}$, most significant bit (MSB; $D_{g}$ ) is inverted. |
| 63 | $1 / 4_{\text {REF }}$ | One-quarter point of internal reference ladder. |

## AD9020

## THEORY OF OPERATION

Refer to the AD 9020 block diagram. As shown, the AD 9020 uses a modified "flash," or parallel, A/D architecture. T he analog input range is determined by an external voltage reference $\left(+V_{\text {REF }}\right.$ and $\left.-\mathrm{V}_{\text {REF }}\right)$, nominally $\pm 1.75 \mathrm{~V}$. An internal resistor ladder divides this reference into 512 steps, each representing two quantization levels. T aps along the resistor ladder ( $1 / 4_{\text {REF }}$, $1 / 2_{\text {REF }}$ and $3 / 4_{\text {REF }}$ ) are provided to optimize linearity. Rated performance is achieved by driving these points at $1 / 4,1 / 2$ and $3 / 4$, respectively, of the voltage reference range.
The A/D conversion for the nine most significant bits (M SBs) is performed by 512 comparators. The value of the least significant bit (LSB) is determined by a unique interpolation scheme between adjacent comparators. The decoding logic processes the comparator outputs and provides a 10-bit code to the output stage of the converter.
Flash architecture has an advantage over other A/D architectures because conversion occurs in one step. This means the performance of the converter is primarily limited by the speed and matching of the individual comparators. In the AD 9020, an innovative interpolation scheme takes advantage of flash architecture but minimizes the input capacitance, power and device count usually associated with that method of conversion.

These advantages occur by using only half the normal number of input comparator cells to accomplish the conversion. In addition, a proprietary decoding scheme minimizes error codes. Input control pins allow the user to select from among Binary, Inverted Binary, T wos C omplement and Inverted T wos Complement coding (see AD 9020 T ruth T able).

## APPLICATIONS

M any of the specifications used to describe analog/digital converters have evolved from system performance requirements in these applications. Different systems emphasize particular specifications, depending on how the part is used. The following applications highlight some of the specifications and features that make the AD 9020 attractive in these systems.

## Wideband Receivers

Radar and communication receivers (baseband and direct IF digitization), ultrasound medical imaging, signal intelligence and spectral analysis all place stringent ac performance requirements on analog-to-digital converters (ADCs). F requency domain characterization of the AD 9020 provides signal-to-noise ratio (SNR) and harmonic distortion data to simplify selection of the ADC.

Receiver sensitivity is limited by the Signal-to-N oise Ratio of the system. The SNR for an ADC is measured in the frequency domain and calculated with a F ast F ourier T ransform (FFT). The SN R equals the ratio of the fundamental component of the signal (rms amplitude) to the rms value of the noise. The noise is the sum of all other spectral components, including harmonic distortion, but excluding dc.
Good receiver design minimizes the level of spurious signals in the system. Spurious signals developed in the ADC are the result of imperfections in the device transfer function (nonlinearities, delay mismatch, varying input impedance, etc.). In the ADC, these spurious signals appear as H armonic Distortion. H armonic Distortion is also measured with an FFT and is specified as the ratio of the fundamental component of the signal (rms amplitude) to the rms value of the worst case harmonic (usually the 2nd or 3rd).
Two-T one Intermodulation Distortion (IM D) is a frequently cited specification in receiver design. In narrow-band receivers, thirdorder IM D products result in spurious signals in the pass band of the receiver. Like mixers and amplifiers, the ADC is characterized with two, equal-amplitude, pure input frequencies. The IM D equals the ratio of the power of either of the two input signals to the power of the strongest third-order IM D signal. Unlike mixers and amplifiers, the IM D does not always behave as it does in linear devices (reduced input levels do not result in predictable reductions in IM D ).
Performance graphs provide typical harmonic and SN R data for the AD 9020 for increasing analog input frequencies. In choosing an A/D converter, always look at the dynamic range for the analog input frequency of interest. The AD 9020 specifications provide guaranteed minimum limits at three analog test frequencies.
A perture $D$ elay is the delay between the rising edge of the EN CODE command and the instant at which the analog input is sampled. M any systems require simultaneous sampling of more than one analog input signal with multiple ADCs. In these situations, timing is critical and the absolute value of the aperture delay is not as critical as the matching between devices.
A perture U ncertainty, or jitter, is the sample-to-sample variation in aperture delay. This is especially important when sampling high slew rate signals in wide bandwidth systems. A perture uncertainty is one of the factors that degrade dynamic performance as the analog input frequency is increased.

## Digitizing Oscilloscopes

Oscilloscopes provide amplitude information about an observed waveform with respect to time. Digitizing oscilloscopes must accurately sample this signal, without distorting the information to be displayed.
One figure of merit for the ADC in these applications is Effective N umber of Bits (ENOBs). ENOB is calculated with a sine wave curve fit and equals:

$$
E N O B=N-L O G_{2}[\text { Error (measured)/Error (ideal) }]
$$

$N$ is the resolution (number of bits) of the ADC. The measured error is the actual rms error calculated from the converter outputs with a pure sine wave input.
The A nalog B andwidth of the converter is the analog input frequency at which the spectral power of the fundamental signal is reduced 3 dB from its low frequency value. $T$ he analog bandwidth is a good indicator of a converter's stewing capabilities.

The $M$ aximum Conversion $R$ ate is defined as the encode rate at which the SNR for the lowest analog signal test frequency tested drops by no more than 3 dB below the guaranteed limit.

## Imaging

Visible and infrared imaging systems both require similar characteristics from AD C s. The signal input (from a CCD camera, or multiplexer) is a time division multiplexed signal consisting of a series of pulses whose amplitude varies in direct proportion to the intensity of the radiation detected at the sensor. These varying levels are then digitized by applying encode commands at the correct times, as shown below.


Imaging Application Using AD9020

The actual resolution of the converter is limited by the thermal and quantization noise of the ADC. The low frequency test for SNR or ENOB is a good measure of the noise of the AD 9020. At this frequency, the static errors in the ADC determine the useful dynamic range of the ADC.
Although the signal being sampled does not have a significant slew rate, this does not imply dynamic performance is not important. The T ransient R esponse and O vervoltage Recovery Time specifications insure that the ADC can track full-scale changes in the analog input sufficiently fast to capture a valid sample.
T ransient Response is the time required for the AD 9020 to achieve full accuracy when a step function is applied. O vervoltage Recovery Time is the time required for the AD 9020 to recover to full accuracy after an analog input signal $150 \%$ of full scale is reduced to the full-scale range of the converter.

## Professional Video

Digital Signal Processing (DSP) is now common in television production. M odern studios rely on digitized video to create state-of-the-art special effects. Video instrumentation also requires high resolution ADCs for studio quality measurement and frame storage.
The AD 9020 provides sufficient resolution for these demanding applications. C onversion speed, dynamic performance and ana$\log$ bandwidth are suitable for digitizing both composite and RGB video sources.

## AD9020

## USING THE AD9020

## Voltage References

The AD 9020 requires that the user provide two voltage references: $+\mathrm{V}_{\text {REF }}$ and $-\mathrm{V}_{\text {REF }}$. T hese two voltages are applied across an internal resistor ladder (nominally $37 \Omega$ ) and set the analog input voltage range of the converter. T he voltage references should be driven from a stable, low impedance source. In addition to these two references, three evenly spaced taps on the resistor ladder ( $1 / 4_{\text {REF }}, 1 / 2_{\text {REF }}, 3 / 4_{\text {REF }}$ ) are available. Providing a reference to these quarter points on the resistor ladder will improve the integral linearity of the converter and improve ac performance. (AC and dc specifications are tested while driving the quarter points at the indicated levels.) The figure below is not intended to show the transfer function of the ADC, but illustrates how the linearity of the device is affected by reference voltages applied to the ladder.


## Effect of Reference Taps on Linearity

Resistance between the reference connections and the taps of the first and last comparators causes offset errors. These errors, called "top and bottom of the ladder offsets," can be nulled by using the voltage sense lines, $+\mathrm{V}_{\text {SENSE }}$ and $-\mathrm{V}_{\text {SENSE }}$, to adjust the reference voltages. Current through the sense lines should be limited to less than $100 \mu \mathrm{~A}$. Excessive current drawn through the voltage sense lines will affect the accuracy of the sense line voltage.
The next page shows a reference circuit which nulls out the offset errors using two op amps and provides appropriate voltage references to the quarter-point taps. F eedback from the sense lines causes the op amps to compensate for the offset errors. The two transistors limit the amount of current drawn directly from the op amps; resistors at the base connections stabilize their operation. The $10 \mathrm{k} \Omega$ resistors (R1-R4) between the voltage sense lines form an external resistor ladder; the quarter point voltages are taken off this external ladder and buffered by an op amp. The actual values of resistors R1-R4 are not critical, but they should match well and be large enough ( $\geq 10 \mathrm{k} \Omega$ ) to limit the amount of current drawn from the voltage sense lines.

The select resistors $\left(R_{s}\right)$ shown in the schematic (each pair can be a potentiometer) are chosen to adjust the quarter-point voltage references, but are not necessary if R1-R 4 match within 0.05\%.

An alternative approach for defining the quarter-point references of the resistor ladder is to evaluate the integral linearity error of an individual device, and adjust the voltage at the quarter-points to minimize this error. This may improve the low frequency ac performance of the converter.
Performance of the AD 9020 has been optimized with an analog input voltage of $\pm 1.75 \mathrm{~V}$ (as measured at $\pm \mathrm{V}_{\text {SENSE }}$ ). If the analog input range is reduced below these values, relatively larger differential nonlinearity errors may result because of comparator mismatches. As shown in the figure below, performance of the converter is a function of $\pm \mathrm{V}_{\text {SENSE }}$.


## AD9020 SNR and ENOB vs. Reference Voltage

Applying a voltage greater than 4 V across the internal resistor ladder will cause current densities to exceed rated values, and may cause permanent damage to the AD 9020. The design of the reference circuit should limit the voltage available to the references.

## Analog Input Signal

The signal applied to AN ALOG IN drives the inputs of 512 parallel comparator cells (see Equivalent Analog Input figure). T his connection typically has an input resistance of $7 \mathrm{k} \Omega$, and input capacitance of 45 pF . The input capacitance is nearly constant over the analog input voltage range, as shown in the graph which illustrates that characteristic.
The analog input signal should be driven from a low distortion, low noise amplifier. A good choice is the AD 9617, a wide bandwidth, monolithic operational amplifier with excellent ac and dc performance. The input capacitance should be isolated by a small series resistor ( $24 \Omega$ for the AD 9617) to improve the ac performance of the amplifier (see AD 9020/PCB Evaluation Board Block Diagram).


AD9020 Reference Circuit


AD9020 Equivalent Analog Input


AD9020 Equivalent Digital Outputs


AD9020 Equivalent Encode Circuit


AD9020 Timing Diagram

## Timing

In the AD 9020, the rising edge of the ENCODE signal triggers the A/D conversion by latching the comparators. (See the AD 9020 Timing Diagram.)
The ENCODE is TTL/CMOS compatible and should be driven from a low jitter (phase noise) source. Jitter on the EN CODE signal will raise the noise floor of the converter. F ast, clean edges will reduce the jitter in the signal and allow optimum ac performance. Locking the system clock to a crystal oscillator also helps reduce jitter. The AD 9020 is designed to operate with a $50 \%$ duty cycle; small ( $10 \%$ ) variations in duty cycle should not degrade performance.

## Data Format

The format of the output data ( $\mathrm{D}_{0}-\mathrm{D}_{9}$ ) is controlled by the M SB INVERT and LSBsINVERT pins. These inputs are dc control inputs, and should be connected to GROUND or $+\mathrm{V}_{\mathrm{s}}$. The AD 9020 T ruth T able gives information to choose from among Binary, Inverted Binary, T wos Complement and Inverted T wos Complement coding.
The OVERFLOW output is an indication that the analog input signal has exceeded the voltage at $+\mathrm{V}_{\text {SENSE }}$. $T$ he accuracy of the overflow transition voltage and output delay are not tested or included in the data sheet limits. Performance of the overflow indicator is dependent on circuit layout and slew rate of the encode signal. The operation of this function does not affect the other data bits ( $\mathrm{D}_{0}-\mathrm{D}_{9}$ ). It is not recommended for applications requiring a critical measure of the analog input voltage.

## Layout and Power Supplies

Proper layout of high speed circuits is always critical but is particularly important when both analog and digital signals are involved.

A nalog signal paths should be kept as short as possible and be properly terminated to avoid reflections. The analog input voltage and the voltage references should be kept away from digital signal paths; this reduces the amount of digital switching noise that is capacitively coupled into the analog section of the circuit. D igital signal paths should also be kept short, and run lengths should be matched to avoid propagation delay mismatch.
In high speed circuits, layout of the ground circuit is a critical factor. A single, low impedance ground plane, on the component side of the board, will reduce noise on the circuit ground. Power supplies should be capacitively coupled to the ground plane to reduce noise in the circuit. M ultilayer boards allow designers to lay out signal traces without interrupting the ground plane and provide low impedance power planes.
It is especially important to maintain the continuity of the ground plane under and around the AD 9020. In systems with dedicated digital and analog grounds, all grounds of the AD 9020 should be connected to the analog ground plane.
The power supplies ( $+\mathrm{V}_{\mathrm{S}}$ and $-\mathrm{V}_{\mathrm{S}}$ ) of the AD 9020 should be isolated from the supplies used for external devices; this further reduces the amount of noise coupled into the A/D converter. Sockets limit the dynamic performance and should be used only for prototypes or evaluation-PCK Elastomerics Part \# CCS-6855 is recommended for the LCC package. (Tel. 215-672-0787)
An evaluation board is available to aid designers and provide a suggested layout.


AD9020 SNR and ENOB vs. Input Frequency


AD9020 Harmonics vs. Input Frequency


AD9020 SNR and ENOB vs. Conversion Rate


Input Capacitance/Resistance vs. Input Voltage

AD9020 Truth Table

| Step | $\begin{gathered} \text { Range } \\ 0=-1.75 V \\ F S=+1.75 V \end{gathered}$ | Offset Binary |  | Twos Complement |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\begin{gathered} \text { True } \\ \text { MSB INV = " } 0 \text { " } \\ \text { LSBS INV = " } 0 \text { " } \end{gathered}$ | $\begin{gathered} \text { Inverted } \\ \text { MSB INV ="1" } \\ \text { LSBs INV ="1" } \end{gathered}$ | $\begin{gathered} \text { True } \\ \text { MSB INV = " } 1 " \\ \text { LSBs INV = " } 0 \text { " } \end{gathered}$ | $\begin{gathered} \text { Inverted } \\ \text { MSB INV =" } 0 \text { " } \\ \text { LSBs INV = " } 1 \text { " } \end{gathered}$ |
| 1024 | > +1.7500 | (1)1111111111 | (1)0000000000 | (1)0111111111 | (1)1000000000 |
| 1023 | +1.7466 | 1111111111 | 0000000000 | 0111111111 | 1000000000 |
| 1022 | +1.7432 | 1111111110 | 0000000001 | 0111111110 | 1000000001 |
| - | - | - | - | - | - |
| - | - | - | - | - |  |
| 512 | +0.0034 | 1000000000 | 0111111111 | 0000000000 | 1111111111 |
| 511 | 0.000 | 0111111111 | 1000000000 | 1111111111 | 0000000000 |
| 510 | -0.0034 | 0111111110 | 1000000001 | 1111111110 | 0000000001 |
| - | - | - | - | - | - |
| - | - | - | - | - | - |
| 02 | -1.7432 | 0000000010 | 1111111101 | 1000000010 | 0111111101 |
| 01 | -1.7466 | 0000000001 | 1111111110 | 1000000001 | 0111111110 |
| 00 | <-1.7466 | 0000000000 | 1111111111 | 1000000000 | 0111111111 |

The overflow bit is always 0 except where noted in parentheses ( ). MSB INVERT and LSBs INVERT are considered dc controls.

## AD 9020/PCB EVALUATION BOARD

The AD 9020/PCB Evaluation Board is available from the factory and is shown here in block diagram form. The board includes a reference circuit that allows the user to adjust both references and the quarter-point voltages. The AD 9617 is included as the drive amplifier, and the user can configure the gain from -1 to -15 .

On-board reconstruction of the digital data is provided through the AD 9713, a 12-bit monolithic DAC. The analog and reconstructed waveforms can be summed on the board to allow the user to observe the linearity of the AD 9020 and the effects of the quarterpoint voltages. T he digital data and an adjustable D ata Ready signal are available through a 37-pin edge connector.


AD9020/PCB Evaluation Board Block Diagram

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

68-Leaded Ceramic Chip Carrier (Z-68)


## 68-Terminal Leadless Chip Carrier (LCC) (E-68A)




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